ShanghaiTech University
School of Information Science and Technology

EE112 Lab Experiments

Experiment 2: Diodes, Bipolar Junction Transistors and MOS Characterization

Contents

1. Introduction

The diodes, bipolar junction transistors and MOS are basic circuit elements in the integrated circuits. Having a good grasp of the basic characteristics is the key to understand their operation and applications. In this lab, we will explore the characteristics of those devices. Make sure to download and print out the Pre-Lab Worksheet and the Lab Worksheet. Make sure to complete the Pre-Lab section before coming to lab. Your lab TAs will check that you have completed the Pre-Lab Worksheet at the beginning of your lab section. Fill out the Lab Worksheet while doing the lab and turn it in with supporting traces and plots to your TAs at the beginning of the lab section

for Lab 3.

2. Materials

The items listed in Table (1) will be needed. *Note: Be sure to answer the questions on the report as you proceed through this lab. The report questions are labeled according to the section in the experiment.*

Table 1: Lab 2 Components

Component	Quantity
Diode 1N4148	1
NPN BJT 2N4401	1
NMOSFET BS170N	1

3. Pre-Lab

3.1. Junction capacitance

Read the Lab21_Primer1 and Lab2_Primer2. Measure the junction capacitance of 1N4148 under various reverse voltage in Multisim based on the method provided in Lab2_Primer2.

3.2. I-V measurement of NMOS

2-Wire Current-Voltage Analyzer for diode and 3-Wire Current-Voltage Analyzer for NPN, PNP have been provided in ELVISmx. By Labview programming, design your own 3-Wire Current-Voltage Analyzer, which can be used to measure the I-V curve of NMOS in Elvis II. To measure the current, 100 Ω sampling resistor is recommended.

4. Lab

4.1. Diode Parameter Characteristic

4.1.1. I-V Measurements

Connect the silicon diode to the 2-Wire Current-Voltage Analyzer in Elvis II. Sweep the voltage from −1V to 1V to generate the I-V curve. Based on the diode equation $I_D = I_s(e^{V_D/nV_T} - 1)$, extrapolate the saturation current I_s, ideality factor n from the I-V data. At high current injection, the current is limited by the series resistance R_s. Identify the series resistance limited region in the I-V curve and measure this series

resistance.

4.1.2. Diode Capacitance Measurements

Reverse bias the diode with voltage from 1V to 5V with 1V step and measure the capacitance of the reverse-biased PN junction. Note: The capacitance measurement will be performed using the Bode Analyzer in Elvis II based on the method in Lab2_Primer2. Fit the capacitance with the step junction model and calculate the zero bias junction capacitance C_{j0}.

4.2. Bipolar Junction Transistor Characterization

The bipolar junction transistor BJT was invented in 1948 by William Shockley at Bell Labs, and became the first mass-produced transistor. In this lab, we will explore the BJTs four regions of operation and also determine its characteristic values. The transistor used in this lab is the 2N4401, an NPN device. It is strongly recommended that you read and understand the section on BJT physics before beginning this experiment.

4.2.1. I-V measurements

The schematic of 2N4401 NPN BJT is shown in Fig. 1. Connect the transistor to the 3-Wire Current-Voltage Analyzer in Elvis II. Set the base current bias from 1 µA to 5 µA, with 1 µA step, measure the corresponding i_C v_{CE} curves. What is the forward current gain β_F? How does it depend on the collector current i_C? Based on the measured I-V curves, determine the early voltage V_A of the transistor from the average of the five measurements.

Fig. 1 2N4401 Schematic.

4.2.2. Base Collector Junction Capacitance Measurements

Measure the base collector junction capacitance CBC under different reversed bias voltage, from 1V to 5V with 1V step. Fit the capacitance with the step junction model and calculate the zero bias junction capacitance C_{j0}.

4.3. MOSFET Characterization

The MOS transistor is another circuit element typically used in integrated circuits. Although they have similar functions to BJTs and can be placed into several analogous topology (e.g. the cascode, common drain, common gate, common source), MOS transistors are completely different in terms of their characteristics and physical mechanisms underlying their operation. The NMOSFET BS170 will be characterized in this lab. **By Labview programming, design your own 3-Wire Current-Voltage Analyzer for NMOS in Elvis II. To measure the current, 100 Ω sampling resistor is recommended.**

4.3.1. I-V Measurements

For BS170 NMOS transistor (Fig. 2)), the configuration for the I-V measurement is shown in Fig. 3. Step V_G from 2.0 V to 2.3 V in 0.05 V increments and sweep V_D from 0 V to 3 V to obtain the MOSFET I-V characterization curves. On the I-V family curves, label the cutoff, triode and saturation regions. Attach this plot in your lab report. What is the expression that describes the boundary between the saturation and triode region?

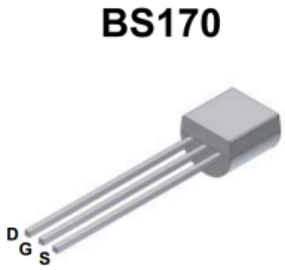

Fig. 2 BS170 Schematic.

Given a bias of V_{GS} = 2.1 V and V_{DS} = 1.5 V, extract the transconductance G_m. What region of operation is this? Given a bias of V_{GS} = 2.1 V and V_{DS} = 0.06 V, extract the transconductance G_m. What region of operation is this?

Using the I-V characteristic plot, extract the channel length modulation factor λ from the slop of the plot. Note that this will vary somewhat depending on which V_{GS} you use.

Now, connect the NMOS as shown in Fig. 4. Sweep V_G from 0 V to 2.5 V and measure the current V_D. Plot $I_D^{1/2}$ vs. V_G. Note: you may have to limit the range of the voltage to avoid taking the square root of the negative currents. $(1/2K_n)^{1/2}$ is the slope of the linear portion of the curve, find K_n. The threshold voltage V_{TH} can be found by measuring where the linear portion of the $I_D^{1/2}$ vs. V_G curve would intersect the V_G axis if it was extended. Find V_{TH}.

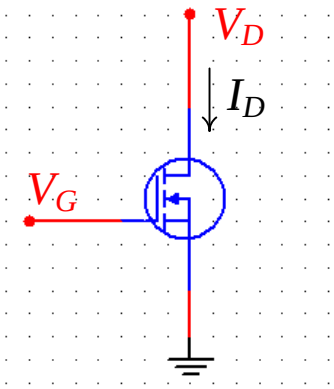

Fig. 3 NMOS I-V Measurement Configuration.

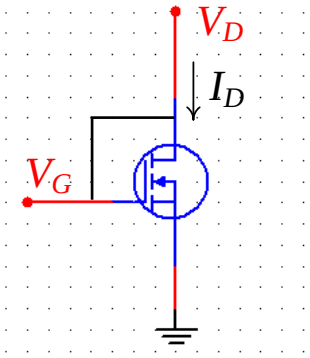

Fig. 4 NMOS Diode Connected Configuration.

4.3.2. C-V Measurements

Leaving the drain open, measure the capacitance between source and gate as a function of V_{gs} from 2.0 V to 2.3 V with 0.1 V step. Leaving the source open, measure capacitance C_{gd} with zero bias.

Reference

[1] UNIVERSITY OF CALIFORNIA AT BERKELEY, College of Engineering Department of Electrical Engineering and Computer Sciences, EE105 Lab Experiments.
[2] Drexel University, ECE-E302, Electronic Devices.