ShanghaiTech University
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EE112 Lab Experiments

Experiment 4: CMOS Inverter and Characterization

Contents

1 Introduction

Complementary MOSFET (CMOS) technology is widely used today to form circuits in numerous and varied applications. It has become the key elements in the today's integrated circuits due to several key advantages, such as low power dissipation, relatively high speed, high noise margins, etc. The CMOS inverter is one of the most basic logic circuit elements in the digital circuits. In this lab, we will build an inverter with a NMOS and a PMOS transistor and measure its basic characteristics.

2 Materials

The items listed in Table 1 will be needed. *Note: Be sure to answer the questions on the report as you proceed through this lab. The report questions are labeled according to the section in the experiment.*

Table 1: Lab 2 Components

Component	Quantity
NMOSFET BS250P	1
NMOSFET BS170N	1
100 nF Capacitor	1

3 Lab

3.1 PMOS Characterization

In Lab 2, we have characterized the NMOS transistor BS170N. In this section, we are going to perform the similar measurements for the PMOS transistor BS250P.

3.1.1 I-V Measurements

For BS250 PMOS transistor in Figure 1, set up the configuration for the I-V measurement as shown in Figure 2. Step V_G from −2.0V to −2.3V in 0.05V increments and sweep V_{DD} from 0V to −3V to obtain the MOSFET I-V characterization curves. On the I-V family curves, label the cutoff, triode and saturation regions. Attach this plot in your lab report. What is the expression that describes the boundary between the saturation and triode region?

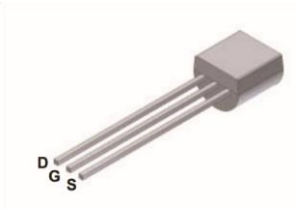

Figure 1: BS250 Schematic

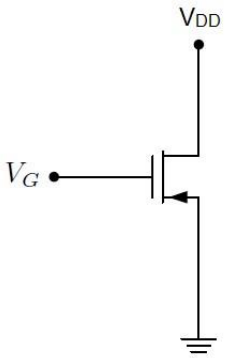

Figure 2: PMOS I-V Measurement Configuration

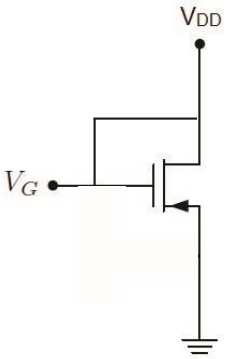

Figure 3: PMOS Diode Connected Configuration

Using the I-V characteristic plot, extract the channel length modulation factor λ from the slop of the plot. Note that this will vary somewhat depending on which VGS you use.

Now, connect the PMOS as shown in Figure (3). Sweep V_{GS} from 0V to -2.5V and measure the current ID. Plot $I_D^{1/2}$ *vs*. V_{GS}. Note: you may have to limit the range of the voltage to avoid taking the square root of the negative currents. $(1/(2K_p))^{1/2}$ is the slope of the linear portion of the

curve, find K_p. The threshold voltage V_{TP} can be found by measuring where the linear portion of the $I_D^{1/2}$ *vs*. V_{GS} curve would intersect the V_{GS} axis if it was extended. Find V_{TP}.

3.1.2 C-V Measurements

Using the technique provided in Lab 2 and leaving the drain open, measure the capacitance between source and gate as a function of V_{gs}. Sweep V_{gs} to cover all the operation regions. Leaving the source open, measure capacitance between drain and gate (C_{gd}) with zero bias.

3.2 CMOS Inverter

The circuit diagram of the CMOS inverter is shown in Figure 4. When the input is at low voltage, for example 0V, the NMOS is off while PMOS is on. Therefore, the output voltage should be at high voltage. On the other hand, when the input is at high voltage, the PMOS is off and the NMOS is on. The output voltage in this case is low.

3.2.1 Voltage Transfer Characteristics

Connect the circuit with the NMOS transistor BS170N and PMOS transistor BS250P. Measure the output voltage as a function of the input voltage V_{out} *vs.*V_{in}. Set the bias voltage V_{DD} = 5V, measure the input voltage from 0V to 5V. What is the maximum allowable input voltage at the low logic state (V_{IL}) and the minimum allowable input voltage at the logic high state (V_{IH})?

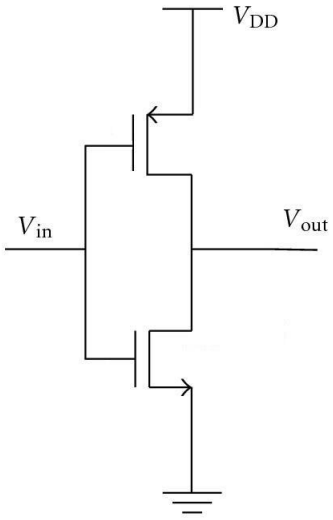

Figure 4: CMOS Inverter Circuit

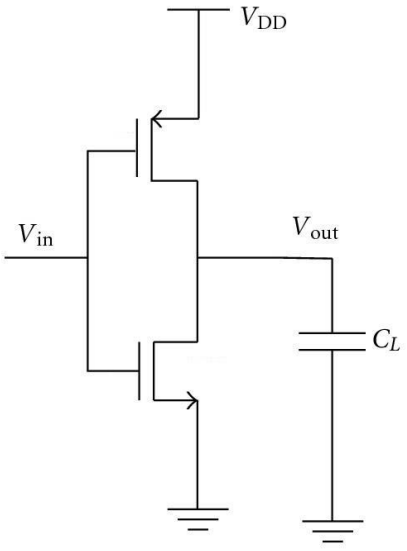

Figure 5: CMOS Inverter Transient Measurement Configuration with load capacitor

3.2.2 Transient Characteristics

Use the function generator to input a square wave signal with $V_L = 0$ and $V_H = 5$V. Use the oscilloscope to observe the input and the output signals for circuit shown in Figure 4. Measure the fall time t_f and rise time t_r. t_f is defined as the fall time for the voltage dropping from 90% to 10%. t_r is defined as the rise time for the voltage rising from 10% to 90%.

Add the load capacitor (10nF) to the inverter, shown in Figure 5. Repeat the measurement.

Reference

[1] UNIVERSITY OF CALIFORNIA AT BERKELEY, College of Engineering Department of Electrical Engineering and Computer Sciences, EE105 Lab Experiments