ShanghaiTech University
School of Information Science and Technology

EE112 Lab Experiments

Experiment 4: Primer and Prelab

CMOS Inverters:

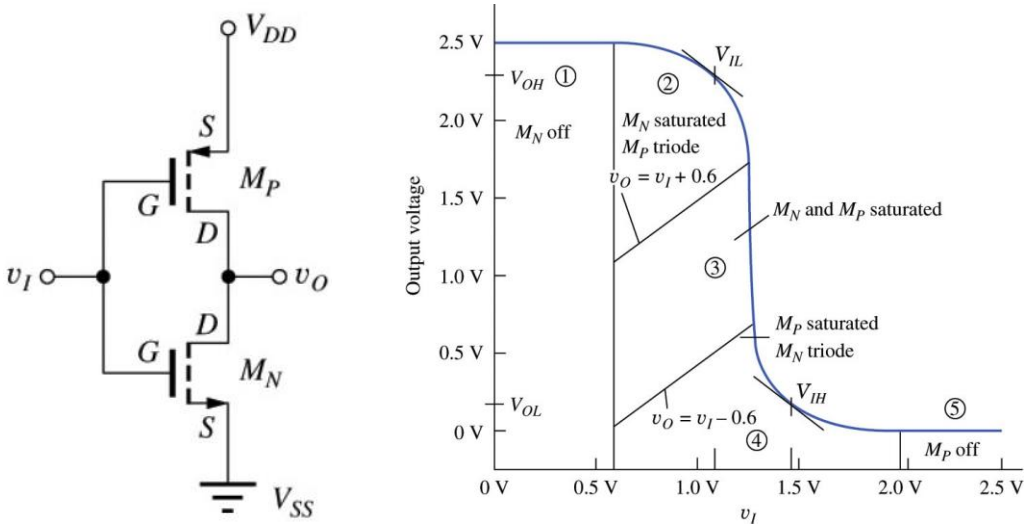

Fig. 1 (a) CMOS inverter circuit. (b) Schematic transfer characteristics showing five regions of operations.

Table 1: Regions of Operation of NMOS and PMOS in CMOS Inverters				
Region	v_I	v_o	**NMOS**	**PMOS**
1	$v_I < V_{TN}$	$V_H \sim V_{DD}$	Cutoff	Triode
2	$V_{TN} < v_I < v_O - \|V_{TP}\|$	High	Saturation	Triode
3	$v_O - \|V_{TP}\| < v_I < v_O + V_{TN}$	$\sim V_{DD}/2$ **	Saturation	Saturation
4	$v_O + V_{TN} < v_I < V_{DD} - \|V_{TP}\|$	Low	Triode	Saturation
5	$V_{DD} - \|V_{TP}\| < v_I$	$V_L \sim 0$	Triode	Cutoff

* Note: V_{TP} is usually a negative number.
** v_O changes rapidly with v_I in Region 3, the precise value depends on the slope of their *i-v* curves in the saturation region.

Figure 1 shows the circuit diagram and the schematic transfer characteristics of a CMOS inverter. (Please ignore the voltage scale in the transfer curve. It was obtained with $V_{DD} = 2.5$V. We will be using 5V and different transistors). There are five regions of operation, as shown in Table 1. To calculate the theoretical transfer curve, you need to use the equations corresponding to the operation regions of NMOS and PMOS, respectively. For example, in Region 2,

$$i_{D,NMOS} = \frac{K_n}{2}(v_{GS,N} - V_{TN})^2 = \frac{K_n}{2}(v_I - V_{TN})^2$$

$$i_{D,PMOS} = K_p\left(|v_{GS,P}| - |V_{TP}| - \frac{|v_{DS,P}|}{2}\right)|v_{DS,P}| = K_p\left((V_{DD} - v_I) - |V_{TP}| - \frac{(V_{DD} - v_O)}{2}\right)(V_{DD} - v_O)$$

Since $i_{D,NMOS}$=$i_{D,PMOS}$, we can solve v_O as a function of v_I. After you solve v_O, you should verify that indeed NMOS is in saturation and PMOS is in triode regime (by comparing v_{DS} and v_{GS} - $V_{TN(P)}$).

Likewise, in Region 4, NMOS is in triode and PMOS is in saturation:

$$i_{D,NMOS} = K_n(v_{GS,N} - V_{TN} - \frac{v_{DS,N}}{2})v_{DS,N} = K_n(v_I - V_{TN} - \frac{v_O}{2})v_O$$

$$i_{D,PMOS} = \frac{K_p}{2}\left(|v_{GS,P}| - |V_{TP}|\right)^2 = \frac{K_p}{2}\left(v_{DD} - v_I - |V_{TP}|\right)^2$$

Solve v_O as a function of v_I again and verify that operation regimes of NMOS and PMOS.

In Region 3, both NMOS and PMOS are in saturation region. To precisely determine v_O, you will need to include the channel length modulation parameters for *both* NMOS and PMOS:

$$i_{D,NMOS} = \frac{K_n}{2}(v_I - V_{TN})^2(1 + \lambda_N v_O)$$

$$i_{D,PMOS} = \frac{K_p}{2}\left(v_{DD} - v_I - |V_{TP}|\right)^2(1 + \lambda_P(V_{DD} - v_O))$$

PreLab Question:

You are highly encouraged to finish the Prelab before your Lab session. You will need this for your Lab Report, and you will be better off knowing how far your experimental and theoretical results while you are doing the experiments.

1. List the device parameters you have measured for *your* NMOS and PMOS. NMOS is from Lab 2, PMOS are from the first part of Lab 3):
   (Please include units in your list)
   V_{TN}= _____
   K_n= _____
   λ_N= _____
   V_{TP}= _____
   K_p= _____
   λ_P= _____

2. Solve the transfer curves in Region 2, 3, and 4 using the formulation above. Obtain analytical solutions. To simply your expression, you can use the parameter $K_R = K_N / K_P$

3. Plug in the values of *your* device parameters; plot the transfer curve for v_I from 0 to 5V (V_{DD}).

Reference

[1] UNIVERSITY OF CALIFORNIA AT BERKELEY, College of Engineering Department of Electrical Engineering and Computer Sciences, EE105 Lab Experiments