ShanghaiTech University
School of Information Science and Technology

EE112 Lab Experiments
Experiment 4: CMOS Inverter and Characterization

3 Lab

3.1 PMOS Characterization

Plot I_D *vs.* V_{DS} curves with different V_{GS}. Label the cutoff, triode and saturation regions on the plot.

What is the channel length modulation λ: _____ .

Plot $I_D^{1/2}$ vs. V_G, extract V_{TP} :_____and K_n : _____.

Plot C_{GS} *vs.* V_{GS} curve.

What zero bias drain gate capacitance C_{GD}: _____ .

3.2 CMOS Inverter

Plot V_{out} *vs.* V_{in} curves.

What is V_{IL} _____ and V_{IH} _____

Plot out the output signal $v_{out}(t)$ without load.

What is fall time t_f _____ and fall time t_r _____

Plot out the output signal $v_{out}(t)$ with 10nF load capacitor.

What is fall time t_f _____ and fall time t_r _____

Reference

[1] UNIVERSITY OF CALIFORNIA AT BERKELEY, College of Engineering Department of Electrical Engineering and Computer Sciences, EE105 Lab Experiments