ShanghaiTech University
School of Information Science and Technology
EE112 Lab Experiments

Lab 5: Multi-Stage Amplifiers Prelab

Contents

1. Introduction

Often, a single transistor amplifier cannot satisfy all of the specifications for a given application and an amplifier circuit is designed with multiple cascaded single-transistor amplifiers. In this lab, you will implement a three-stage amplifier, which will amplify an audio signal from a headphone jack and drive a low-impedance speaker.

Make sure to download and print out the Pre-Lab Worksheet and the Lab Worksheet. You may also find the datasheets for the transistors used in this lab to be useful: 2N4401, 2N4403, BS170.

Make sure to complete the Pre-Lab Worksheet before coming to lab. Your lab TA will check that you have completed the Pre-Lab Worksheet at the beginning of your lab section. Fill out the Pre-Lab and Lab Worksheet while doing the lab and turn them in with supporting traces and plots at the beginning of the first lab section for Lab 6.

2. Pre-Lab

Middle Band Gain (A_{mid})	10 ± 20 %
High Cutoff Frequency (f_H)	≥ 20 kHz
Output Swing (SW)	≥ 1 Vpp
Supply Voltage (V_{dd})	5 V
Output load (R_L)	8 Ω

Table 1: Amplifier specification

In this prelab, you will be designing an amplifier with the specifications as shown

in Table 1. The topology for your design is fixed and is shown in Figure 1.

Don’t worry if the circuit in Figure. 1 looks daunting. In this prelab, we will go through the design of the circuit step by step.

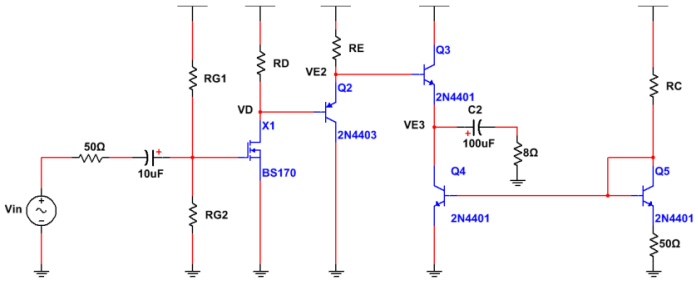

Figure 1: Circuit topology for Lab 5.

You will need to simulate your circuit with Multisim.

2.1 Back of the envelope determination of DC bias points

On your prelab worksheet, write simple analytical expressions for the DC bias voltages at V_D, V_{E2}, V_{E3}. You may leave your expressions in terms of V_{be}, I_D, etc. Ignore base currents and assume that the bipolar transistors have an infinite Early voltage and that the MOSFET has no channel-length modulation.

2.2 Input stage

The purpose of the input stage is to present a high input impedance to the voltage source and to provide voltage gain for the amplifier. Shown below in Figure 2 is the input stage of the amplifier.

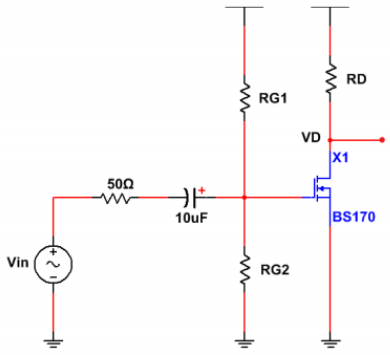

Figure 2: First stage circuit topology.

Since you are now an expert at designing common-source amplifier circuits after having completed Lab 3, design the first stage to have a gain of 10 ± 20%. Make sure that the drain voltage bias point will be compatible with the bias points required for the later stages and that the output voltage swing is greater than 1 Volt. Use the nMOS

device parameters that you characterized in Lab 2 for this stage. First do a back-of-the envelope hand calculation for your design, and verify your design and tweak parameters to achieve the specifications in Multisim.

In your prelab worksheet, write down the midband (no capacitors) small signal circuit for the input stage. Also write expressions for the midband gain, output resistance, and output swing. Fill out the tables in your prelab worksheet with the numerical values you obtained from hand calculation and simulation.

2.3 Output stage

Next, we will jump ahead and design the output stage. The purpose of the output stage is to provide enough current to be able to drive the low impedance 8 Ω speaker load. We will first analyze and design the common collector circuit with current source bias, and then later design an implementation of the current source. Again, design is to be done using hand calculations, followed by verification and design tweaking in Multisim.

2.3.1 Determination of bias current

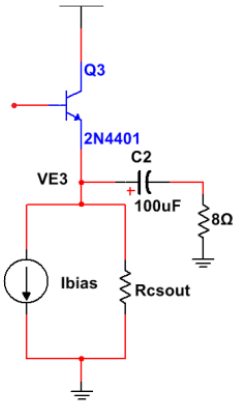

Figure 3: Output stage circuit topology, current source circuit not shown

The only design parameter for this stage is the current source value I_{bias}. We will do both a small signal and large signal analysis of the output stage and figure out two constraints for the value of the current source.

In your prelab worksheet, write down the small signal midband circuit for the output stage with 8 Ω speaker load, and write expressions for the midband voltage gain and input resistance of the circuit. How much bias current do we need to be able to get a voltage midband gain of 0.9? 0.99? Let $R_{csout} = r_o$ of the 2N4401 NPN transistor.

Next, analyze the output swing of the output stage, referring to the diagram in Figure 4. Treat the capacitor as an AC short. What is the maximum ac current that can be sourced from the supply? What is the maximum ac current that can be sunk to ground? What are the maximum and minimum output voltages of the stage, defining the output swing? Write expressions for the four values in your prelab worksheet.

From the expression for the minimum output voltage, what bias current is required to achieve a 1 Vpp or 0.5 V amplitude output swing? Write this value in your worksheet, and use this value in your design. Check the datasheet for the 2N4401 NPN transistor, and make sure that your designed I_{bias} is not higher than the maximum collector current rating, and that the power dissipation $P = I_{bias} \times V_{ce}$ in the bipolar transistor Q3 is less than the maximum power rating.

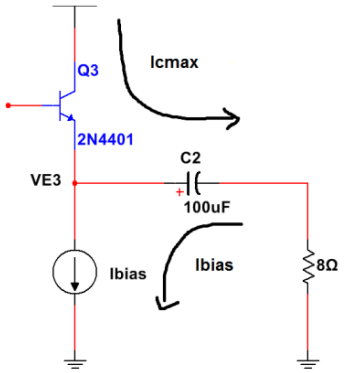

Figure 4: Output swing analysis showing maximum current excursions. For simplicity, the output resistance of the current source is not shown.

2.3.2 Current source design

Shown in Figure 5 is a diagram showing the current source circuit. The current source circuit is comprised of two parts. The right branch is a circuit which generates a bias voltage for the base of npn bipolar transistor Q4 on the left branch, which is acting as a current source load. Here, the design is to choose the proper value of R_C to generate the desired I_{bias}.

If you need help with the design, try the following method. Ignoring V_{ce} dependence on I_C and using KVL on the loop indicated on Figure 5, write an expression relating I_{bias} and I_{source}, and numerically solve for I_{source}. Next, applying KCL to the node connected to the two bases of the transistors, write an expression relating R_C to I_{bias} and I_{source}, and numerically solve for R_C.

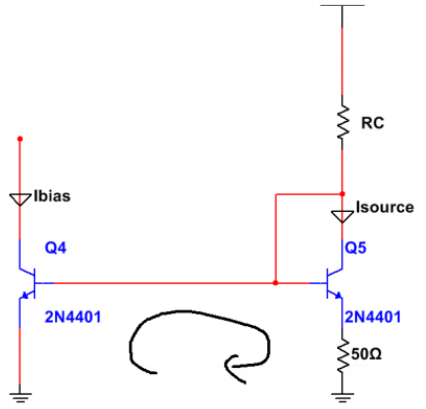

Figure 5: Current source circuit

Fill out the tables in your prelab worksheet with the numerical values you obtained from hand calculation and simulation. For the small signal values, make sure to do the Multisim simulations of the full output stage with transistor current source circuit and speaker load, and to set a DC bias voltage equal to V_{E2} for the input of transistor Q3. The hand calculation small signal values can be the values you calculated for the circuit with the transistor load modelled as a current source.

2.4 Middle stage

The middle stage primarily serves as an AC and DC buffer between the two stages. If we were to directly cascade the input and output stages together, the following two things would happen:

1. Because the bias current of the output stage is so much higher than the input stage, the base of the output drive transistor Q3 would draw significant current from R_D and totally alter the output bias point of the input stage.
2. The output impedance of the input stage and the input impedance of the output stage are of similar magnitudes. Not all of the voltage generated by the input stage would be coupled to the output stage due to the loading effect.

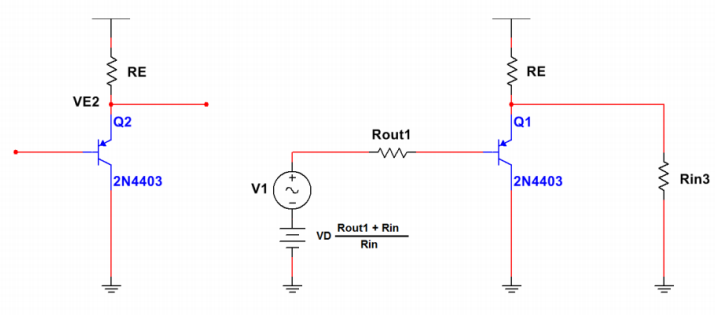

Figure 6: Middle stage circuit without and with input and output loading.

Shown in Figure 6 is the common collector circuit topology for the middle stage. The common collector topology is a good choice here because its output voltage bias point is not very sensitive to the bias current and because the common collector circuit has a high input impedance and a low output impedance, which is exactly what we need to couple voltage generated by the input stage to the output stage.

For this stage, the only design parameter is R_E. The following exercises will guide your design decision for the value of R_E. With loading from the output resistance of the input stage and input resistance of the output stage, draw the small signal circuit and write an expression for the 'loaded gain' of the circuit shown in Figure 6. It is important to notice that V_{E2} is mostly independent of R_E, and so the value of R_E sets the bias current as well as appears in the small signal circuit.

Next, we analyze the output swing of V_{E2}. What are the maximum and minimum output voltages of the stage, defining the output swing? Write expressions for these values in your prelab worksheet. Choose a value for R_E that both provides a loaded gain close to 1 and allows for a swing greater than 1 Vpp. Fill out the tables in your

worksheet with the numerical values you obtained from hand calculation and simulation of the middle stage.

2.5 Putting it all together

Now that you have designed and verified each of the three stages, cascade them together as shown in Figure 1. Simulate in Multisim the frequency response from 1 Hz to 20 kHz and verify the output swing of the entire circuit. Attach plots of the frequency response as well as a plot showing evidence of a 1 Vpp output swing of the entire amplifier.

Reference

[1] UNIVERSITY OF CALIFORNIA AT BERKELEY, College of Engineering Department of Electrical Engineering and Computer Sciences, EE105 Lab Experiments