ShanghaiTech University
School of Information Science and Technology
EE112 Lab Experiments

Lab 6: Differential Amplifier Prelab Worksheet

1. Pre-Lab

1.1 Differential Input Stage

Please draw the equivalent "half circuit" for the differential signals.

Please write down the expression of the differential voltage gain (A_{dm}= (V_{o1}−V_{o2})/V_{dm}):

_____

Please write down the expression of differential gain high cutoff frequency (f_{Hdm}):____

_____

Please write down the expression of maximum differential output swing and express it in terms of DC base voltage V_b:

For hand calculation only:

Resistor load R_1 and R_2:_____

Tail Current Source I_{bias}:_____

1.2 Widlar Current Source

Please write down the expression that relates I_{ref}, I_{bias}, V_t and R_4:

Please write down the expression that relates I_{ref}, V_{be3}, R_3, V_{DD} and V_{SS}:

Please write down the output impedance of current mirror (R_{out}):

Please write down the expression of the minimum allowable voltage on the collector of Q4:

According to the I_{bias} from previous section, select proper R_3 and R_4:_____

Verify the performance of the current source by Multisim simulation:

Design Parameter	Hand Calculation	Multisim Simulation
I_{bias}		
I_{ref}		
R_{out}		

Table 1: Widlar Current Source Design

1.3 Common Mode Characterization

Please draw the equivalent “half circuit” for common mode signal.

Please write down the expression of the common mode gain with 0.1% load resistor mismatch ($A_{cm} = (V_{o1} - V_{o2})/V_{dm}$):_____

The expression of minimal common input voltage:_____

The expression of maximum common input voltage:_____

1.4 Putting it all together

Now connect the current source and differential pair together and verify its performance in Multisim.

Performance	Hand Calculation	Multisim Simulation
Differential Mode Gain (A_{dm})		
Differential Mode Gain (A_{dm})		
Differential Output Swing (SW)		
Common Mode Gain (A_{cm}) with mismatch		
Common Mode rejection Ratio (CMRR) with mismatch		

Table 2: Overall performance verification

Attach the plot of transient waveform of ($V_{o1} - V_{o2}$) v.s. V_{dm} at a frequency below the cutoff frequency.

Attach the plot showing evidence of a 2 V differential output swing.

Attach the plot of the frequency response of A_{dm} from 10 Hz to 100 kHz.

Attach the plot of transient waveform of ($V_{o1} - V_{o2}$) v.s. V_{cm} with 0.1% load resistor mismatch.

Attach the plot of the frequency response of A_{cm} with 0.1% load resistor mismatch from 10 Hz to 100 kHz.

Reference

[1] UNIVERSITY OF CALIFORNIA AT BERKELEY, College of Engineering Department of Electrical Engineering and Computer Sciences, EE105 Lab Experiments