EE112 - Fall 2016
Analog Integrated Circuits I

Prof. Haoyu Wang
wanghy@shanghaitech.edu.cn
5210 Research Bldg.

Review: Ideal Op-Amp

- Infinite input impedance
  - » No current goes in, virtual open circuit (虚断)
- Zero output impedance
- Infinite open-loop gain, A
  - » Virtual short circuit between the inverting and non-inverting input ports (虚短)
- Infinite bandwidth
- Infinite common-mode rejection
  - » Common mode rejection ratio (CMRR)

Electrical Characteristics of a Real Op-Amp

7.3 Electrical Characteristics µA741C, µA741M

at specified virtual junction temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A[1]	µA741C			µA741M			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0	25°C		1	6		1	5	mV
			Full range			7.5		±15	6	
$\Delta V_{IO(adj)}$	Offset voltage adjust range	V_O = 0	25°C		±15			20	200	mV
I_{IO}	Input offset current	V_O = 0	25°C		20	200			500	nA
			Full range			300			500	
I_{IB}	Input bias current	V_O = 0	25°C		80	500		80	500	nA
			Full range			800			1500	
V_{ICR}	Common-mode input voltage range		25°C	±12	±13		±12	±13		V
			Full range	±12			±12			
V_{OM}	Maximum peak output voltage swing	R_L = 10 kΩ	25°C	±12	±14		±12	±14		V
		R_L ≥ 10 kΩ	Full range	±12			±12			
		R_L = 2 kΩ	25°C	±10			±10	±13		
		R_L ≥ 2kΩ	Full range	±10			±10			
A_{VD}	Large-signal differential voltage amplification	R_L ≥ 2kΩ	25°C	20	200		50	200		V/mV
		V_O = ±10 V	Full range	15			25			
r_i	Input resistance		25°C	0.3	2		0.3	2		MΩ
r_o	Output resistance	V_O = 0, See[2]	25°C		75			75		Ω
C_i	Input capacitance		25°C		1.4			1.4		pF
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICRmin}	25°C	70	90		70	90		dB
			Full range	70			70			
k_{SVS}	Supply voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC}$)	V_{CC} = ±9 V to ±15 V	25°C		30	150		30	150	µV/V
			Full range			150			150	
I_{OS}	Short-circuit output current		25°C		±25	±40		±25	±40	mA
I_{CC}	Supply current	V_O = 0, No load	25°C		1.7	2.8		1.7	2.8	mA
			Full range			3.3			3.3	
P_D	Total power dissipation	V_O = 0, No load	25°C		50	85		50	85	mW
			Full range			100			100	

Switching Characteristics of a Real Op-Amp

over operating free-air temperature range, $V_{CC\pm}$ = ±15 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	µA741C			µA741M			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_r	Rise time	V_I = 20 mV, R_L = 2 kΩ, C_L = 100 pF, See Figure 1		0.3			0.3		µs
	Overshoot factor			5%			5%		—
SR	Slew rate at unity gain	V_I = 10 V, R_L = 2 kΩ, C_L = 100 pF, See Figure 1		0.5			0.5		V/µs

Imperfections in Practical Op-Amps

- Finite open-loop gain ($A_o < \infty$)
- Finite input resistance ($R_i < \infty$)
- Non-zero output resistance ($R_o > 0$)
- Finite bandwidth
- Offset (偏移) voltage
- Input bias and offset currents

Offset (偏移) Voltage

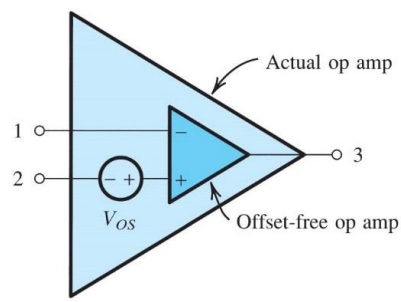

Figure 2.28 Circuit model for an op amp with input offset voltage V_{OS}.

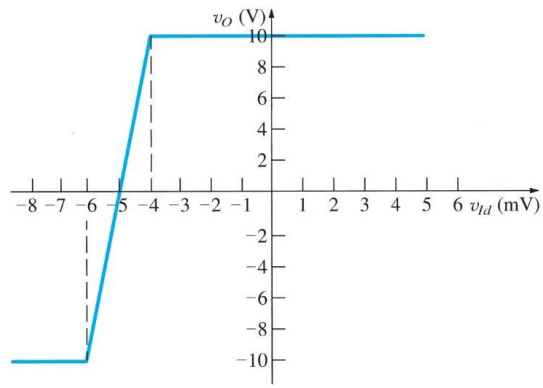

Figure E2.21 Transfer characteristic of an op amp with V_{OS} = 5 mV.

Trimming of Offset Voltage

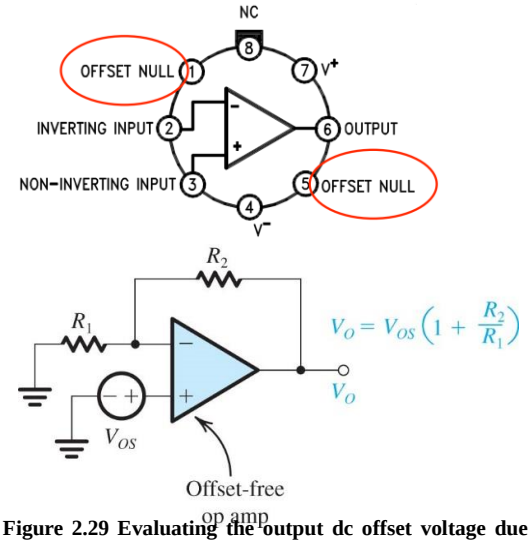

Figure 2.29 Evaluating the output dc offset voltage due to V_{OS} in a closed-loop amplifier.

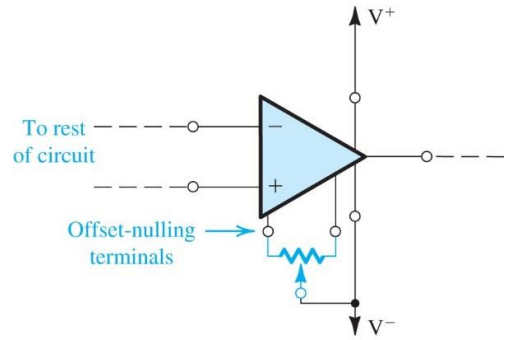

Figure 2.30 The output dc offset voltage of an op amp can be trimmed to zero by connecting a potentiometer to the two offset-nulling terminals. The wiper of the potentiometer is connected to the negative supply of the op amp.

Input Bias Currents and Offset Currents

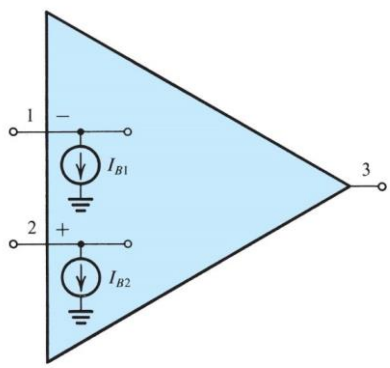

Figure 2.32 The op-amp input bias currents represented by two current sources I_{B1} and I_{B2}.

- The input terminals need to be supplied with bias currents, I_{B1} and I_{B2}, for Op Amp to function. (This will become clear towards the end of the semester).
- Input bias current: $I_B = (I_{B1} + I_{B2})/2$
- Input offset current: $I_{OS} = |I_{B1} - I_{B2}|$
- Typical bipolar transistor Op amps:
  - » I_B ~ 100 nA
  - » I_{OS} ~ 10 nA

Effect of Input Bias Current in Amplifier Circuit

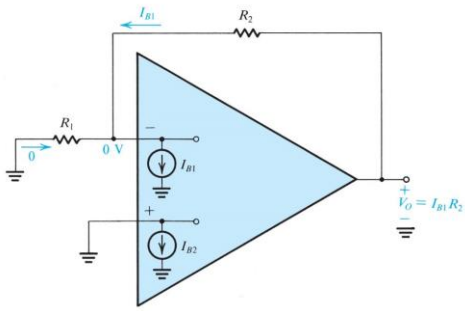

Figure 2.33 Analysis of the closed-loop amplifier, taking into account the input bias currents.

- In the absence of input voltage, the output should be zero for ideal Op Amp. However, with non-zero I_B,
- $V_O = I_{B1}R_2 \approx I_B R_2$

Reducing the Effect of Input Bias Currents

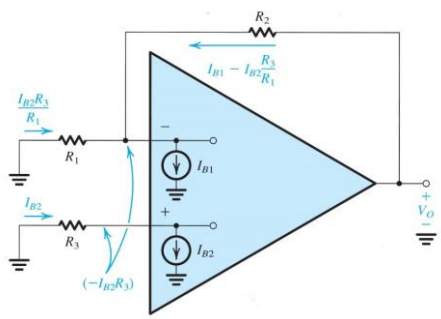

Figure 2.34 Reducing the effect of the input bias currents by introducing a resistor R_3.

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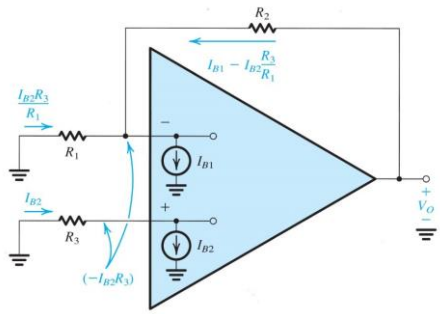


Figure 2.34 Reducing the effect of the input bias currents by introducing a resistor R_3.

Frequency Response of Open-Loop Op Amp

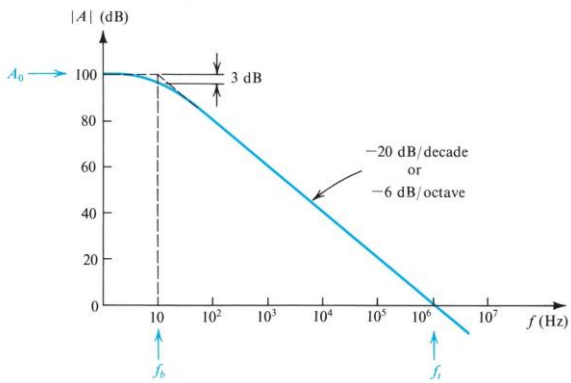
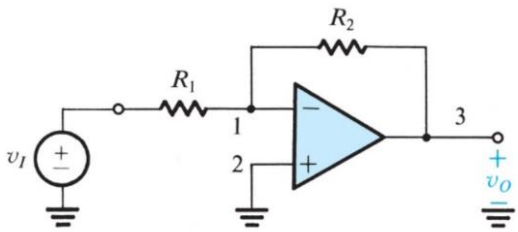


Figure 2.39 Open-loop gain of a typical general-purpose, internally compensated op amp.

Single pole response with a dominant pole at ω_b

Frequency Response of Closed-Loop Op Amp (Inverting Amplifier Example)



- Steps to find frequency response of closed-loop amp

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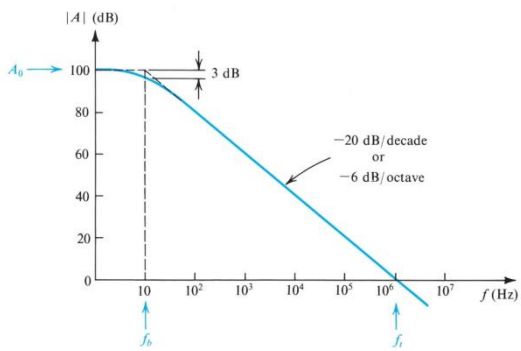

Frequency Response of Closed-Loop (Noninverting Amplifier Example)

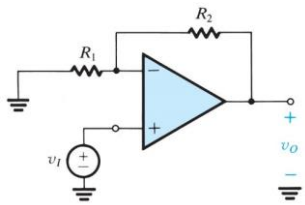

Figure 2.12 The noninverting configuration.

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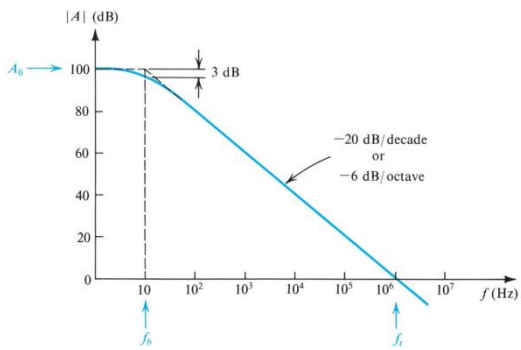


Output Saturation

- The output voltage swing is limited by
  - » 1. Saturation voltage (usually a volt or two lower than power supply voltage)
  - » 2. Maximum output current (in case of small load resistance)
- Output waveform appears to be “clipped” when either condition happens

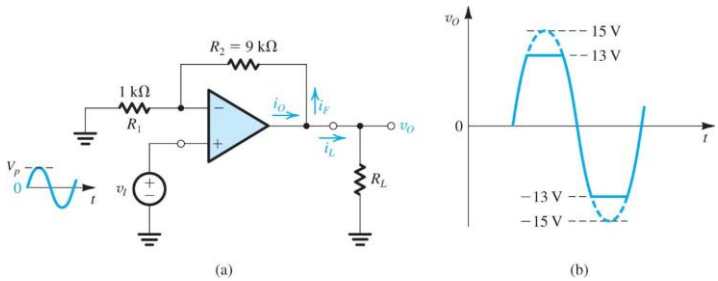


Figure 2.42 (a) A noninverting amplifier with a nominal gain of 10 V/V designed using an op amp that saturates at ±13-V output voltage and has ±20-mA output current limits. **(b)** When the input sine wave has a peak of 1.5 V, the output is clipped off at ±13 V.

Slew Rate (压摆率)

- Amplifier output is limited by "slew rate": maximum rate of change possible at output

$$SR = \left.\frac{dv_o}{dt}\right|_{max}$$

- SR is specified in datasheet in V/μs.

- Note: SR limit is different from bandwidth limit:
  - » Limited bandwidth is a linear phenomenon, it does not result in a change the shape of an input sinusoid
  - » SR limitation can cause nonlinear distortion to input sinusoidal signal

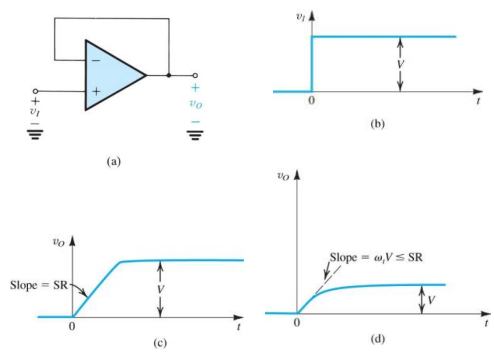
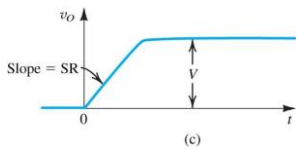


Figure 2.43 (a) Unity-gain follower. **(b)** Input step waveform. **(c)** Linearly rising output waveform obtained when the amplifier is slew-rate limited. **(d)** Exponentially rising output waveform obtained when V is sufficiently small so that the initial slope ($\omega_t V$) is smaller than or equal to SR.

Comparison of Slew Rate and Bandwidth Limits

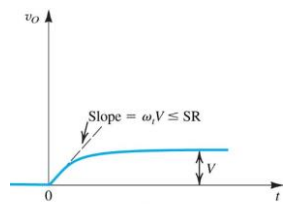
- For step function input waveform, both SR and bandwidth limits cause the output to rise with a finite slope, but there is an important difference:



(c)

Slew rate limited output:

Slope = SR



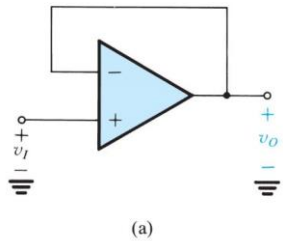
(d)

Bandwidth limited output:

Slope = $\omega_t V$ < SR

(V is the steady state output voltage)

Full-Power Bandwidth



(a)

Figure 2.43 (a) Unity-gain follower.

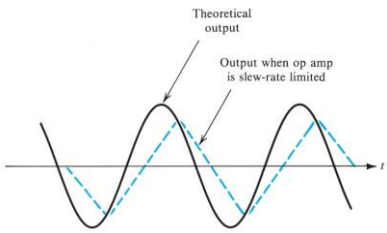


Figure 2.44 Effect of slew-rate limiting on output sinusoidal waveforms.

- For sinusoidal input to unity-gain follower:

$$v_I = V_i \sin \omega t$$

- Rate of change:

$$\frac{dv_I}{dt} = V_i \omega \cos \omega t \leq SR$$

- **Full-power bandwidth**:

  The frequency at which SR-limited distortion starts to occur for an output sinusoid with maximum rated output voltage, V_{omax},

$$\omega_M V_{omax} = SR$$

$$f_M = \frac{SR}{2\pi V_{omax}}$$

Summary

- Open loop gain
- Input impedance
- Output impedance
- Input offset & Bias
- CMRR
- Saturation
- Unity-gain bandwidth
- Slew rate
- Full-power bandwidth