EE112 - Fall 2016
Analog Integrated Circuits I

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MOSFET

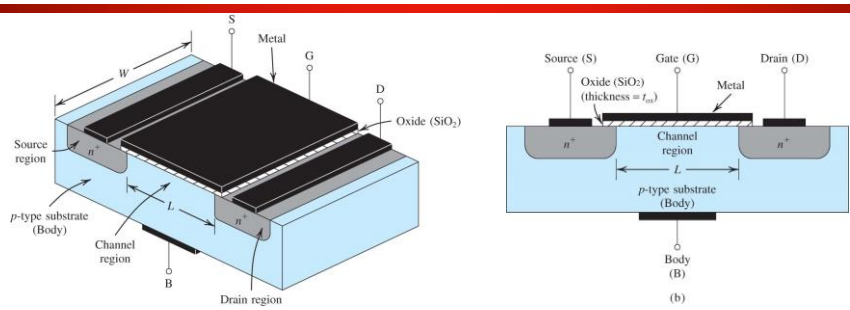

Figure 5.1 Physical structure of the enhancement-type NMOS transistor: **(a)** perspective view; **(b)** cross section. Typically L = 0.03 µm to 1 µm, W = 0.05 µm to 100 µm, and the thickness of the oxide layer (t_{ox}) is in the range of 1 to 10 nm.

- MOSFET: metal-oxide-semiconductor field effect transistor
- Typically
  - » Channel length: L ~ 10 nm to 0.35 µm
  - » Channel width: W ~ 0.05 µm to 100 µm
  - » Oxide thickness: t_{ox} ~ 1 to 10 nm

NMOSFET (NMOS)

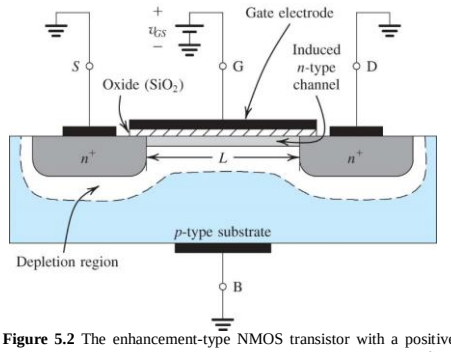

Figure 5.2 The enhancement-type NMOS transistor with a positive voltage applied to the gate. An *n* channel is induced at the top of the substrate beneath the gate.

- **N-channel (n-沟道)** MOSFET
  - » Current conducted by e^-s
- 3 terminal device
  - » **Source (S, 源)**: n+ (heavily n-type)
  - » **Drain (D, 漏)**: n+
  - » **Gate (G, 栅)**; metal deposited on insulator above channel
- **Substrate (Body, 衬底, 体)** is a 4th terminal
  - » Substrate is p-doped
- Electrons are induced in channel when a positive gate voltage is applied
- Electrons moves from Source to Drain
  - » Current flows from D to S

Creating a "Channel (沟道)" for Current Flow

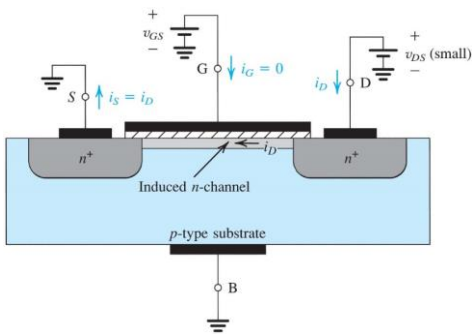

Figure 5.3 An NMOS transistor with $v_{GS} > V_t$ and with a small v_{DS} applied. The device acts as a resistance whose value is determined by v_{GS}. Specifically, the channel conductance is proportional to $v_{GS} - V_t$, and thus i_D is proportional to $(v_{GS} - V_t)v_{DS}$. Note that the depletion region is not shown.

- MOS is a capacitor across an insulator (oxide) When a positive voltage is applied at Gate, electrons are induced under the gate.
- At "**threshold (阈值)**", sufficient number of electrons form a "channel" between Source and Drain, forming a conductive channel.
- Total charge in the channel:

  $$|Q| = C_{ox} \cdot WL \cdot (v_{GS} - V_t)$$

  where $C_{ox} = \varepsilon_{ox}/t_{ox}$ is oxide capacitance per unit area
  - » $\varepsilon_{ox} = 3.9\varepsilon_0 = 3.9 \times 8.854 \times 10^{-12}$ F/m
  - » W : gate width
  - » L : gate length
  - » V_t: Threshold voltage
  - » $v_{GS} - V_t \equiv v_{OV}$ is called "**Overdrive Voltage(过驱动电压)**"

Current at Small v_{DS}

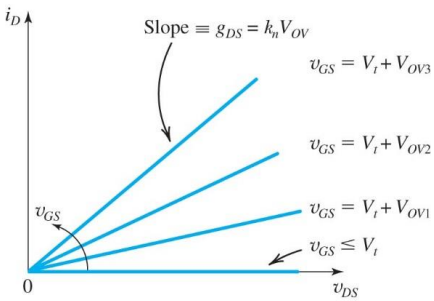

Figure 5.4 The i_D - v_{DS} characteristics of the MOSFET in Fig. 5.3 when the voltage applied between drain and source, v_{DS}, is kept small. The device operates as a linear resistance whose value is controlled by v_{GS}.

- When $v_{OV} = v_{GS} - V_t > 0$, a channel is formed between Source and Drain.
- Linear charge density in channel:
- Electric field along the channel
- Drain current = charge density × velocity:
- At small v_{DS}, the transistor is like a gate-controlled variable resistor

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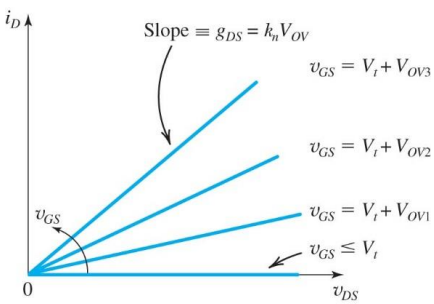

Figure 5.4 The i_D - v_{DS} characteristics of the MOSFET in Fig. 5.3 when the voltage applied between drain and source, v_{DS}, is kept small. The device operates as a linear resistance whose value is controlled by v_{GS}.

Triode Region ($v_{DS} < v_{OV}$)

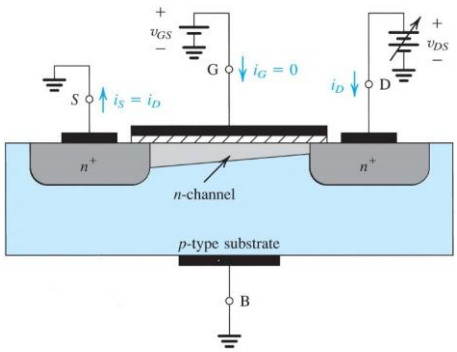

Figure 5.5 Operation of the enhancement NMOS transistor as v_{DS} is increased. The induced channel acquires a tapered shape, and its resistance increases as v_{DS} is increased. Here, v_{GS} is kept constant at a value > V_t; $v_{GS} = V_t + V_{OV}$.

- As v_{DS} increases, the potential in the channel is no longer a constant. Assume the channel is $v(x)$:

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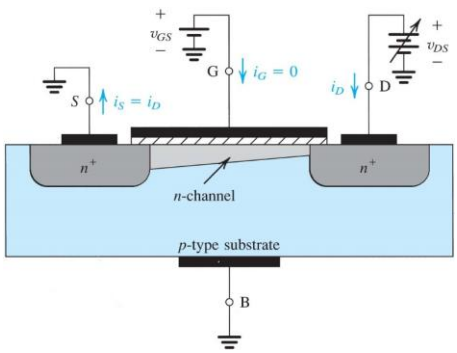

Figure 5.5 Operation of the enhancement NMOS transistor as v_{DS} is increased. The induced channel acquires a tapered shape, and its resistance increases as v_{DS} is increased. Here, v_{GS} is kept constant at a value > V_t; $v_{GS} = V_t + V_{OV}$.

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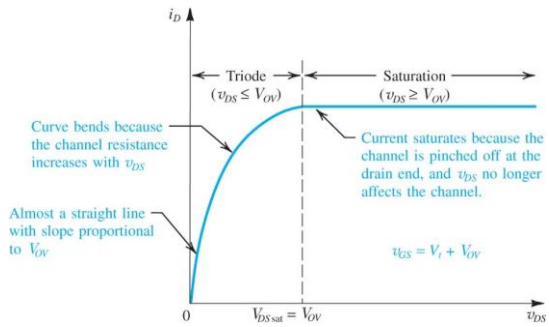


Figure 5.7 The drain current i_D versus the drain-to-source voltage v_{DS} for an enhancement-type NMOS transistor operated with $v_{GS} = V_t + V_{OV}$

Pinch-Off (夹断)

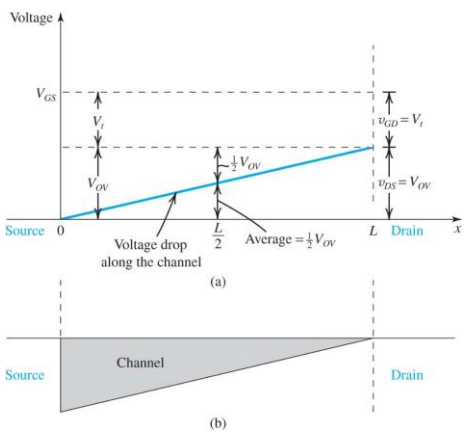


Figure 5.8

The channel potential at the drain side is v_{DS}. When $v_{DS} = v_{OV}$, the local charge density there

So the channel is "pinched off" near the Drain. Once the channel is pinched off, the drain current remains constant:

This region, $v_{DS} > v_{OV}$, is called “Saturation (饱和)"

Saturation Region ($v_{DS} > v_{OV}$)

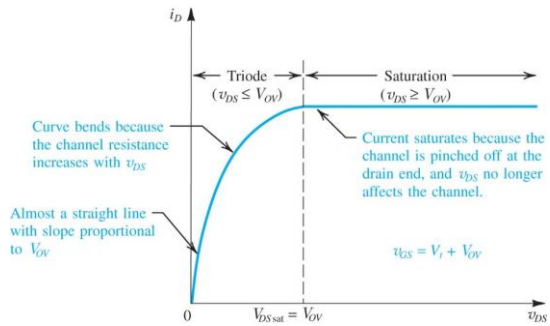
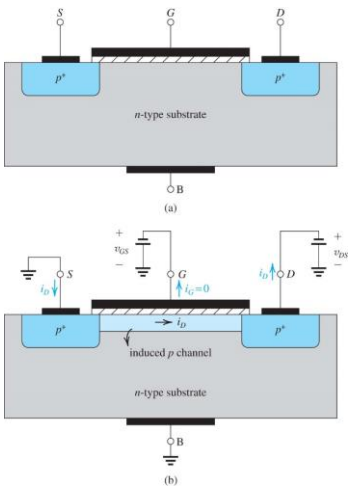


Figure 5.7 The drain current i_D versus the drain-to-source voltage v_{DS} for an enhancement-type NMOS transistor operated with $v_{GS} = V_t + V_{OV}$

PMOSFET (PMOS)



- P-channel MOSFET
  - » Current conducted by holes
- 3 terminal device
  - » Source (S): p+ (heavily p-type)
  - » Drain (D): p+
  - » Gate (G): metal deposited on insulator above channel
- Substrate (called “Body”) is a 4th terminal
  - » Substrate is n-doped
- Holes is induced in channel when a negative gate voltage is applied
- Holes moves from Source to Drain
  - » Current flows from S to D

CMOS (Complementary MOS)

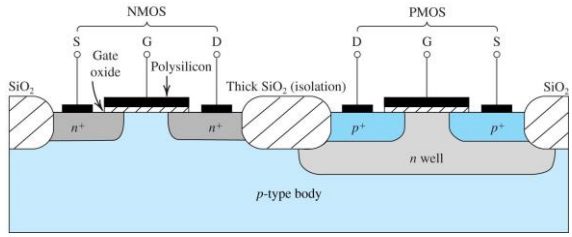


Figure 5.10 Cross section of a CMOS integrated circuit. Note that the PMOS transistor is formed in a separate *n*-type region, known as an *n* well. Another arrangement is also possible in which an *n*-type substrate (body) is used and the *n* device is formed in a *p* well. Not shown are the connections made to the *p*-type body and to the *n* well; the latter functions as the body terminal for the *p*-channel device.

- CMOS is the prevalent IC technology today
- Since NMOS and PMOS are formed on oppositely doped substrates, one of the transistor needs to be placed in a "**well(阱)**"
- PMOS is placed in an "**n well(n阱)**" here.
- Alternatively, NMOS can be placed in p well

Circuit Symbol for NMOS

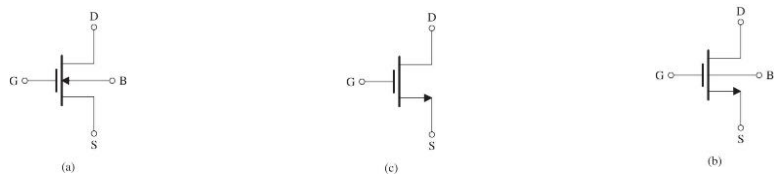
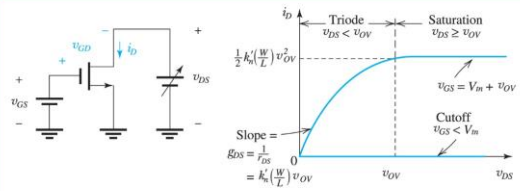


Figure 5.11 (a) Circuit symbol for the *n*-channel enhancement-type MOSFET. **(b)** Modified circuit symbol with an arrowhead on the source terminal to distinguish it from the drain and to indicate device polarity (i.e., *n* channel). **(c)** Simplified circuit symbol to be used when the source is connected to the body or when the effect of the body on device operation is unimportant.

- 4 terminal including Body (Arrow pointing to channel indicating substrate is p-type
- Modified circuit symbol with arrow on source (Arrow indicating direction of current flow)
- Simplified circuit symbol with body connected to source (or when the effect of the body on device operation is unimportant)

Summary

Table 5.1 Regions of Operation of the Enhancement NMOS Transistor



- $v_{GS} < V_{tn}$: no channel; transistor in cutoff; $i_D = 0$
- $v_{GS} = V_{tn} + v_{OV}$: a channel is induced; transistor operates in the triode region or the saturation region depending on whether the channel is continuous or pinched off at the drain end;

Triode Region	*Saturation Region*
Continuous channel, obtained by: $v_{GD} > V_{tn}$	Pinched-off channel, obtained by: $v_{GD} \leq V_{tn}$
or equivalently: $v_{DS} < v_{OV}$	or equivalently: $v_{DS} \geq v_{OV}$
Then, $i_D = k_n'\left(\frac{W}{L}\right)\left[(v_{GS} - V_{tn})v_{DS} - \frac{1}{2}v_{DS}^2\right]$	Then $i_D = \frac{1}{2}k_n'\left(\frac{W}{L}\right)(v_{GS} - V_{tn})^2$
or equivalently, $i_D = k_n'\left(\frac{W}{L}\right)\left(v_{OV} - \frac{1}{2}v_{DS}\right)v_{DS}$	or equivalently, $i_D = \frac{1}{2}k_n'\left(\frac{W}{L}\right)v_{OV}^2$