EE112 - Fall 2016
Analog Integrated Circuits I

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Circuit Symbol for NMOS

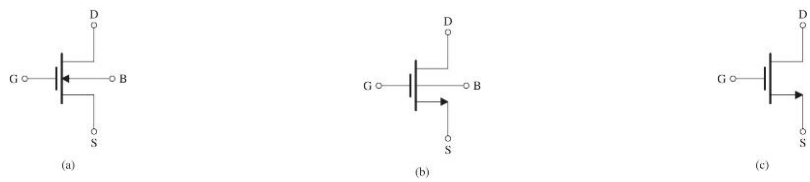


Figure 5.11 (a) Circuit symbol for the *n*-channel enhancement-type MOSFET. **(b)** Modified circuit symbol with an arrowhead on the source terminal to distinguish it from the drain and to indicate device polarity (i.e., *n* channel). **(c)** Simplified circuit symbol to be used when the source is connected to the body or when the effect of the body on device operation is unimportant.

- 4 terminal including Body (Arrow pointing **to** channel indicating substrate is **p-type**
- Modified circuit symbol with arrow on source (Arrow indicating direction of current flow)
- Simplified circuit symbol with body connected to source (or when the effect of the body on device operation is unimportant)

- Note in NMOS
  - **Drain voltage is always more positive than source voltage**
  - **Current always flows from Drain to Source**

I-V Curves of NMOS

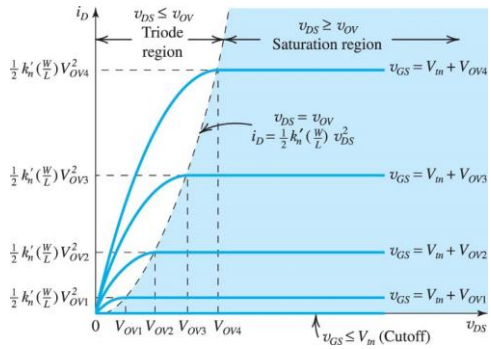


Figure 5.13 The i_D - v_{DS} characteristic for an enhancement-type NMOS transistor.

Relative Voltage Levels of NMOS

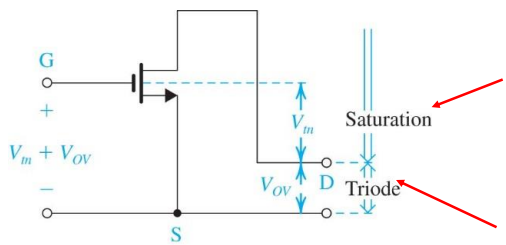


Figure 5.12 The relative levels of the terminal voltages of the enhancement NMOS transistor for operation in the triode region and in the saturation region.

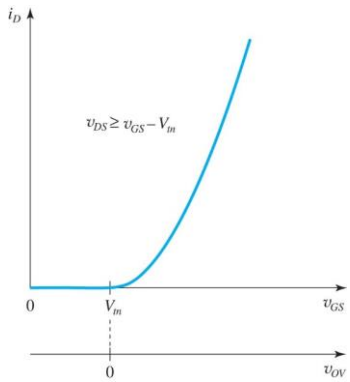
Analog Circuit (e.g., linear amplifiers) usually biased in Saturation region

Digital circuit (e.g. inverter) and power electronics (switch mode power supply) use Triode region as one of the states

V_{tn}: threshold voltage of NMOS

V_{tn} is usually fixed once a **process (technology, 工艺)** is selected

Drain Current vs Gate Voltage



- In Saturation Region

- To experimentally determine V_{tn}:

Figure 5.14 The i_D-v_{GS} characteristic of an NMOS transistor operating in the saturation region. The i_D-v_{OV} characteristic can be obtained by simply relabeling the horizontal axis, that is, shifting the origin to the point $v_{GS} = V_{tn}$.

Finite Output Resistance due to Channel length Modulation (沟长调制)

- When $v_{DS} = v_{OV}$

- When $v_{DS} > v_{OV}$

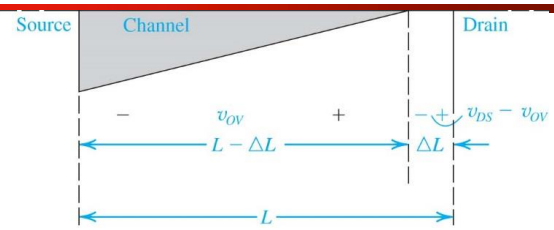


Figure 5.16 Increasing v_{DS} beyond v_{DSsat} causes the channel pinch-off point to move slightly away from the drain, thus reducing the effective channel length (by ΔL)

Output Resistance of MOSFET

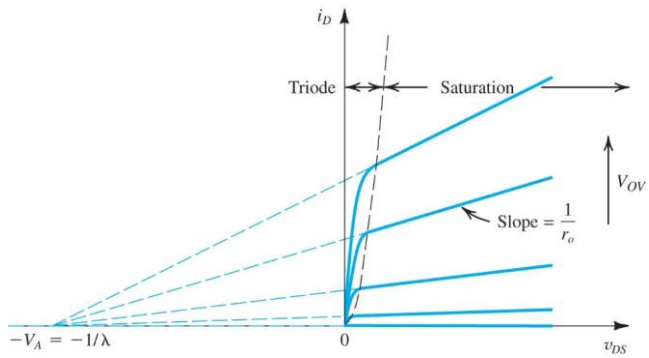


Figure 5.17 Effect of v_{DS} on i_D in the saturation region. The MOSFET parameter V_A depends on the process technology and, for a given process, is proportional to the channel length L.

Circuit Symbol of PMOS

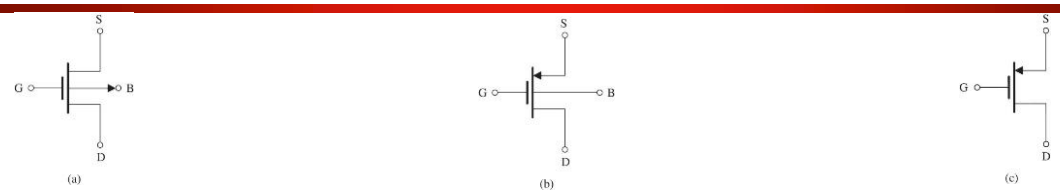
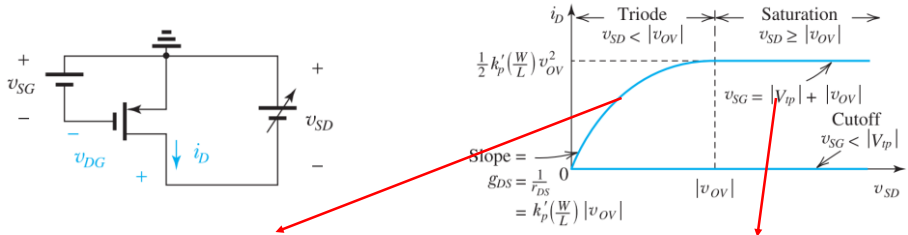


Figure 5.19 (a) Circuit symbol for the *p*-channel enhancement-type MOSFET. **(b)** Modified symbol with an arrowhead on the source lead. **(c)** Simplified circuit symbol for the case where the source is connected to the body.

- 4 terminal including Body (Arrow pointing **from** channel indicating substrate is **n-type**
- Modified circuit symbol with arrow on source (Arrow indicating direction of current flow)
- Simplified circuit symbol with body connected to source (or when the effect of the body on device operation is unimportant)

- Note in PMOS
  - » **Source voltage is always more positive than Drain voltage**
  - » **Current always flows from Source to Drain**
  - » **Source is usually drawn on top so current flows downward (convention)**

PMOS I-V Equations



- Triode Region
- Saturation Region

Relative Voltage Levels of PMOS

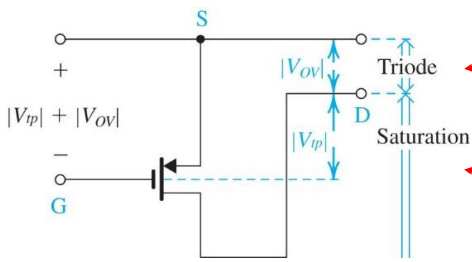


Figure 5.20 The relative levels of the terminal voltages of the enhancement-type PMOS transistor for operation in the triode region and in the saturation region.

Digital circuit (e.g. inverter) and power electronics (switch mode power supply) use Triode region as one of the states

Analog Circuit (e.g., linear amplifiers) usually biased in Saturation region

V_{tp}: threshold voltage of NMOS

V_{tp} is usually fixed once a **process (technology, 工艺)** is selected

Diode-Connected Transistor

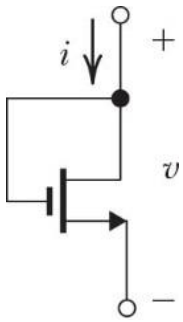


Figure 5.22

- With Gate connected to Drain, it becomes a 2-terminal device.
- This is called diode-connected transistor
- In this configuration, the transistor is always in Saturation.

Example Circuit (1)

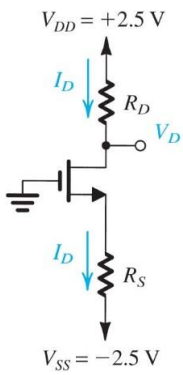


Figure 5.21 Circuit for Example 5.3.

- Design problem:

Determine R_S and R_D such that the NMOS is biased at I_D = 0.4mA and V_D = 0.5V. The NMOS has V_t = 0.7V, $\mu_n C_{ox}$ =100 $\mu A/V^2$, L =1 μm and W = 32 μm.

Example Circuit (2)

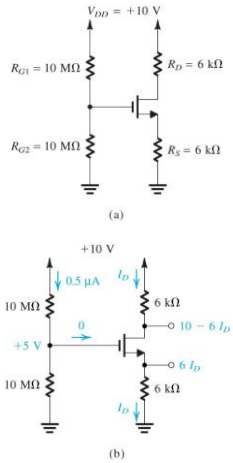


Figure 5.24 (a) Circuit for Example 5.6. **(b)** The circuit with some of the analysis details shown.

- DC operating point:

Analyze the circuit to determine the voltages at all notes and the currents through all branches. Let V_{tn} = 1 V and k_n' (W/L) = 1 mA/V^2. Neglect the channel length modulation effect.

Continued

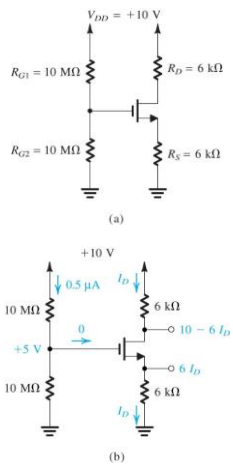


Figure 5.24 (a) Circuit for Example 5.6. **(b)** The circuit with some of the analysis details shown.

Example Circuit (3)

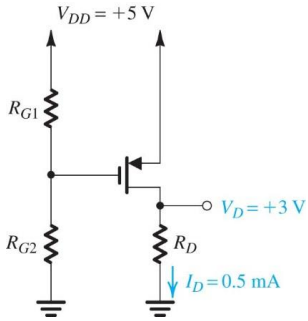


Figure 5.25 Circuit for Example 5.7.

- Design Problem

Design the circuit such that I_D = 0.5 *mA* and V_D = 3 V. PMOS has V_{tp} = −1V, $\mu_p C_{ox}(W/L)$ = 1mA/V^2. Also find the maximum R_D for PMOS to remain in Saturation.