EE112 - Fall 2016
Analog Integrated Circuits I

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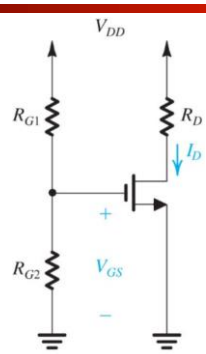
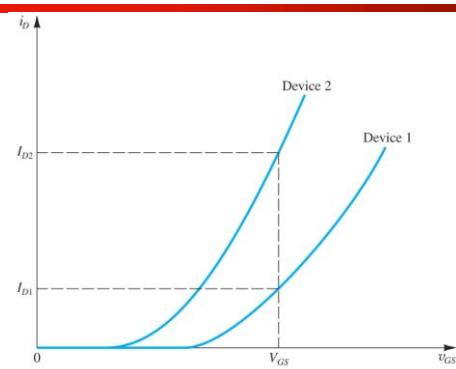
Purposes of Bias Circuit

- Provide a stable bias drain (collector) current
- Bias insensitive to variations in
  - » Transistor parameters (β for BJT, V_t, k for MOS),
  - » Temperature and other environmental changes
- Keep transistors in flat part of the I-V curves (Saturation for MOS, Active for BJT) for desired output swing

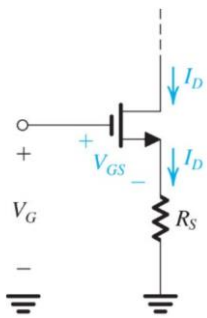
Example of Non-Ideal Bias

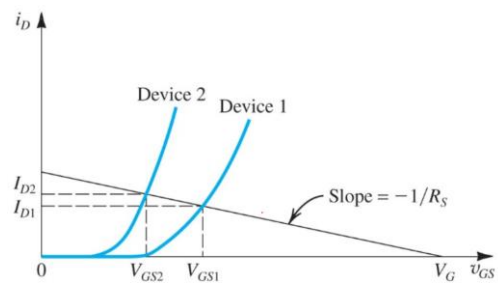




- Fixed v_{GS} from voltage divider
- Large variation in i_D due to device variations
- Large temperature dependence
  - » μ_n and V_t are temperature sensitive

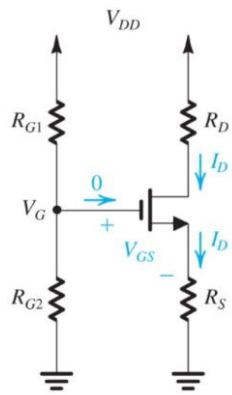
Adding Source Resistance R_s



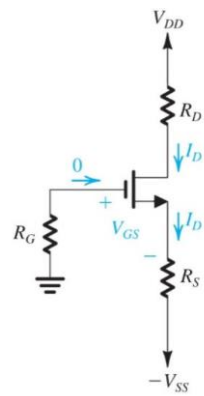


- R_S provides a negative feedback
  - » If I_D increases, V_{GS} decreases -> reduce I_D
  - » If I_D decreases, V_{GS} increases -> increase I_D
- Stabilize I_D w.r.t. device and temperature variations

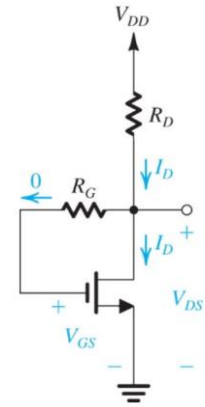
Practical Implementations



Single Power Supply

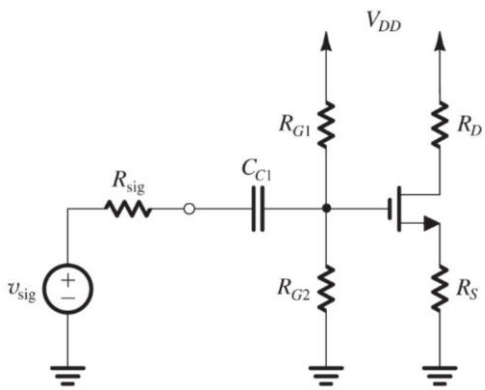


Dual Power Supply



Drain-to-Gate Feedback

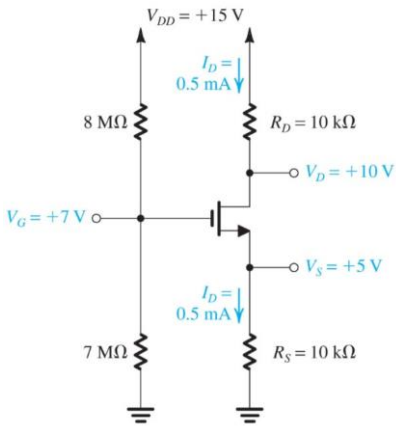
Coupling Capacitor to Separate AC Signal from DC Bias



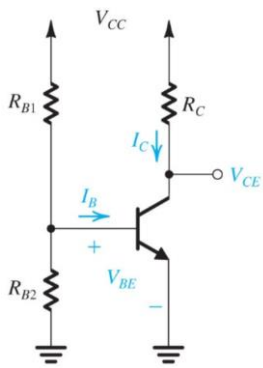
- Coupling capacitor is DC-open and AC-short
- Prevent signal source to change bias condition
- The coupling capacitor creates a lower bound of operating frequency

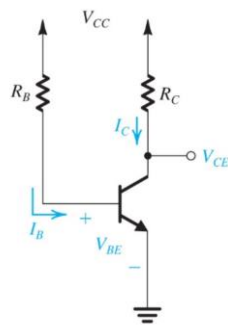
Bias Design Example

Goal: design bias for I_D = 0.5 mA.
MOS has V_t = 1V and k_n = 1 mA/V^2

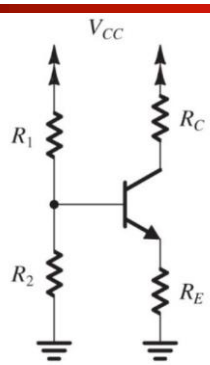


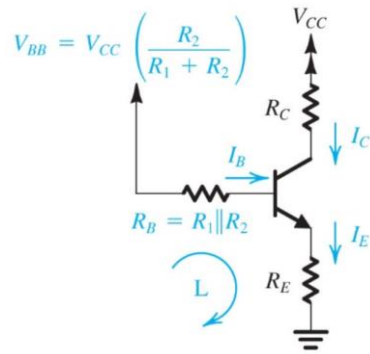
Non-Ideal Biasing Schemes for BJT





Good (Stable) Biasing Circuits for BJT





- Similar to MOSFET bias, but must consider finite base current:
- First, find Thevenin equivalent circuit of bias circuit:

Design Example of BJT Bias

Goal: design bias circuit for I_E = 1 mA with V_{CC} = 12 V and β = 100