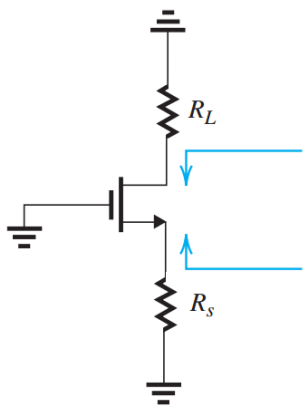
EE112 - Fall 2016
Analog Integrated Circuits I

Prof. Haoyu Wang
wanghy@shanghaitech.edu.cn
5210 Research Bldg.

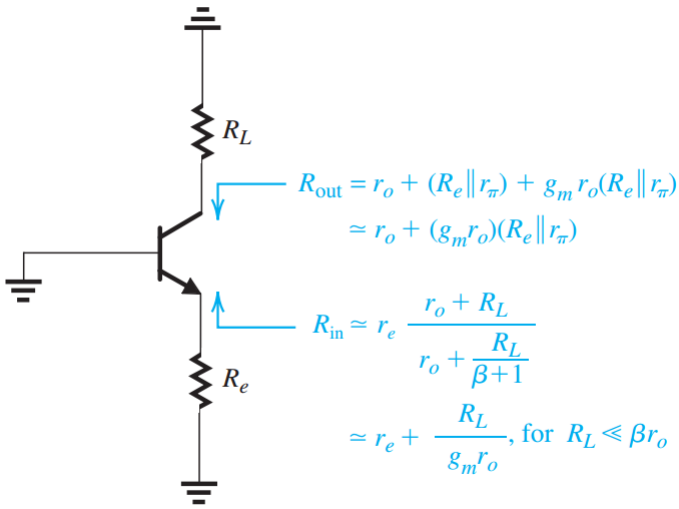
Impedance Transformation of Common Gate Amplifier



$$R_{out} = r_o + R_s + g_m r_o R_s$$
$$\simeq r_o + (g_m r_o) R_s$$

$$R_{in} = \frac{r_o + R_L}{1 + g_m r_o}$$
$$\simeq \frac{1}{g_m} + \frac{R_L}{g_m r_o}$$

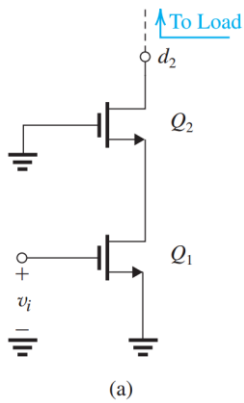
Impedance Transformation of Common Base Amplifier



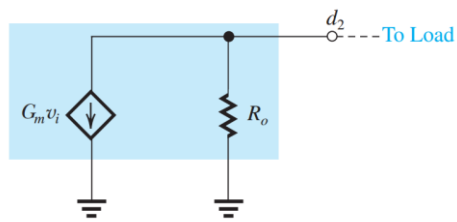
$$R_{\text{out}} = r_o + (R_e \| r_\pi) + g_m r_o (R_e \| r_\pi)$$
$$\simeq r_o + (g_m r_o)(R_e \| r_\pi)$$

$$R_{\text{in}} \simeq r_e \frac{r_o + R_L}{r_o + \frac{R_L}{\beta + 1}}$$
$$\simeq r_e + \frac{R_L}{g_m r_o}, \text{ for } R_L \ll \beta r_o$$

MOS Cascode

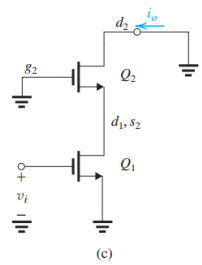


(a)

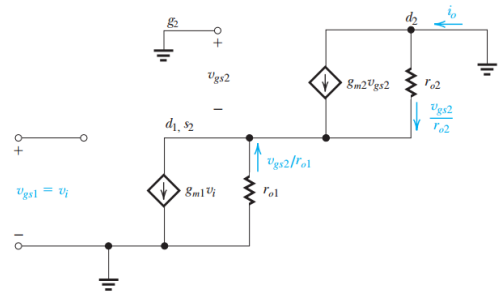


(b)

Continued/G_m

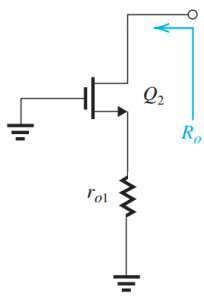


(c)

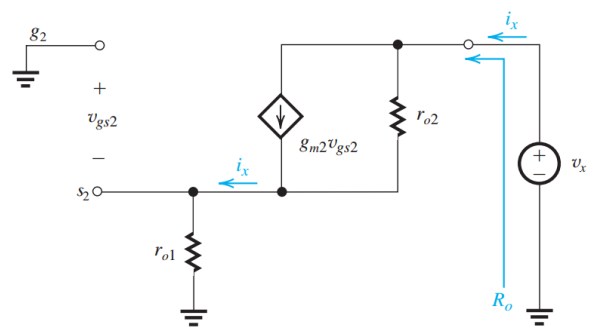


(d)

Continued/R_o

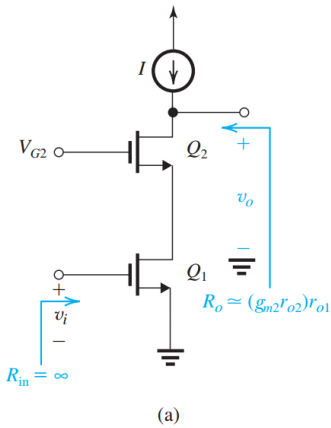


(a)

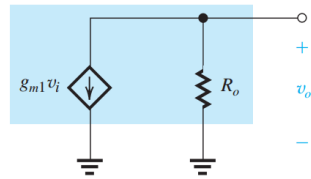


(b)

MOS Cascode Amplifier

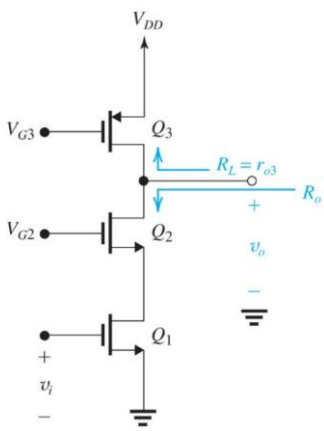


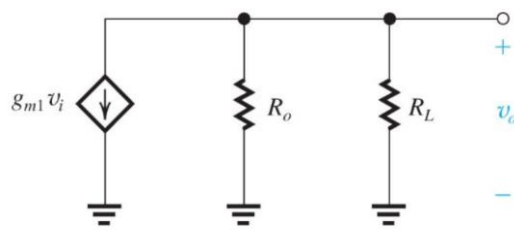
(a)



(b)

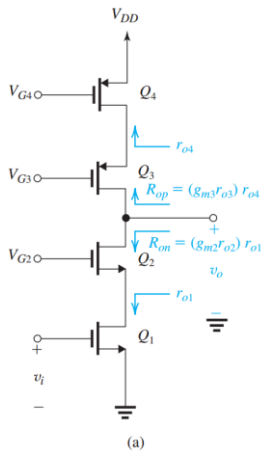
Cascode Amplifier with Simple Active Load



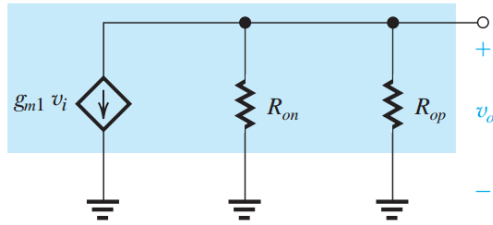


(b)

Cascode Amplifier with Cascode Current-Source Load

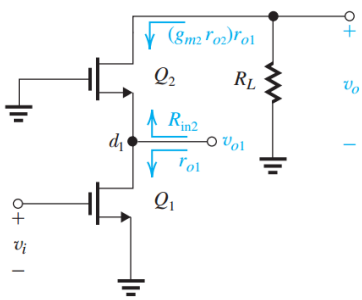


(a)

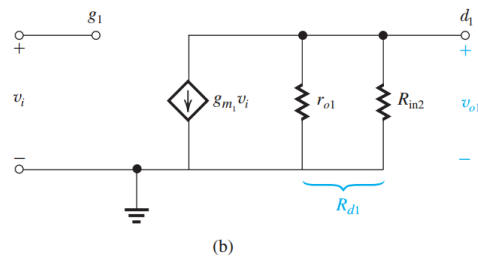


(b)

Think of Cascode as Multistage Amplifier with CS followed by CG

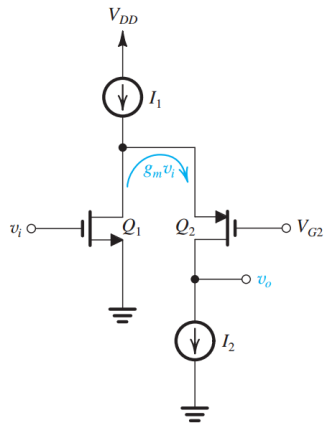


(a)



(b)

The Folded Cacode

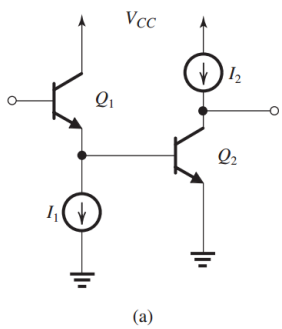


Folding the CG stage using PMOS

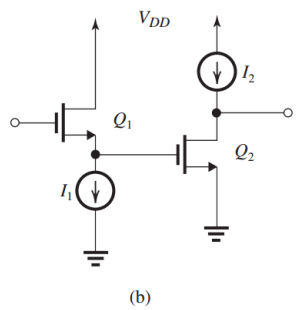
- Q_2 is biased with I_2
- Q_1 is biased with $I_1 - I_2$

Folded cascode avoids staking too many transistors vertically, which will be difficult for low V_{DD}

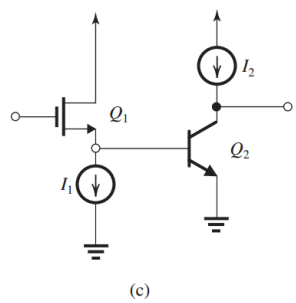
Useful Transistor Pairings



(a)



(b)



(c)

CC+CE

- High R_{in}
- Much wider bandwidth than single CE

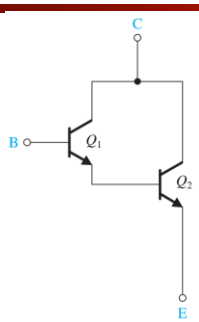
CD+CS

- Main benefit is wider bandwidth than single CS

CD+CE (BiCMOS)

- Similar to MOS version
- Higher g_m

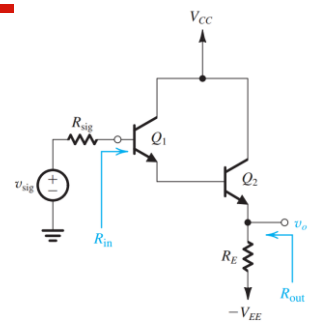
Darlington Pair



(a)

Darlington pair

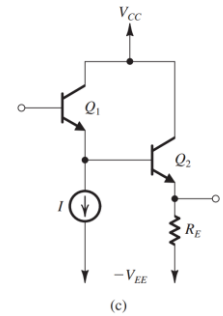
- Composite BJT with $\beta = \beta_1\beta_2$



(b)

CC+CC

high performance emitter follower



(c)

CC+CC

high performance emitter follower with separate current bias for Q_1 -> high β_1