EE112 - Fall 2016
Analog Integrated Circuits I

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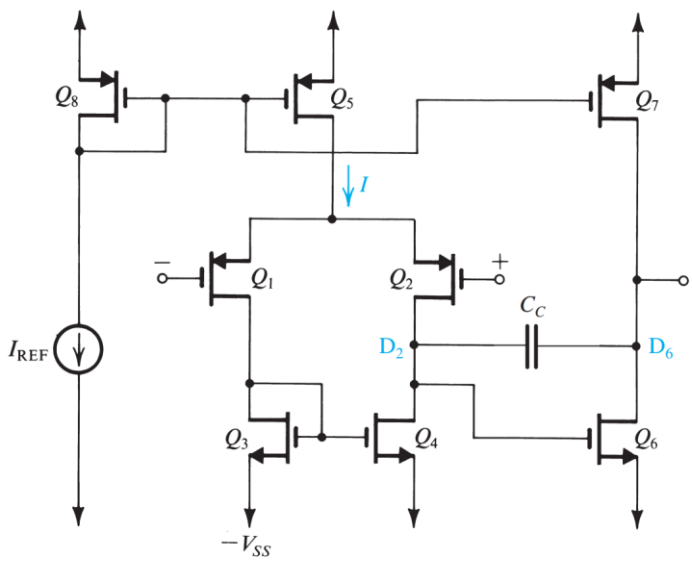
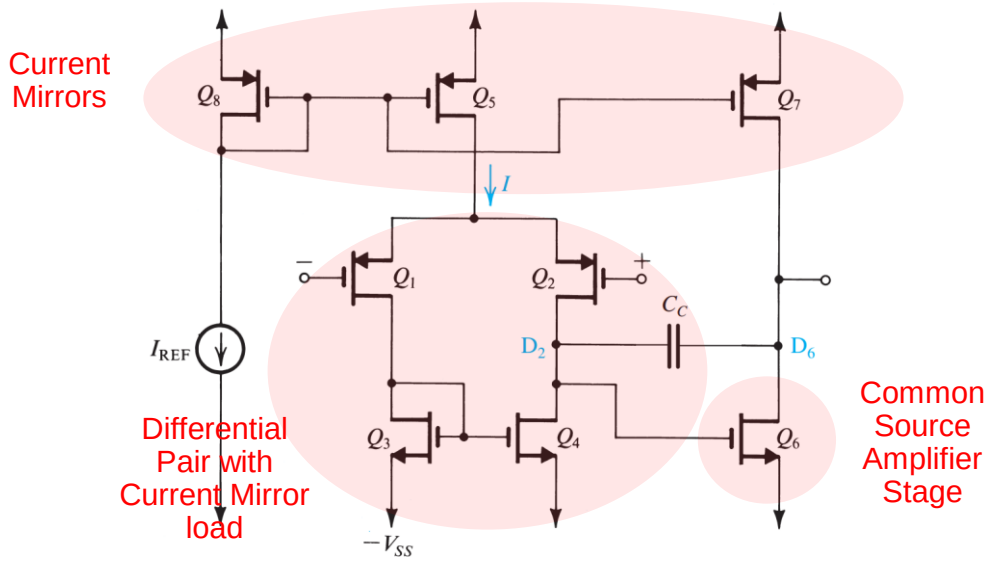
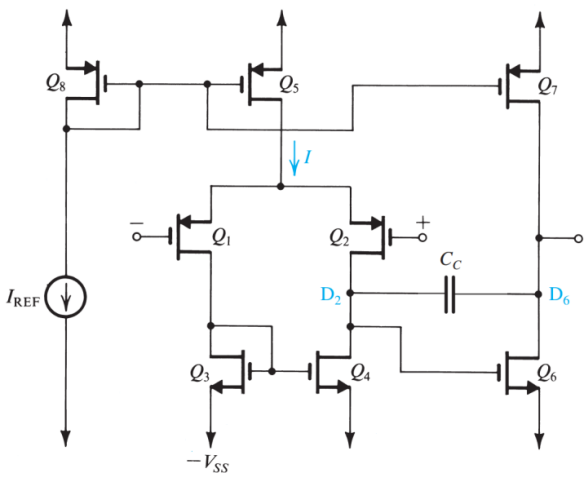
Two-Stage CMOS Op-Amp Circuit



Stages Scrutinize



Voltage Gains



- Voltage gain of the first stage (Q_1, Q_2): Differential input, single-ended output:

$$A_1 = -g_{m1}(r_{o2} \parallel r_{o4})$$

- Voltage gain of the 2nd stage (Q_6): Common source with current source load:

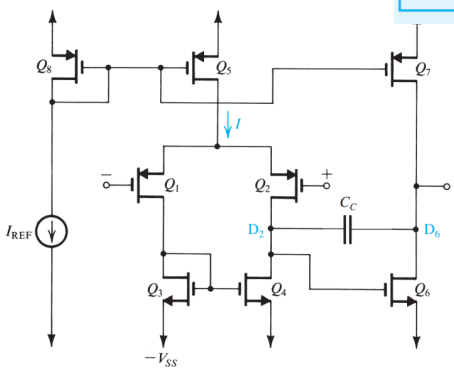
$$A_2 = -g_{m6}(r_{o6} \parallel r_{o7})$$

- Total gain

$$A_o = A_1 A_2$$

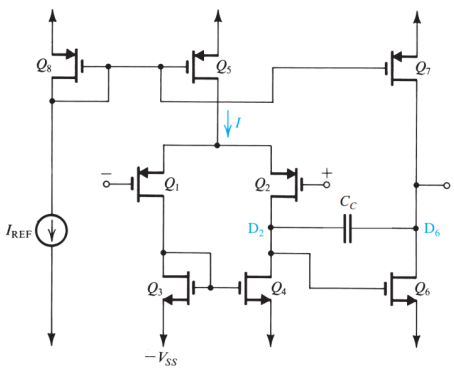
Example:

Transistor	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	Q_8
W/L	20/0.8	20/0.8	5/0.8	5/0.8	40/0.8	10/0.8	40/0.8	40/0.8

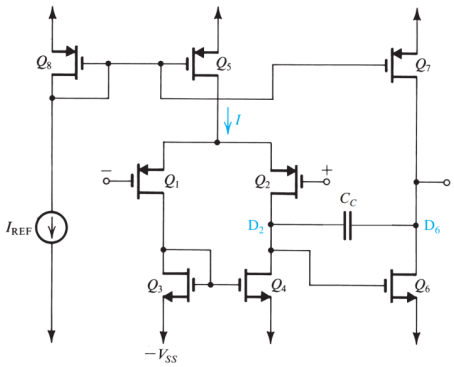


- I_{REF} = 90 μA, V_{tn} = 0.7 V, V_{tp} = -0.8 V, $\mu_n C_{ox}$ = 160 $\mu A/V^2$, $\mu_p C_{ox}$ = 40 $\mu A/V^2$, $|V_A|$ = 10 V for all devices $V_{DD} = V_{SS}$ = 2.5 V.
- Find I_D, $|V_{OV}|$, $|V_{GS}|$, g_m, r_o for all Q's, voltage gain, input common mode range, output voltage range.

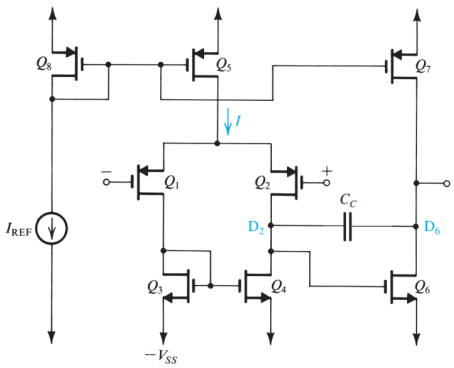
Solution: DC Parameters



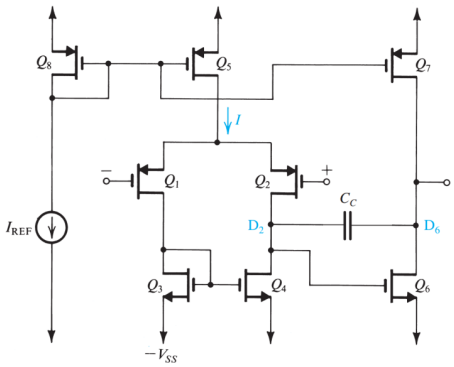
Solution: AC Parameters



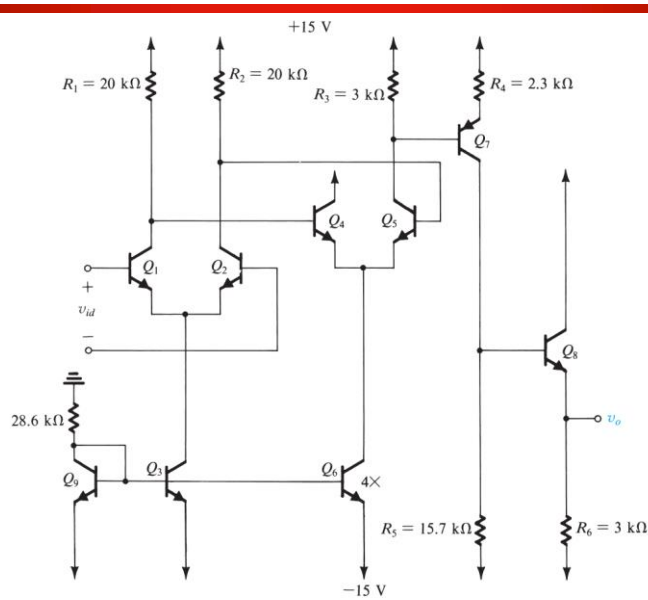
Solution: Input Common-Mode Ranges



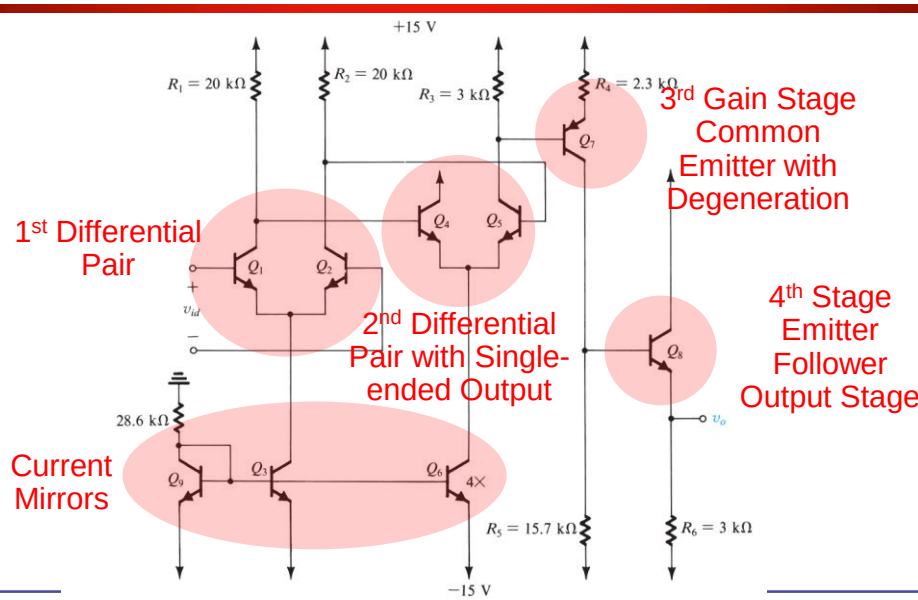
Solution: Output Ranges



A Four-Stage Bipolar Op-Amp



Stages Scrutinize



DC Solution