ShanghaiTech University
School of Information Science and Technology

EE112 Analog Integrated Circuits I

Homework 1

Due: Oct. 8th 2016 before lecture

Read the chapter 1.

1. An amplifier operating from ±3 V supplies provides a 2.2 V peak sine wave across a 100 Ω load when provided with a 0.2 V peak input from which 1.0 mA peak is drawn. The average current in each supply is measured to be 20 mA. Find the voltage gain, current gain, and power gain expressed as ratios and in decibels as well as the supply power, amplifier dissipation, and amplifier efficiency.

2. An amplifier with 40 dB of small-signal, open-circuit voltage gain, an input resistance of 1 MΩ, and an output resistance of 100 Ω, drives a load of 500 Ω. What voltage and power gains (expressed in dB) would you expect with the load connected? If the amplifier has a peak output-current limitation of 20 mA, what is the rms value of the largest sine-wave input for which an undistorted output is possible? What is the corresponding output power available?

3. You are given two amplifiers, A and B, to connect in cascade between a 10 mV, 100 kΩ source and a 100 Ω load. The amplifiers have voltage gain, input resistance, and output resistance as follows: for A, 100 V/V, 100 kΩ, 10 kΩ, respectively; for B, 10 V/V, 10 kΩ, 1 kΩ, respectively. Your problem is to decide how the amplifiers should be connected. To proceed, evaluate the two possible connections between source S and load L, namely, SABL and SBAL. Find the voltage gain for each both as a ratio and in decibels. Which amplifier arrangement is best?

4. A designer wishing to lower the overall upper 3 dB frequency of a three-stage amplifier to 10 kHz considers shunting one of two nodes: Node A, between the output of the first stage and the input of the second stage, and Node B, between the output of the second stage and the input of the third stage, to ground with a small capacitor. While measuring the overall frequency response of the amplifier, she connects a capacitor of 1 nF, first to node A and then to node B, lowering the 3 dB frequency from 3 MHz to 200 kHz and 20 kHz, respectively. If she knows that each amplifier stage has an input resistance of 100 kΩ, what output resistance must the driving stage have at node A? At node B? What capacitor value should she connect to which node to solve her design problem most economically?