ShanghaiTech University
School of Information Science and Technology

EE112 Analog Integrated Circuits I

Homework 6

Due: Nov 17th before lecture

Read the chapter 7.

1. Various measurements are made on an NMOS amplifier for which the drain resistor R_D is 20 kΩ. First, dc measurements show the voltage across the drain resistor, V_{RD}, to be 1.5 V and the gate-to-source bias voltage to be 0.7 V. Then, ac measurements with small signals show the voltage gain to be –10 V/V. What is the value of V_t for this transistor? If the process transconductance parameter k_n' is 200 μA/V^2, what is the MOSFET's W/L?

2. For the amplifier circuit in Fig. 1 with V_{CC} = + 5 V and R_C = 1 kΩ, find V_{CE} and the voltage gain at the following dc collector bias currents: 0.5 mA, 1 mA, 2.5 mA, 4 mA, and 4.5 mA. For each, give the maximum possible positive- and negative-output signal swing as determined by the need to keep the transistor in the active region. Present your results in a table.

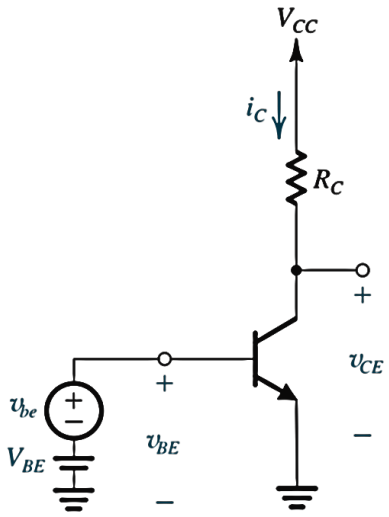

Figure 1

3. Consider the FET amplifier of Fig. 2 for the case V_t = 0.4 V, k_n = 5 mA/V^2, V_{GS} = 0.6 V, V_{DD} = 1.8 V, and R_D = 10 kΩ.
   (a) Find the dc quantities I_D and V_{DS}.
   (b) Calculate the value of g_m at the bias point.
   (c) Calculate the value of the voltage gain.
   (d) If the MOSFET has λ = 0.1 V^{-1}, find r_o at the bias point and calculate the voltage gain.

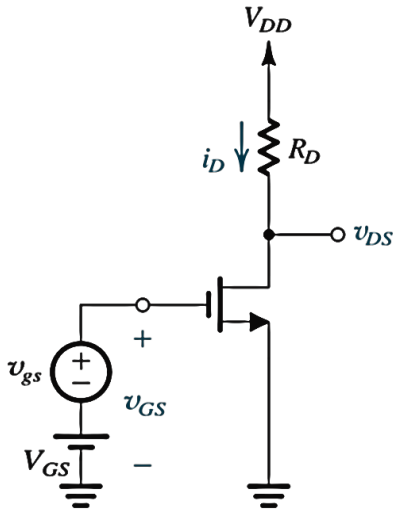

Figure 2

4. For the NMOS amplifier in Fig. 3, replace the transistor with its T equivalent circuit, assuming $\lambda = 0$. Derive expressions for the voltage gains v_s/v_i and v_d/v_i.

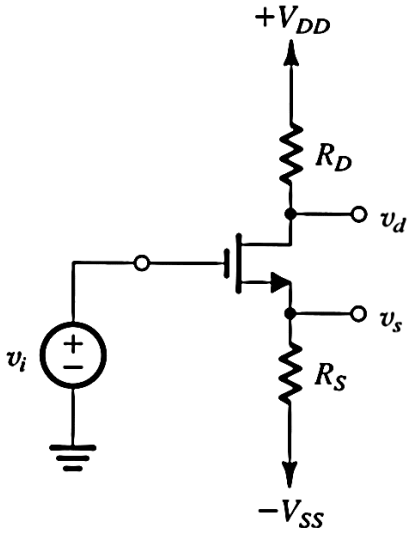

Figure 3