ShanghaiTech University
School of Information Science and Technology

EE112 Analog Integrated Circuits I

Homework 7

Due: Dec. 1st before exam

Read the chapter 7.

1. A CG amplifier using an NMOS transistor for which g_m = 2 mA/V has a 5 kΩ drain resistance R_D and a 5 kΩ load resistance R_L. The amplifier is driven by a voltage source having a 750 Ω resistance. What is the input resistance of the amplifier? What is the overall voltage gain G_v? By what factor must the bias current I_D of the MOSFET be changed so that R_{in} matches R_{sig}?

2. An emitter follower is operating at a collector bias current of 0.5 mA and is used to connect a 10 kΩ source to a 1kΩ load. If the nominal value of β is 100, what output resistance R_{out} and overall voltage gain G_v result? Now if transistor β is specified to lie in the range 50 to 150, find the corresponding range of R_{out} and G_v.

3. An NMOS transistor is connected in the bias circuit of Fig. 1, with V_G = 5 V and R_S = 3 kΩ. The transistor has V_t = 1 V and k_n = 2 mA/V^2. What bias current results? If a transistor for which k_n is 50% higher is used, what is the resulting percentage increase in I_D?

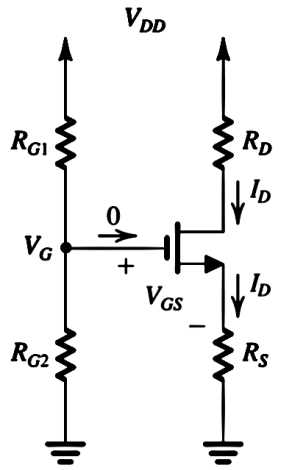

Figure 1

4. For the circuit in Fig. 2 find the value of R that will result in $I_O \approx 0.5$ mA. What is the largest voltage that can be applied to the collector? Assume $|V_{BE}| = 0.7$ V.

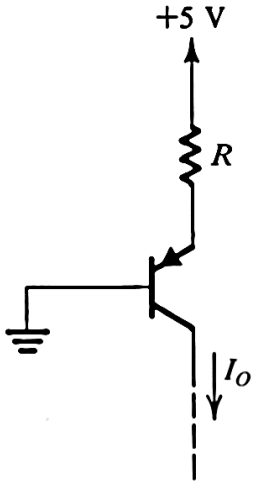

Figure 2

5. Figure 3 shows the circuit of an amplifier fed with a signal source v_{sig} with a source resistance R_{sig}. The bias circuitry is not shown. Replace the BJT with its hybrid-π equivalent circuit of Fig. 4. Find the input resistance $R_{in} \equiv v_\pi/i_b$, the voltage transmission from source to amplifier input, v_π/v_{sig}, and the voltage gain from base to collector, v_o/v_π. Use these to show that the overall voltage gain v_o/v_{sig} is given by

$$\frac{v_o}{v_{sig}} = -\frac{\beta R_C}{r_\pi + R_{sig}}$$

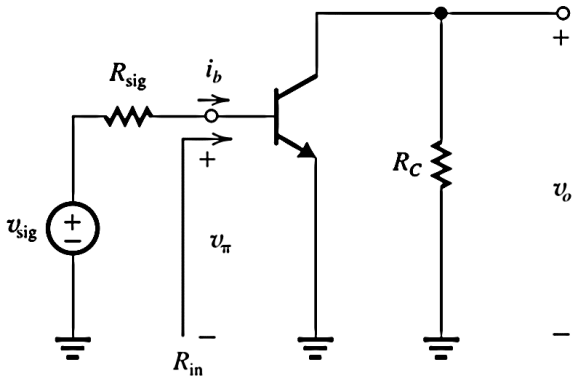

Figure 3

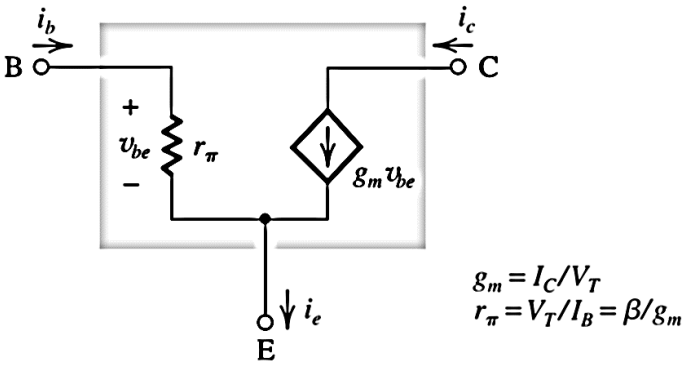

Figure 4

6. Using the topology of Fig. 5, design an amplifier to operate between a 2 kΩ source and a 2 kΩ load with a gain v_o/v_{sig} of –40 V/V. The power supply available is 15 V. Use an emitter current of approximately 2 mA and a current of about one-tenth of that in the voltage divider that feeds the base, with the dc voltage at the base about one-third of the supply. The transistor available has β = 100. Use standard 5% resistors (see Appendix J).

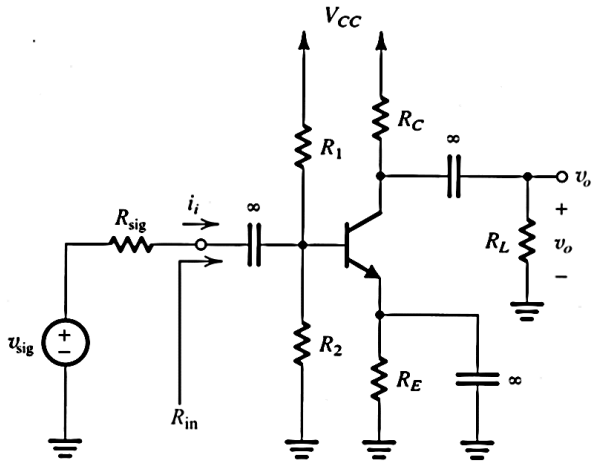

Figure 5

7. For the emitter follower in Fig. 6, the signal source is directly coupled to the transistor base. If the dc component of v_{sig} is zero, find the dc emitter current. Assume β = 100. Neglecting r_o, find R_{in}, the voltage gain v_o/v_{sig}, the current gain i_o/i_i, and the output resistance R_{out}.

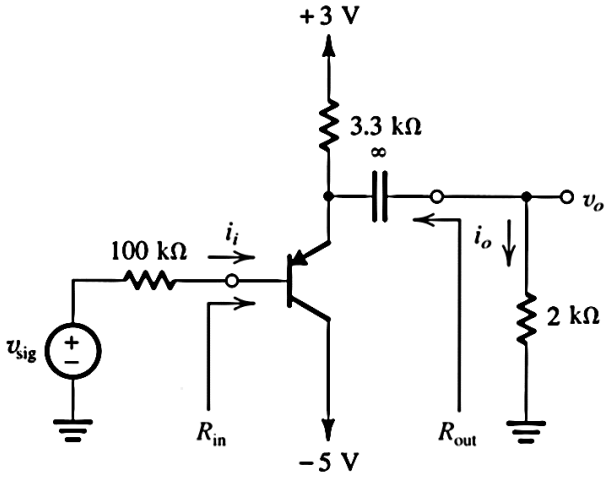

Figure 6