ShanghaiTech University
School of Information Science and Technology

EE112 Analog Integrated Circuits I

Homework 8

Due: Dec. 13th Before Lecture

Read the chapter 8.

1. For the current-steering circuit of Fig. 1, find I_O in terms of I_{REF} and device W/L ratios.

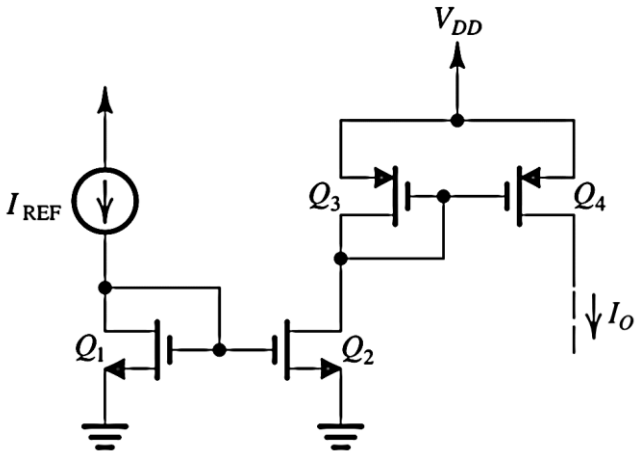

Figure 1

2. For the circuit in Fig. 2, let $|V_{BE}| = 0.7$ V and $\beta = \infty$. Find I, V_1, V_2, V_3, V_4, and V_5 for (a) $R = 10$ kΩ and (b) $R = 100$ kΩ.

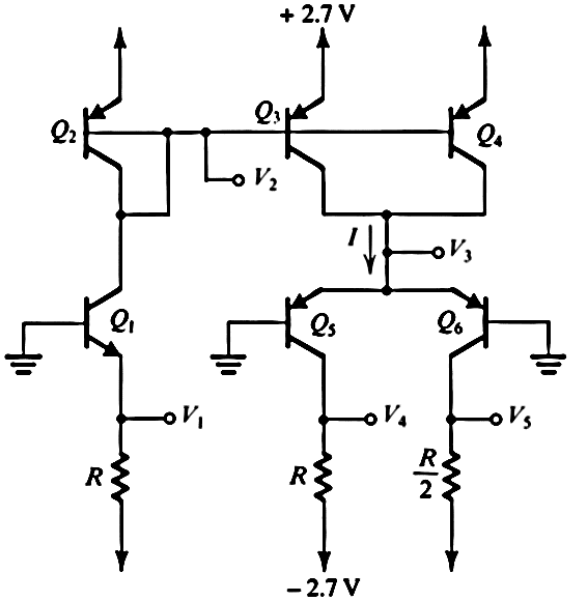

Figure 2

3. Fig.3 shows an IC MOS amplifier formed by cascading two common-source stages. Assuming that $V_{An} = |V_{Ap}|$ and that the biasing current sources have output resistances equal to those of Q_1 and Q_2, find an expression for the overall voltage gain in terms of g_m and r_o of Q_1 and Q_2. If Q_1 and Q_2 are to be operated at equal overdrive voltages, $|V_{OV}|$, find the required value of $|V_{OV}|$ if $|V_A| = 5$ V and the gain required is 400 V/V.

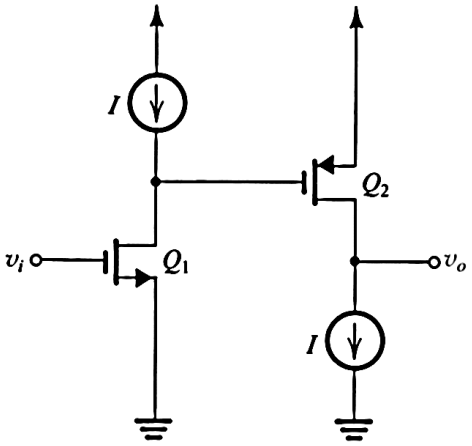

Figure 3

4. In the common-gate amplifier circuit of Fig. 4, Q_2 and Q_3 are matched. $k_n'(W/L)_n = k_p'(W/L)_p = 4$ mA/V^2, and all transistors have $|V_t| = 0.8$ V and $|V_A| = 20$ V. The signal v_{sig} is a small sinusoidal signal with no dc component.

(a) Neglecting the effect of V_A, find the dc drain current of Q_1 and the required value of V_{BIAS}.

(b) Find the values of g_{m1} and r_o for all transistors.

(c) Find the value of R_{in}.

(d) Find the value of R_{out}.

(e) Calculate the voltage gains v_o/v_i and v_o/v_{sig}.

(f) How large can v_{sig} be (peak-to-peak) while maintaining saturation-mode operation for Q_1 and Q_2?

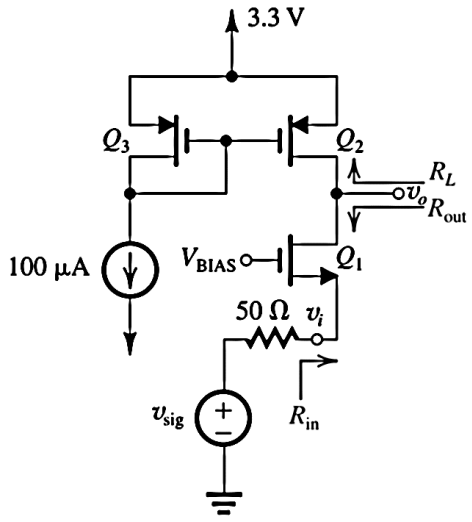

Figure 4

5. In this problem, we will explore the difference between using a BJT as cascode device and a MOSFET as cascode device. Refer to Fig. 5. Given the following data, calculate G_m, R_o, and A_{vo} for the circuits (a) and (b): I = 100 μA, β = 125, $\mu_n C_{ox}$ = 400 μA/V^2, W/L = 25, V_A= 1.8 V.

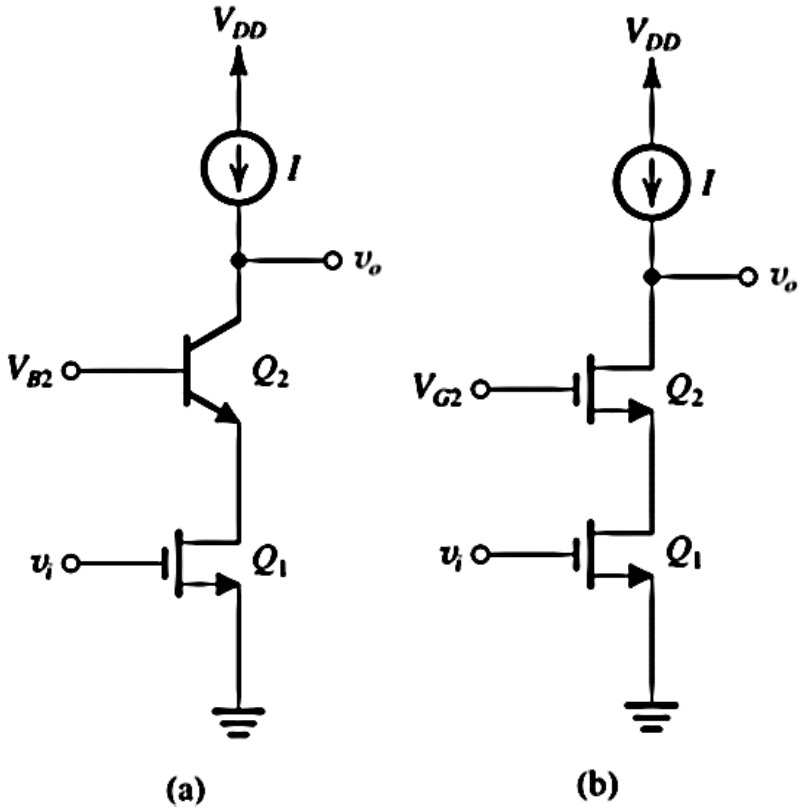

Figure 5

6. The transistors in the circuit of Fig. 6 have β = 100 and V_A = 50 V.
(a) Find R_{in} and the overall voltage gain.
(b) What is the effect of increasing the bias currents by a factor of 10 on R_{in}, G_v, and the power dissipation?

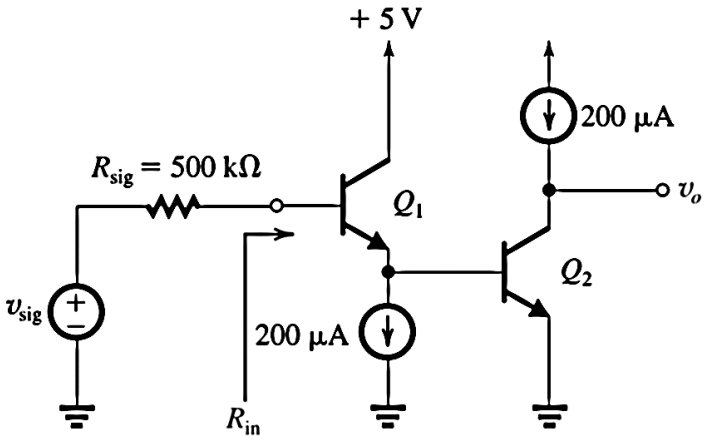

Figure 6