A Composite CMOS Pair and an Adjoint

In Honor of Professor M. N. S. Swamy's 75th Birthday

Haoyu Wang and Robert W. Newcomb
Microsystems Laboratory, ECE Department
University of Maryland
College Park, MD 20742 USA
E-mail: {newcomb, wanghy}@umd.edu

***Abstract*—The CMOS transistor pair of Seevinck and Wassenaar is reviewed. Beside the properties previously reported it is shown by calculating the effective SPICE parameter LAMBDA that the channel length modulation is improved. The analytic derivation is verified by simulations of both P and N type pairs. It is also shown that for small effective gate voltages a negative incremental resistance is obtained for which the adjoint is found following the theory of Professor Swamy.**

I. INTRODUCTION

In 1972 under the direction of Professor Swamy an adjoint theory for nonlinear circuits was introduced [1]. And in1987 Seevinck and Wassenaar introduced the nonlinear CMOS pair shown in Figure 1 [2, Figure 2], showing that it had various advantages when incorporated in circuits such as linear voltage controlled current sources {their linear MOS transconductor, often now called operational transconductance amplifiers (OTAs)}. One of their interesting uses was as a floating-bias voltage source realized by a diode-connected CMOS pair [2, Figure 4]. With the improving floating-bias voltage source characteristic, the CMOS pair can find its applications in both linear and nonlinear circuits. Here we consider the diode-connected CMOS pair as a three terminal equivalent transistor of interest in its own right. As there are two ways to diode connect the CMOS pair, there are two different diode connected pairs, one behaving as an NMOS transistor and the other as a PMOS one, these being shown in Figure 2. In the following we analyze the properties of the NMOS pair with the PMOS one having complementary properties. Then in Section IV we show that this device can behave as a negative differential resistor to which the adjoint theory of Professor Swamy [1] holds. That being the case we find in Section IV its adjoint.

Although not discussed in [2], from the analysis we find that the channel length modulation effect is apparently decreased for the diode-connected pair. This effect could be used to generate improved devices such as cascode current mirrors. With the availability of the simple, linear, tunable transconductor composed by the composite CMOS pair, a variety of applications have been realized in analog signal processing systems, such as voltage amplifiers, OTA's gyrators, oscillators, complete filters, and four-quadrant multipliers. [2]- [7]

Besides these attractive features, the drawback of the composite CMOS pair is that the equivalent threshold voltage is too large to be applied in the low power supply operation. Also, the decrease of equivalent transconductance will incur noise issues. [7]

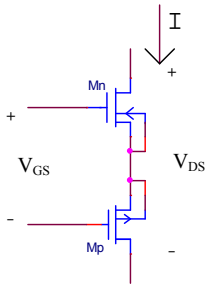

Figure 1. The CMOS pair of [1]

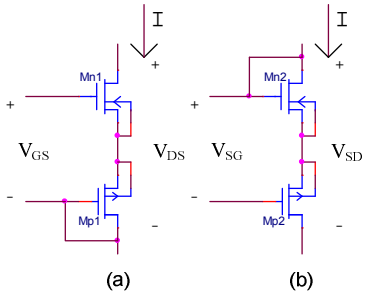

Figure 2. Diode-connected CMOS pairs. (a) NMOS, (b) PMOS

II. MODELING AND MATHEMATICAL DERIVATIONS

Following [2] we assume when turned on both transistors in the pair are in saturation in which case

$$I = \beta_n (V_{GSn} - V_{thn})^2 (1 + \lambda_n V_{DSn}) \quad (1a)$$

$$= \beta_p (V_{SGp} - |V_{thp}|)^2 (1 + \lambda_p V_{SDp}) \ . \quad (1b)$$

Where I is the NMOS drain current and the PMOS source current, the V_{th} are threshold voltages, $V_{GS} = -V_{SG}$ & $V_{DS} = -V_{SD}$ are gate-source and drain to source voltages, respectively; also $2\beta = K_P(W/L)$ where $K_P = \mu C_{ox}$ and W & L are the channel width and length.

We apply these to the equivalent NMOS diode connected diode-connected CMOS pair of Figure 2(a). We assume that the device has the equivalent description

$$I = \beta(V_{GS} - V_{th})^2(1 + \lambda V_{DS}) \quad . \tag{2}$$

As in [1], by solving for V_{GS} while assuming $\lambda = 0$, we find

$$\beta = \frac{\beta_n \beta_p}{(\sqrt{\beta_n} + \sqrt{\beta_p})^2} \tag{3a}$$

$$V_{th} = V_{thn} + |V_{thp}| . \tag{3b}$$

To obtain the relationship for λ we note that quite accurately (dividing (1a) by (1b))

$$I \approx \frac{1 + \lambda_n V_{DSn}}{1 + \lambda_p V_{SDp}} \Rightarrow V_{SDp} = \frac{\lambda_n}{\lambda_p} V_{DSn} . \tag{4a}$$

And by Kirchhoff's law (and (4a)),

$$V_{SDp} = V_{DS} - V_{DSn}$$

$$\Rightarrow V_{DSn} = (\frac{\lambda_p}{\lambda_n + \lambda_p}) V_{DS} . \tag{4b}$$

Again dividing (1a) by (2) gives on using (4b)

$$I \approx \frac{1 + \lambda_n V_{DSn}}{1 + \lambda V_{DS}} \Rightarrow \lambda V_{DS} = \frac{\lambda_p \lambda_n}{\lambda_n + \lambda_p} V_{DS} \tag{4c}$$

to finally give

$$\lambda = \frac{\lambda_n \lambda_p}{\lambda_n + \lambda_p} . \tag{5}$$

It should be noted that if the two transistors in the diode-connected pair are completely complementary then the β is decreased by a factor or 4, λ is decreased and V_{th} is increased by a factor of 2.

III. Simulations Results

To check the analytic theory we use the MOSIS 2 micron transistors since they closely follow equations (1) and we have their SPICE parameters available on the web [8]. The key ones of these are, for W = L and the bulk tied to the source (giving $V_{th} = V_{TO}$):

$\beta_n = 2.524\times10^{-5}$ A/V^2, $\beta_p = 0.954\times10^{-5}$ A/V^2,
$\lambda_n = 0.01843$ V^{-1}, $\lambda_p = 0.05012$ V^{-1},
$V_{Ton} = 0.858$ V, $V_{Top} = -0.889$ V.

From equations (3) & (4) these give for both diode-connected pairs of Fig. 2

$\beta = 3.659\times10^{-6}$ A/V^2, $V_{th} = 1.747$ V, $\lambda = 0.013$ V^{-1}.

Figure 3 gives SPICE runs for the drain current I on the Y axis vs. the V_{DS} on the X axis with V_{GS} varied. The Y axis scale for the top varies from 0 to 1.2 milliAmps while on the bottom it varies from 0 to 120 microAmps. From these curves the differences between the normal NMOS at the top versus the diode-connected NMOS at the bottom can be seen.

To calculate the simulated value for λ we find the slope of the curve, S at a current I for V_{DS} in the flat region

$$S = \frac{\partial I}{\partial V_{DS}} = \lambda \frac{I}{(1 + \lambda V_{DS})} \tag{6a}$$

and solve for λ

$$\lambda = \frac{S}{I - S \cdot V_{DS}} . \tag{6b}$$

The using (6) on the SPICE cursors values for $V_{DS} = 8$ V, $V_{GS} = 8$V, I = 113.8 uA gives $\lambda = 0.0086$ V^{-1} as compared to the calculated value of 0.013 V^{-1}. The difference is seen to come from the approximation to 1 at (4a).

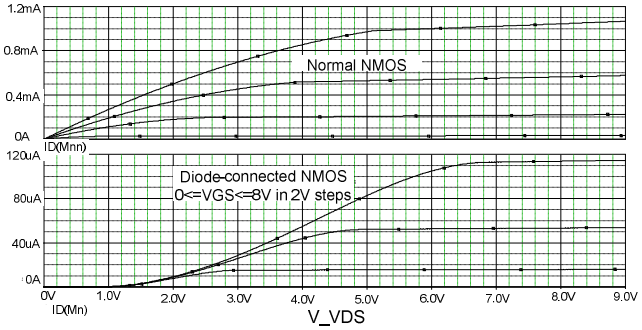

Figure 3. I_D vs. V_{DS}, $0 \le V_{DS} \le 9$ V, with V_{GS} in 2 V steps, $0 \le V_{GS} \le 8$ V. Top = normal NMOS (Y axis from 0 to 1.2 mA), bottom = diode-connected NMOS (Y axis from 0 to 120 uA).

IV. A Resistor with Negative Incremental Resistance

If instead of tying the bulks to the sources of their own transistors they are tied to the drains of the complementary transistor of the diode-connection, as shown in figure 4, the threshold voltage becomes dependent upon the drain to source voltage. This leads to negative slope in what is otherwise the constant current region. Figure 5 illustrates the effect (the top curve is for $V_{GS} = 4$ V with the $V_{GS} = 1$ V cut off).

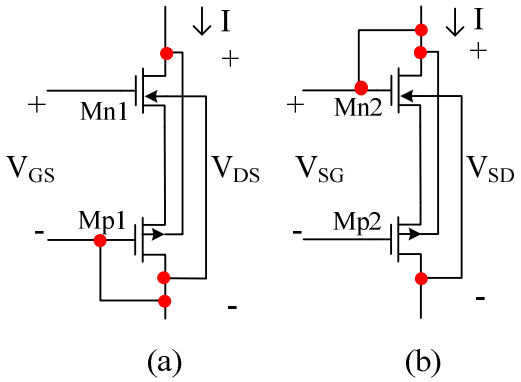

Figure 4. Modified Diode-connected CMOS pairs. (a) NMOS, (b) PMOS

Using the laws of the transistors one can see the negative incremental resistance from the fact that the threshold voltage changes via V_{DS} (for the NMOS diode connection) by the addition of

$$(\lambda_n + \lambda_p)[\sqrt{(\frac{\lambda}{\lambda_p})V_{DS} + \varphi} + \sqrt{\varphi}] \tag{7}$$

to V_{th} of (3b), where φ = 0.6 V.

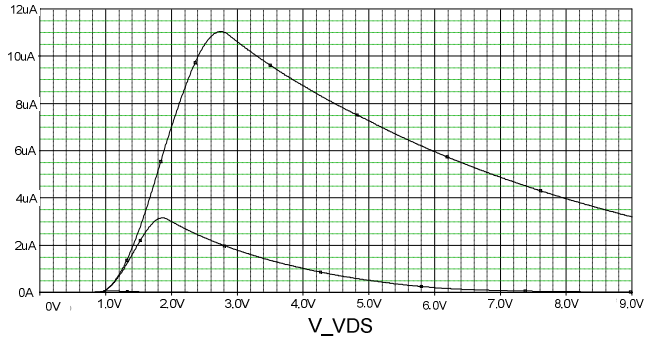

Figure 5. Bulks tied to complement sources. I_D vs. V_{DS}, $0 \le V_{DS} \le 9$ V, with V_{GS} in 1 V steps, $0 \le V_{GS} \le 4$ V. Y axis from 0 to 12 uA.

If instead of tying the bulks within the diode-connected device we tie them to the bias sources which normally are larger than internal voltages we note that the threshold voltage will remain essentially constant so that curves similar to those of Fig. 3 will result, though with larger threshold voltages.

V. The Adjoint

In the 1972 paper [1] under Professor Swamy the adjoint of a nonlinear time-invariant circuit was introduced in order to find the sensitivity with respect to a circuit parameter. This used the convolution in the time domain of voltages or currents in the original circuit with those in the adjoint. Although this did not cover transistors as such, we can readily extend it to them. Here, however, we apply the theory given in [1] directly to the resistor of Section IV. For that we use the very first entry in Table I of [1] as applied to I of (2) with V_{GS} fixed and with I varying with V_{DS} and dependent upon various parameters. Denoting adjoint quantities by superscript a, Choosing λ as the parameter and using (7), we have

$$I^a = \lambda \frac{\partial I}{\partial(\lambda V_{DS})} V_{DS}^a \tag{8a}$$

$$= \lambda[\frac{1}{(1+\lambda V_{DS})} - (1+\frac{\lambda_n}{\lambda_p})\frac{1}{(V_{GS}-V_{th})}]V_{DS}^a \tag{8b}$$

Here V_{DS}, and V_{th} as a function of it, is calculated in the original circuit and used (along with the constant V_{GS}) in the adjoint circuit. Note that the adjoint of this resistor is another resistor but with somewhat different characteristics. The contribution to the sensitivity is given, again from the first row of Table I of [1], by

$$-\frac{(\Delta\lambda)}{\lambda}(V_{DS} * I^a) \tag{8c}$$

VI. Conclusions

Using the approximation of (4a) we repeat the results of [2] and are able to obtain the new λ of a diode-connected CMOS pair. The analytic results are close to the simulated results but do reflect the approximation of (4a). By connecting the bulks to complementary sources we obtain a new device with negative incremental resistance. For this device we are able to apply the nonlinear sensitivity analysis of Professor Swamy [1] by finding its adjoint. However, many open problems are raised, including the need for finding the adjoints of the full diode-connected device.

References

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