Design of a Phase-Shifted ZVS Full-Bridge Front-End DC/DC Converter for Fuel Cell Inverter Applications

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***Abstract* – In this paper, a phase-shifted ZVS full-bridge DC/DC converter is investigated and designed to function as the voltage boosting stage of a two stage power inverter for a fuel cell powered Distributed Energy System (DES). Design considerations of the ZVS DC/DC converter are discussed in detail. The complex resonant tank analysis of the converter design is simplified using the state plane approximation technique. This technique is used to obtain a linear small signal model. Using this model, the DC/DC converter is designed and simulated. The simulation results validated the state plane approximation technique. In addition to this, an RCD snubber circuit is employed in order to filter the output noise of the circuit.**

Index Terms:* *DC/DC converter, fuel cell, full bridge, phase-shift, pulse width modulation, RCD snubber, zero voltage switching.

I. INTRODUCTION

Substantial amount of research has been conducted to effectively utilize the energy from fuel cells [1-3]. Fuel cells convert chemical energy stored in fuel directly into electrical power. In comparison to other energy sources, fuel cells are very efficient in their fuel-to-electric conversion [1]. Fuel cells have low emission and vibration, which can make them suitable for on-site electricity production. Moreover, fuel cells have applications for residential heating and power systems [2].

With the emerging trend of distributed energy generation, there is an increased demand for improved power electronic technologies such as power converters and energy storage systems. For distributed energy generation to become more cost effective, available and reliable, power converter technology must become more efficient and dependable.

A fuel cell inverter converts the DC voltage from fuel cells to an AC output for grid integration. Generally, as shown in Fig. 1, a fuel cell inverter has two main components: a DC/DC converter and a DC/AC inverter. The first stage is required to boost the DC voltage of the fuel cell to an appropriate higher level, 400V for this design, and to regulate the low-voltage and high-current output of the fuel cell. The second stage converts this DC signal into a 60Hz AC signal. This work focuses on the design of the first stage of a fuel cell inverter. The design specifications are listed in Table I.

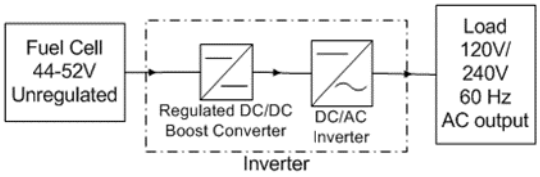

Fig. 1: Block diagram of fuel cells inverter.

TABLE I: DC/DC CONVERTER DESIGN SPECIFICATIONS

Description	Min.	Typ.	Max.
Input Voltage (V)	44	48	52
Output Voltage (V)	-	400	-
Output Power (W)	400	-	1200
Frequency (KHz)	-	100	-

There are several types of DC/DC converter topologies such as buck, boost, buck-boost, Ćuk, flyback, forward, half-bridge and full-bridge configurations. Each of these topologies has its own advantages and disadvantages based on the requirements of the specified application. For this particular application, the full-bridge converter topology, shown in Fig. 2, is chosen.

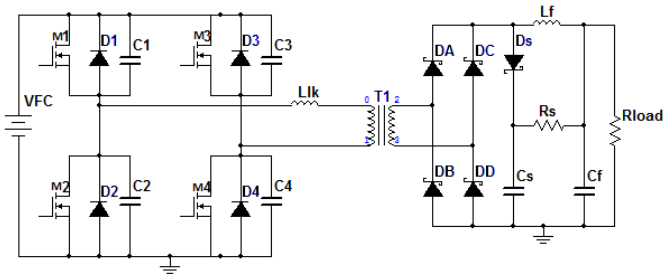

Fig. 2: Full-bridge converter with parasitic elements.

In order to ensure circuit efficiency, the ZVS technique was used [3-6] in conjunction with an RCD snubber circuit [7]. This technique uses the parasitic elements within the full-bridge converter to create a resonant tank and enable zero voltage across the switching elements before they are turned on. Having this zero voltage drop across switching elements helps to avoid the overlap of switching current and voltage that can cause power dissipation. This is appealing for high voltage converters, as transformer leakage inductance and winding capacitance leads to a resonant network within the

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circuit [6]. This technique also allows for high frequency applications as the switching losses are proportional to the switching frequency.

The advantages of full-bridge configuration lie in three aspects. First, it provide the galvanic isolation. In full cell inverter application, galvanic isolation between the input and output is desired because it allows the full cells to be isolated from the grid, which improves the safety and decreases noise sensitivity. In addition, galvanic isolation helps to mitigate transistor and diode device stress [8]. Secondly, with this topology it is possible to achieve zero-voltage-switching (ZVS), and thereby substantially decrease switching losses and increase the overall conversion efficiency [3-6]. Thirdly, various specialized controller integrated circuits (ICs) are available for full-bridge converters [9].

Disadvantages of a full-bridge configuration can occur when operating in a high-output-voltage mode. This includes parasitic secondary ringing and the stress it creates on the rectifier diodes. In order to alleviate this, an RCD snubber circuit can be employed. RCD snubber circuits are commonly used to prevent the secondary voltage from exceeding a desired level [7].

The contribution of this paper is to introduce a simple method to analyze a full-bridge DC/DC converter employing the ZVS technique. By using state plan analysis and averaging method, complex resonant circuit analysis is reduced to a simpler geometric analysis [5,6]. Also, the use of an RCD snubber circuit is tested.

II. FULL-BRIDGE CONVERTER

The full-bridge converter topology consists of a DC power source, an H-bridge MOSFET configuration, a high frequency transformer, a full bridge diode rectifier, a low pass LC filter and a resistive load. The H-bridge MOSFETs are controlled in such a way to produce an AC voltage at the primary side of the transformer. Then, this AC voltage is scaled up using the transformer. On the secondary side, a full bridge diode rectifier is utilized to rectify the high frequency AC voltage to a DC voltage. Finally, the LC filter is used to create a smooth DC output. Occasionally, snubber circuits are incorporated to suppress the transient current spikes.

Based on the switching mode, there are two types of converters: hard-switched and soft-switched pulse-width-modulated (PWM) converters [5,6]. For hard-switched PWM converters, there is a voltage-current overlap during the switching transition, which leads to substantial losses. Since the number of switching transitions increase with the increase of switching frequency, hard-switched PWM converts are generally inefficient in high frequency applications.

The merit of a soft switched full-bridge converter comes with the idea of eliminating this loss by removing the voltage-current overlaps. To make soft switching possible, a phase-shifted PWM technique is employed. This technique introduces a deliberate phase shift within the switching transitions of each transistor pair of the H-bridge legs so that the output is controlled as function of the phase difference. The phase shift variable, ϕ, is defined as the percentage of the on-time of each transistor over the switching cycle. This variable has a range of $0 \leq \phi \leq 1$.

$$\phi = \frac{t_{on}}{T_S} \tag{1}$$

The relationship between the primary and secondary voltage of the transformer depends on the number of turns on each side as well as the phase shift variable. If the voltage drop across conducting MOSFETs is assumed to be negligible, then the primary side voltage and the input voltage are equal. This can be seen in the following equation.

$$V_{sec} = \frac{N_s}{N_p} \cdot \phi \cdot V_{prim} = n \cdot \phi \cdot V_{in} \tag{2}$$

where N_s and N_p are the number of turns in the secondary and primary of the transformer respectively and n is their ratio.

To relate the secondary voltage to the output voltage, the principle of volt-second balance is employed [6]. It states that the average voltage value that is applied to an ideal inductor must be zero. Thus, in steady state analysis, assuming negligible voltage drop across the rectifying diodes, the voltage drop across the secondary side of the transformer is equal to the output voltage. Thus, the input voltage and the output voltage are related by the conversion ratio, M, which is defined in the following equation.

$$M(\phi) = \frac{V_{out}}{V_{in}} = n \cdot \phi \tag{3}$$

A. State Plane Analysis: Averaging and Normalization

State Plane Analysis is employed to simplify the complex resonant tank analysis to simple geometrics. The theory behind this concept is to use averaging and normalization techniques.

Averaging involves neglecting high frequency components and using only the DC and low frequency components of signals. This assumption is good as long as the period is much smaller than the system's natural response time [6]. Normalization of the tank waveforms helps to simplify figures in the state plane. The tank characteristic impedance, R_o, is used as base impedance, R_{base}. The base voltage, V_{base}, can be chosen arbitrarily. The normalized values that are used for the plane analysis consist of the following equations.

Base voltage:

$$V_{base} = V_{in} \tag{4}$$

Base impedance:

$$R_0 = \sqrt{\frac{L_{lk}}{C_{eq}}} \tag{5}$$

Base current:

$$I_{base} = \frac{V_{base}}{R_0} \tag{6}$$

Normalized Voltage of M2:

$$m_2 = \frac{V_{M2}}{V_{base}} \tag{7}$$

Normalized leakage inductor current:

$$j_{Lk} = \frac{i_{Lk}}{I_{base}} \tag{8}$$

Peak normalized leakage inductor current:

$$J_{Lk} = \frac{n \cdot I_{out}}{I_{base}} \tag{9}$$

Normalized frequency:

$$F = \frac{f_s}{f_0} \tag{10}$$

where L_{lk} is the leakage inductance of the transformer, C_{eq} is the equivalent capacitance of the parasitic capacitance and any discrete capacitance of the converter, V_{in} is the input voltage from the fuel cell, V_{M2} is the on-state voltage drop across M_2 as shown in Fig. 2, i_{Lk} is the instantaneous current through the transformer, I_{out} is the output DC current, f_s is the switching frequency and f_o is the resonant frequency of the tank.

The normalized state plane is a plot of $m_2(t)$ vs. $j_L(t)$ with 't' used as implicit parameter. For ZVS, it is required to have $j_{LK} \geq 1$ [6]. If j_{LK} is less than one, V_{M2} cannot reach the value of V_{base} and switching loss will be unavoidable.

B. *Step-by-Step Analyses of the Phase-Shifted PWM Full-Bridge Converter (PS-PWM-FB Converter)*

The ZVS technique effectively uses the parasitic elements to enable lossless switching transitions. These parasitic elements include the MOSFET's built-in diode and capacitance and the transformer's leakage inductance. It is also possible to include a separate discrete capacitor to alter the equivalent capacitance of the resonant tank. Fig. 2 depicts the overall system of a full-bridge converter employing the Snubber circuit. The ZVS technique uses the phase shifting technique to create a deliberate dead time where all the switching transistors remain off due to the resonant tank created from the parasitic elements.

The complete cycle of the PS-PWM FB converter consists of twelve subintervals. The step-by-step analysis of these subintervals are described below [5,6]. Fig. 3 displays the waveforms that are used to describe how the system operates. Note that the subintervals on the x axis are not to scale. Also it assumes that the gate drivers of the switching MOSFETs have abrupt transitions.

As shown in Fig. 4, *Subinterval 0* (t_0) is the duration between T_0 and T_1. This is assumed to be the initial state of the cycle. At this subinterval, M_2, D_4 and all secondary diodes are conducting. With all rectifying diodes conducting simultaneously, the transformer is short-circuited on the secondary side. Consequently, the voltage across the primary is also zero. Furthermore, $I_{Lk} = -n \cdot I_{out}$ and $V_{out} = 0V$. *Subinterval 1* (t_1) begins when M_2 is turned off. D_4 and all the rectifier diodes continue to conduct. The negative current then begins to simultaneously charge up the parasitic capacitance C_2 while discharging the parasitic capacitance C_1. The equivalent circuit of this stage can be approximated as a simple LC circuit with a resonant frequency of ω_o which is given by the following equation

$$\omega_0 = \frac{1}{\sqrt{L_{Lk} \cdot C_{eq}}} \tag{11}$$

For this subdivision, the initial conditions are $j_{LK} = -j_{Lk}$ and $m_2 = 0$. It is concluded with $m_2 = 1$ and $j_{LK} = -j_{Lk1}$ where j_{Lk1} is the normalized current at T_2. The normalized state plan for this subinterval is shown in Fig. 3. The solution of the state plane geometry consists of,

$$j_{Lk1} = \sqrt{J_{Lk}^2 - 1} \tag{12}$$

$$\alpha = \omega_0 \cdot t_1 = \tan^{-1}\left(\frac{1}{j_{Lk1}}\right) \tag{13}$$

$$t_1 = \frac{\alpha}{\omega_0} \tag{14}$$

Subinterval 2 begins with D_1 becoming forward biased then clamping the voltage V_{M2_ds} to V_{in}. With the primary still shorted, the applied input voltage causes the leakage current to increase at the speed of V_{in}/L_{Lk}. This current, initially being $-n \cdot I_{out}$, becomes zero at the end of this subinterval. M_1 then starts conducting within this interval. At *Subinterval 3*, the commuting current continues to increase from zero to positive $n \cdot I_{out}$ with the same slope as the previous interval. The state plane analysis of t_2 and t_3 can be combined and summarized as shown in Fig. 4.

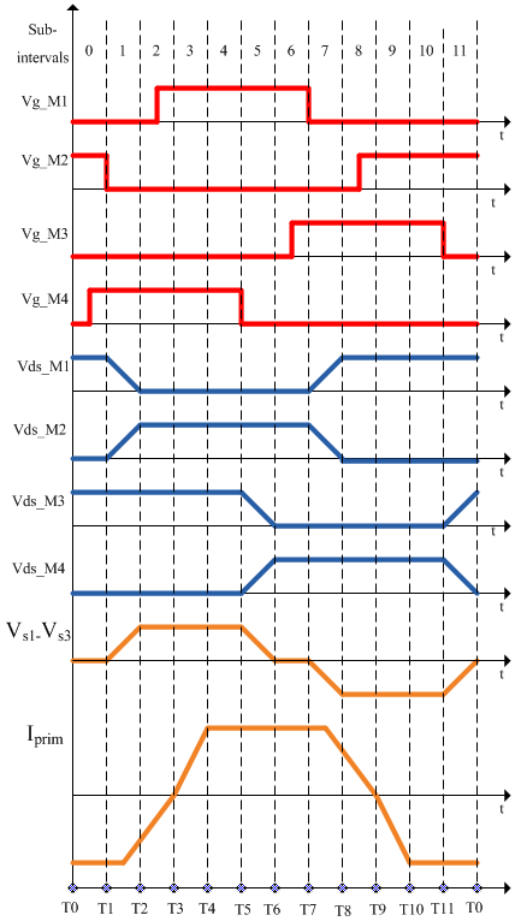

Fig. 3: Primary side waveforms of PS-PWM-FB converter with resonant complete transitions [6].

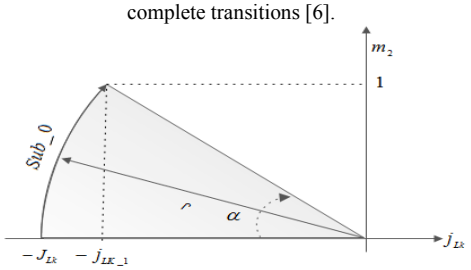

Fig. 4: State plane representation of *subinterval 1* [6].

From the current-voltage relationship of the inductor, the duration of t_2 and t_3 can be determined as the following.

$$t_2 + t_3 = \frac{L_{Lk}}{V_{in}}(n \cdot I_{out} + i_{Lk1}) \quad (15)$$

Subinterval 4 (t_4) is an active interval in which the input energy is transferred to the output. At this stage, D_C and D_D become reverse biased and there is nonzero voltage across the secondary. This step is concluded when M_4 is turned off. At *Subinterval 5* (t_5), D_A and D_D continue to conduct. With M_4 turned off at the previous stage, V_{ds_M4} starts to charge while V_{ds_M3} simultaneously discharges at the speed of $(n \cdot I_{out})/(C_{M3}+C_{M4})$. From the linear current-voltage relationship of the capacitor, the length of the interval is given by,

$$t_5 = \frac{L_{Lk}}{n \cdot I_{out}}(C_{M3} + C_{M4}) \quad (16)$$

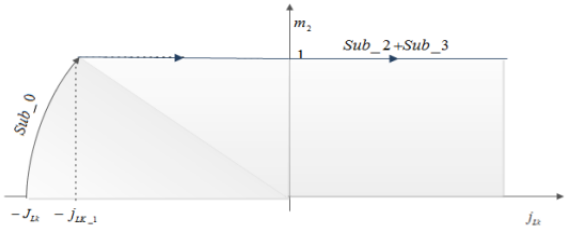

Fig. 5: State plane representation of *subintervals 2* and *3* [6].

Subinterval 6 (t_6) begins when D_B and D_C becoming forward biased, which shorts the secondary. The primary current, being at maximum and constant, freely circulates and causes conduction losses as it passes through the transformer and the switching MOSFETs. Minimizing this duration is very crucial so that the benefits obtained from the ZVS technique can be appreciated. This is possible by choosing the value of the turn ratio in such a way to get a phase shift of slightly less than unity [6].

Due to symmetry, the analysis of *Subintervals 7* to *11* and back to *Subinterval 0* are similar to that from *Subintervals 1* to *6*. The overall ZVS mechanisms are summarized in Table II. The complete normalized state plane is shown in Fig. 6 below. The corresponding output voltage is shown in Fig. 7. Due to symmetry, only half of the cycle is shown for the output.

TABLE II: SUMMARY OF THE COMPLETE ZVS ANALYSES

Subintervals	**0**	**1**	**2**	**3**	**4**	**5**
Conducting Devices	M_2	-	D_1/M_1	M_1		
	D_4			M_4		-
	D_A,D_B,D_C,D_D				D_A,D_D	
Subintervals	**6**	**7**	**8**	**9**	**10**	**11**
Conducting Devices	M_1	-	D_2/M_2	M_2		
	D_3			M_3		-
	D_A,D_B,D_C,D_D				D_B, D_C	

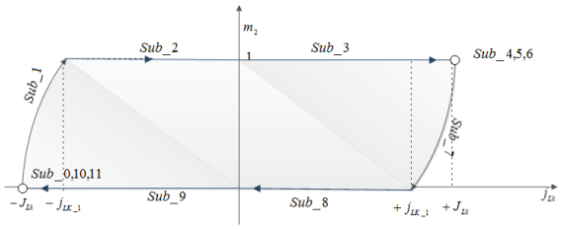

Fig. 6: The complete state trajectory [6].

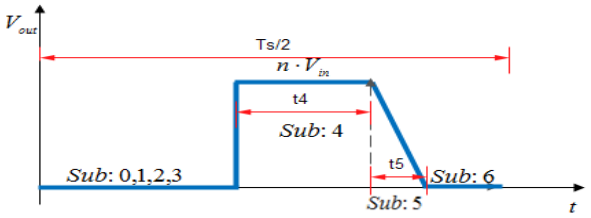

Fig. 7: Average output voltage [6].

The average output voltage is equal to the area under the curve. This can be calculated as the following.

$$< V_o > = \frac{2}{T_s}\left(n \cdot V_{in} \cdot t_4 + \frac{1}{2} n \cdot V_{in} \cdot t_5\right) \quad (17)$$

C. *Phase shift control*

Phase shift control, ϕ, performs the role of the duty cycle. As shown in Fig. 8, when ϕ is zero, V_{ds_M2} and V_{ds_M4} are in phase and the output voltage is zero. When ϕ is 1, V_{ds_M4} and V_{ds_M2} are opposite in phase and output voltage is at its maximum value. As shown in Eq. (1), the 'on-time' per half cycle is given by the following.

$$t_{on} = \phi \cdot \frac{T_s}{2} = t_1 + t_2 + t_3 + t_4 \quad (18)$$

If t_4 is calculated from the above relationship and the result is substituted into Eq. (17), the average voltage is given by the following.

$$< V_o > = \frac{2n \cdot V_{in}}{T_s}\left(\phi \cdot \frac{T_s}{2} - t_1 - t_2 - t_3 + \frac{1}{2} t_5\right) \quad (19)$$

With this, the turn ratio can be approximated as the following.

$$M(\phi) = \frac{V_{out}}{n \cdot V_{in}} \cong \frac{<V_o>}{n \cdot V_{in}} = \phi - \frac{2}{T_s}\left(t_1 + t_2 + t_3 - \frac{1}{2} t_5\right) \quad (20)$$

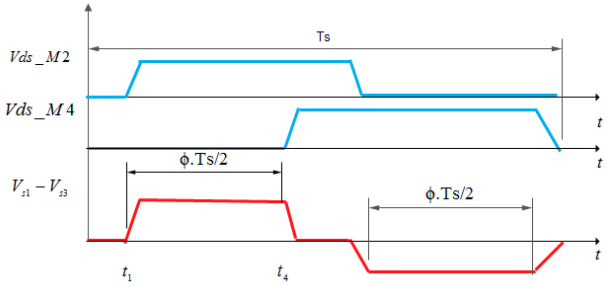

Fig. 8: Waveforms on the primary side of transformer [6].

Substituting Eqs. (14), (15) and (16) into (20) and normalizing the result gives the following.

$$M(\phi) = \phi + \frac{F}{2\pi}\left[\frac{1}{J_{Lk}} - 2\tan^{-1}\left(\frac{1}{\sqrt{J_{Lk}^2-1}}\right) - 2\left(J_{Lk} + \sqrt{J_{Lk}^2-1}\right)\right] \quad (21)$$

This equation is of the form:

$$M(\phi) = \phi + F \cdot P_{ZVT}(J_{Lk}) \quad (22)$$

Where F is a normalized frequency and P_{ZVT} is a small negative number which is defined as the following.

$$P_{ZVT}(J_{Lk}) = \frac{1}{2\pi}\left[\frac{1}{J_{Lk}} - 2\tan^{-1}\left(\frac{1}{\sqrt{J_{Lk}^2-1}}\right) - 2\left(J_{Lk} + \sqrt{J_{Lk}^2-1}\right)\right] \quad (23)$$

D. *Switching Delays and Pulse Width Calculations*

Due to the symmetry of the system, t_0=t_6, t_1=t_7, t_2+t_3=t_8+t_9, t_4=t_{10} and t_5=t_{11}. For analysis purposes, changes occurring within an interval are assumed to happen in the middle of the subinterval. For the cases where two subintervals are combined, it is assumed that time is linearly distributed within that range. Based on these assumptions and the complete cycle analysis of the system, the delays and pulse width magnitude of the gate driver signals are summarized in Table III. Note that the duration of *Subinterval 0* is calculated as the following.

$$t_0 = \frac{T_s}{2} - t_1 - (t_2 + t_3) - t_4 - t_5 \quad (24)$$

TABLE III: SUMMARY OF DELAYS AND PULSE WIDTH CALCULATIONS

FET	Delay	Pulse Width
M 1	$t_0 + t_1 + \frac{1}{4}(t_2 + t_3)$	$\frac{3}{4}(t_2 + t_3) + t_4 + t_5 + t_6$
M 2	$\sum_{n=0}^{7} t_n + \frac{1}{4}(t_8 + t_9)$	$\frac{3}{4}(t_8 + t_9) + t_{10} + t_{11} + t_0$
M 3	$\sum_{n=0}^{5} t_n + \frac{t_6}{2}$	$\frac{t_6}{2} + \sum_{n=7}^{10} t_n$
M 4	$\frac{t_0}{2}$	$\frac{t_0}{2} + \sum_{n=1}^{4} t_n$

E. *Design Guidelines and Constrains*

The design procedures employed to find the proper component values of the implemented circuit are listed in the following step-by-step analysis.

1. Based on the maximum, minimum and desired power specifications of the ZVS range, find (V_{in_max}, I_{out_max}), (V_{in_max}, I_{out_min}), (V_{in_min}, I_{out_max}), (V_{in_min}, I_{out_min}), ($V_{in\_nominal}$, $I_{out\_nominal}$). These are possible operating points.

2. For ZVS operation, it is required to have the value of j_{Lk} to be greater than one. If this is not the case, it not possible to have zero voltage across switching elements and thus there will be switching loss. Thus, the worst case scenario, which happens when there is the maximum input voltage and minimum output current, should be set such that $j_{LK} \geq J_{min} = 1.01$. The base impedance can be determined from J_{min} with the following equation.

$$j_{Lk} \geq J_{min} \rightarrow J_{min} = \frac{n \cdot I_{out}}{I_{base}} = \frac{n \cdot I_{out}}{\left(\frac{V_{base}}{R_0}\right)} \quad (25)$$

3. The turn ratio should be chosen in such a way that the effective duty cycle is only slightly less than 1.

$$n = \frac{V_{out}}{\phi \cdot V_{in}} \quad (26)$$

4. Using the winding capacitance of the transformer, the MOSFET capacitance and any additional discrete capacitance, the equivalent capacitance, C_{eq}, is calculated as,.

$$C_{eq} = \frac{4}{3}C_{MOSFET} + \frac{1}{2}C_{transformer} + C_{discrete} \quad (27)$$

5. The leakage inductance is calculated using Eq. (5). For a transformer to operate with square wave, minimizing leakage inductance and winding capacitance is imperative to avoid overshoots and unwanted oscillations [10].

6. The output filter inductor and capacitor values are then calculated based on the maximum ripple current and voltage amplitudes.

To guarantee ZVS transition, all the five operation points should have phase shift values that are within the allowed range: $0 \leq \phi \leq 1$. The ideal conversion ratio has a unity value. However, in practice, the resonant transitions reduce the value of the effective duty cycle as shown in Eq. (23). Thus, the converter should be designed such that it can operate at maximum phase-shift values.

III. SIMULATION RESULTS

The simulation of the PS-PWM FB converter was conducted using CoolSPICE provided by CoolCAD Electronics LLC. The simulation results are matched with the theoretical analysis.

To verify the ZVS transition, the switching transition of the passive-to-active leg, which is composed of M_1 and M_2, is analyzed here. This transition starts when M_2 is turned off. As shown in Fig. 9, M_1 is turned on with nearly zero-voltage across it. The same is valid for the active-to-passive transition of M_3 and M_4.

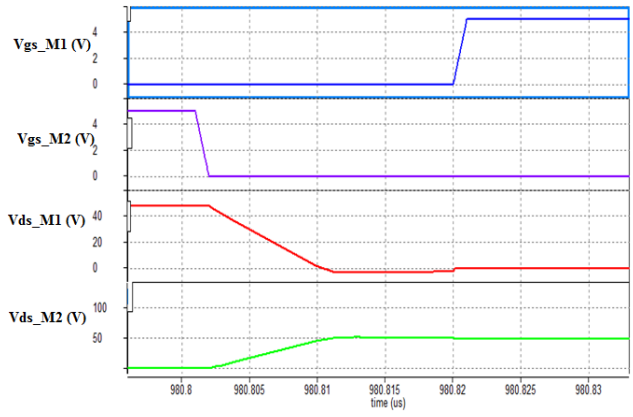

Fig. 9: Simulation result of the switching transition.

As shown in Fig. 10, the output voltage for the simulation is 401V and the current is 2.58 A, thus the output power is 1034 W.

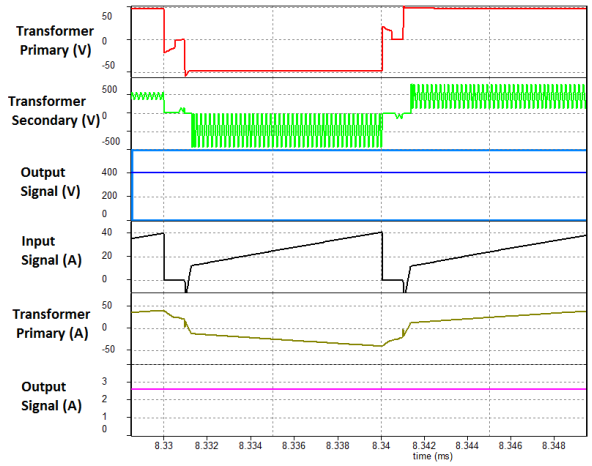

Fig. 10: Waveforms from simulation with snubber.

A. *RCD snubber circuit*

As shown in Fig. 10 above, the voltage drop across the secondary side of the transformer has a significant amount of ringing as well as large peak reverse voltage drops that can lead to rectifier diode breakdown. For this simulation, the ringing frequency, f_r, was measured to be 5.02 GHz. To eliminate this ringing, an RCD snubber circuit is used.

The snubber operates by allowing excess current, left over from when a pair of secondary diodes stop conducting, such as D_A and D_D or D_B and D_C in the case of Fig. 2. This current is lead through D_S and C_S, until the excess current is zero. The resistor, R_S, provides a discharge path in order to balance the snubbing capacitor [7].

Utilization of the snubber circuit even if there is an associated dissipation loss, is necessary to mitigate the parasitic ringing. Fig. 11 depicts the output of the converter after employing a snubber circuit [7]. As shown, the snubber circuit significantly reduces the ringing on the secondary.

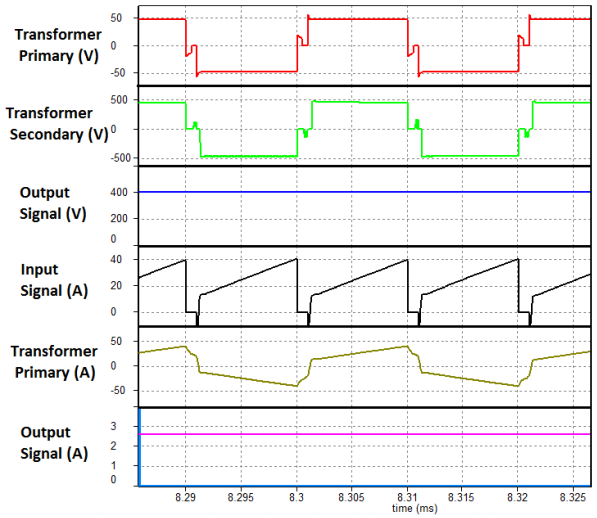

Fig. 11: Waveforms from simulation with snubber.

IV. CONCLUSIONS

The operation of a full bridge converter to regulate the output of a fuel cell is discussed and important design trade-offs and guidelines are presented. A method to design a phase shifted zero-voltage-switching DC/DC converter is also outlined successfully. The method is verified using CoolSPICE provided by CoolCAD Electronics LLC.

V. ACKNOWLEDGEMENT

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