# A Novel Approach to Design EV Battery Chargers Using SEPIC PFC Stage and Optimal Operating Point Tracking Technique for LLC Converter

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***Abstract*—In this paper, a plug-in electric vehicle battery charger is proposed based on SEPIC PFC and LLC topologies. In addition, a new approach in introduced to actively control the dc link voltage and track the maximum efficiency point of a LLC converter over the wide voltage range of the high voltage battery pack. Comprehensive circuit modeling and loss analysis at maximum efficiency point of LLC converter are carried out. A 3.3 kW charger, charging the Li-ion battery with an output voltage range of 100 V to 420 V from variable dc link voltage, is designed and simulated. In comparison to conventional approaches, the LLC stage demonstrates 4.4% efficiency improvement at the heaviest load condition and 16.5% efficiency improvement in the lightest load condition.**

## I. INTRODUCTION

Li-ion battery technology has dominated the battery market of plug-in electric vehicles (PEVs). This is due to its attractive features such as high energy density, no memory effect, and slow loss of charge. The charging profile of a typical Li-ion battery cell is plotted in Fig. 1. According to this profile, the voltage of a deeply depleted Li-ion cell can go down to 1 V. The wide voltage range of Li-ion cell is mapped to a wide voltage range (100 V – 420 V) of the on-board battery pack. Consequently, the on-board charger must be compatible with this wide voltage range [1].

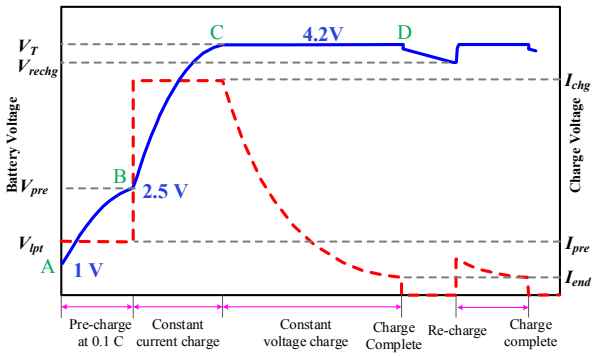


Fig. 1. Charging profile of Li-ion battery [2].

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A typical isolated charger consists of two power converters, front-end stage for rectification of ac input power and power factor correction (PFC), and second-stage dc/dc converter for voltage regulation and galvanic isolation [3]–[5]. Boost and its derivative topologies are commonly utilized in the PFC stage. This is because of their simple circuit configurations, continuous input current, and low total harmonic distortion (THD). In order to be compatible with universal grid voltages (85 V - 265 V, 47 Hz – 70 Hz), typically the dc link voltage is regulated at 390 V [6]–[8].

In dc/dc isolation stage, zero-voltage switching (ZVS) topologies are preferable to enhance efficiency of chargers [9]–[11]. In particular, LLC topology has several advantages over other ZVS topologies, such as (a) short circuit protection, (b) good voltage regulation in light load condition, (c) the ability to operate with ZVS over wide load ranges, and (d) no diode reverse recovery losses through soft commutation [10], [12]–[16].

The schematic of a conventional two stage isolated PEV battery charger based on boost PFC and full bridge LLC topologies is plotted in Fig. 2. In PEV battery charging applications, optimization of the LLC converter over the wide output voltage ranges becomes a challenging issue [8], [17], [18]. In [19] and [20], two recently reported LLC battery chargers have their output voltage ranges to be 320 V – 420 V and 250 V – 450 V, respectively. However, neither work is able to charge the deeply depleted battery pack (100 V – 250 V).

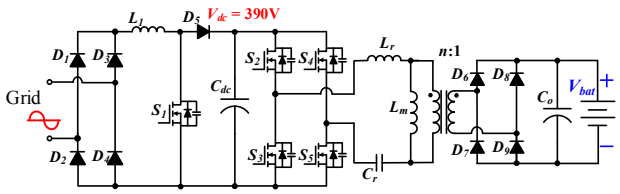


Fig. 2. Conventional two stage isolated charger based on boost PFC and full bridge LLC converters.

This paper proposes a new approach to optimize the efficiency of the LLC stage over the full battery voltage range (100 V – 420 V) and load conditions without adding any additional circuit or implementing on/off control. The schematic of the proposed charger is plotted in Fig. 3. A single-ended primary-inductor converter (SEPIC) PFC stage is utilized. Thus, the dc link voltage can vary in a wide range without satisfying the compatibility with universal grid input.

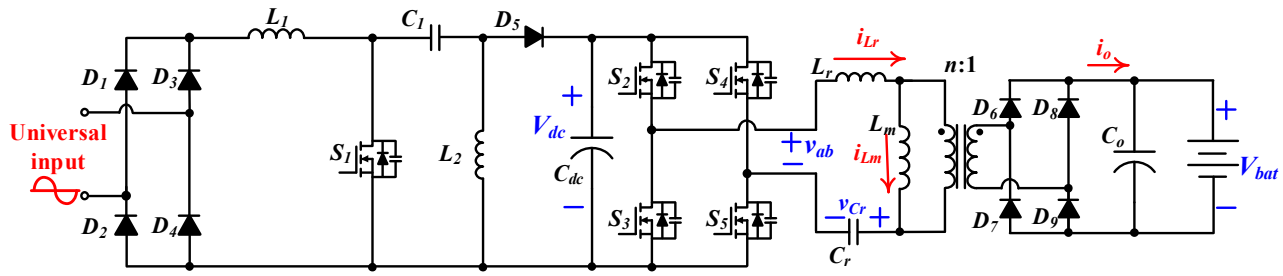


Fig .3. Proposed two stage isolated charger based on SPEIC and full bridge LLC topologies.

By actively controlling the dc link voltage with respect to the variation of battery voltage, the conversion efficiency of the dc/dc converter is always regulated to be the optimal value through keeping the switching frequency close to its primary resonant frequency and thereby minimizing the circulating current in the resonant tank. With the proposed maximum efficiency point tracking technique, the efficiency performance of dc/dc converter is improved across the wide battery voltage range.

## II. Proposed Maximum Efficiency Point Tracking of LLC Converter

### A. Optimal operation point of LLC converter

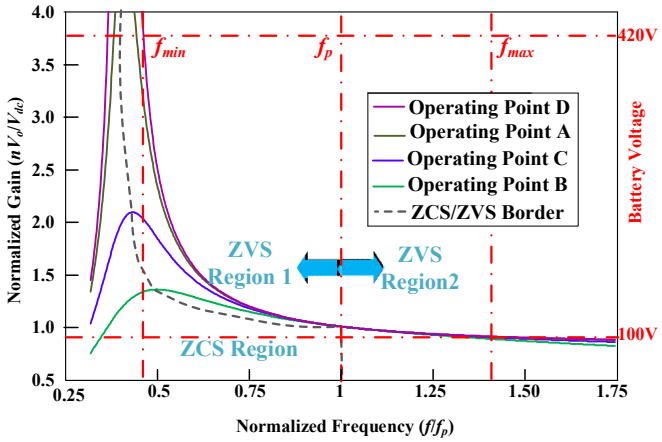


Fig. 4. DC voltage characteristics of LLC stage.

Based on the battery charging profile given in Fig. 1, the dc voltage characteristics of a LLC PEV battery charger with fixed 390 V dc link voltage is extracted as shown in Fig. 4. Four different curves corresponding to the four critical operating points in the charging process of a Li-ion battery pack rated at 3.3 kW, are marked in Fig. 4. $f_p$ is the primary resonant frequency between $L_r$ and $C_r$. Boundary between zero current switching (ZCS) and ZVS regions is also marked in the figure. ZVS region could be further divided into two regions: (a) ZVS region 1 ($f < f_p$); and (b) ZVS region 2 ($f > f_p$).

In order to be adaptive to the wide voltage variation of the

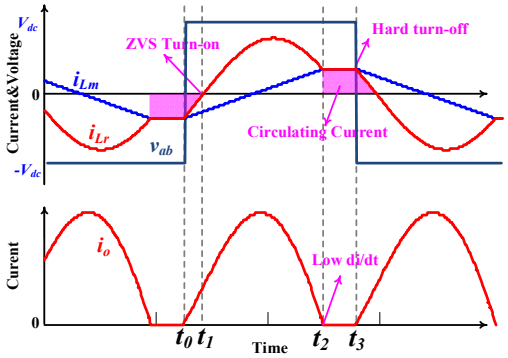


Fig. 5. Simulated waveforms of LLC stage operating in ZVS region 1.

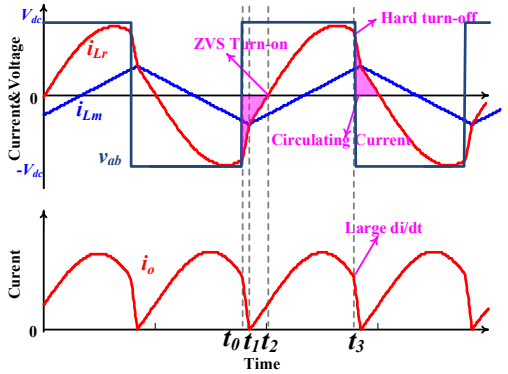


Fig. 6. Simulated waveforms of LLC stage operating in ZVS region 2

battery pack, LLC converter must be designed such that its operating region covers both the maximum and minimum battery voltage. This means that the converter operates in both ZVS region 1 and ZVS region 2 during the charging process. Accordingly, the switching frequency varies in a wide range to regulate the output voltage to follow the battery pack voltage.

Fig. 5 shows the simulated waveforms of LLC resonant converter operating in ZVS Region 1, in which the resonant tank input voltage $v_{ab}$, resonant inductor current $i_{Lr}$, magnetizing inductor current $i_{Lm}$, output current $i_o$ waveforms are given.

In the time interval [$t_2$, $t_3$), secondary diodes $D_6$-$D_9$ are reverse biased and the transformer is disabled, which enables $L_m$ to participate into the resonance with $L_r$ and $C_r$. $i_{Lr}$ is

circulating within the resonant network without delivering any power to the load. This circulating current causes additional conduction losses. These losses are related to the switching frequency, and greatly increase as the switching frequency is varied away from the primary resonant frequency.

Fig. 6 shows the simulated waveforms of LLC resonant converter operating in ZVS Region 2. At $t_o$, $S_3$ and $S_4$ are turned off with a high turning off current, which cause high switching losses. In the time interval [$t_0$, $t_1$), secondary diodes $D_7$ and $D_8$ are turned off fast with a high $di/dt$, which causes high reverse recovery losses.

Fig. 7 shows the simulated waveforms of LLC resonant converter operating at $f_p$. At $t_0$, $S_3$ and $S_4$ are turned off with hard switching. However, the turning off current is much smaller than operating in ZVS region 2. At $t_1$, $S_2$ and $S_5$ are turned on; $D_{S2}$ and $D_{S5}$ are turned off; both are ZVS. At $t_2$, $D_6$ and $D_9$ are turned off at zero current with low $di/dt$. Consequently, reverse recovery losses from the secondary diodes are eliminated.

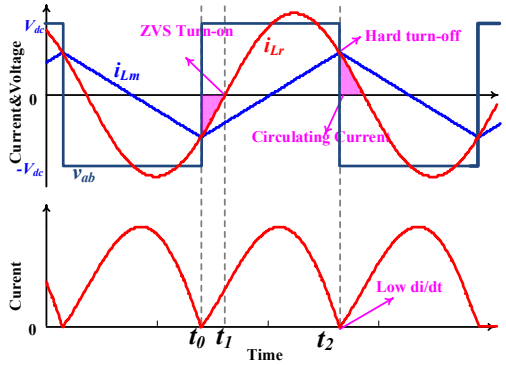


Fig. 7. Simulated waveforms of LLC converter operating at $f_p$.

At $f_p$, LLC converter has minimum circulating energy in the resonant tank, which corresponds to the lowest conduction losses. The conduction losses at resonant frequency are much smaller than conduction losses at ZVS Region 1. Meanwhile, the switching losses at resonant frequency are much smaller than that of ZVS Region 2. It can be concluded that operating LLC converter at primary resonant frequency corresponds to the minimum losses and the maximum conversion efficiency.

### *B. Proposed maximum efficiency point tracking technique*

Control diagram of proposed isolated charger based on SPEIC and full bridge LLC topologies is plotted in Fig. 8. The PFC outer voltage loop reference is obtained from the battery voltage and forced to follow the variation of the battery voltage. The reference voltage increases gradually with the increase of state of charge (SoC) and always follows,

$$V_{dc} = n(V_{bat} + 2V_D) \tag{1}$$

where, n is the turn ratio of the transformer; $V_d$ is the diode forward voltage drop.

With this control methodology, the LLC converter would automatically tune its switching frequency to be close to the primary switching frequency by the adopted parallel double control loops. Thus, the maximum efficiency point can be continuously tracked, and the efficiency of the circuit across the wide output voltage range can be enhanced.

A SoC algorithm is utilized to detect the SoC of the battery pack. In the pre charge mode and constant current charging mode, the current control loop is activated. Different current reference is generated from the SoC algorithm to regulate the charging current to be 0.1C and 1C, respectively. Output current is sensed and compared with the reference current through an error amplifier. The error is compensated through a PI compensator and fed to the voltage controlled oscillator. The dead-band block is used to convert the frequency signal

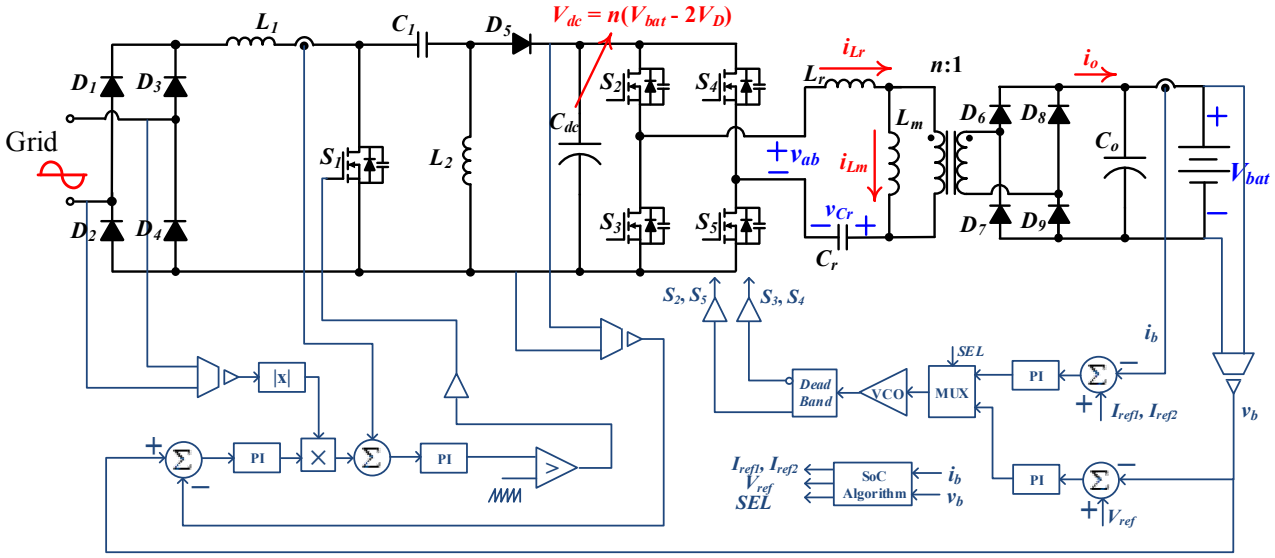


Fig .8. Control diagram of proposed isolated charger based on SPEIC and full bridge LLC topologies.

to two complementary gate drive signals with specific dead-band time. In the constant voltage charging mode, the voltage control loop is activated. Control of constant voltage operation is similar to that of the constant current operation. When the charging current degrades to 0.02 C, the charging is completed and the charger is disabled.

## III. Circuit Modeling and Loss Analysis

### A. Circuit Modeling

At $f_p$, the resonant tank $L_r$ and $C_r$ in LLC topology operate as a band pass filter (BPF). The full bridge operates as a square wave generator. Since the diodes in the secondary rectification bridge also operate complimentarily, the primary side of the transformer can be modeled as a square wave signal. The equivalent circuit model of LLC converter at resonant frequency is plotted in Fig. 9.

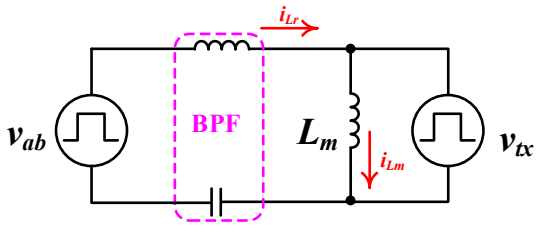


Fig. 9. Equivalent circuit model of LLC converter at resonant frequency.

Due to the band pass filtering effect, only the fundamental frequency component of the square wave signal is allowed to pass. Fig. 10 provides the waveforms of $i_{Lm}$ and $i_{Lr}$ in a single switching period.

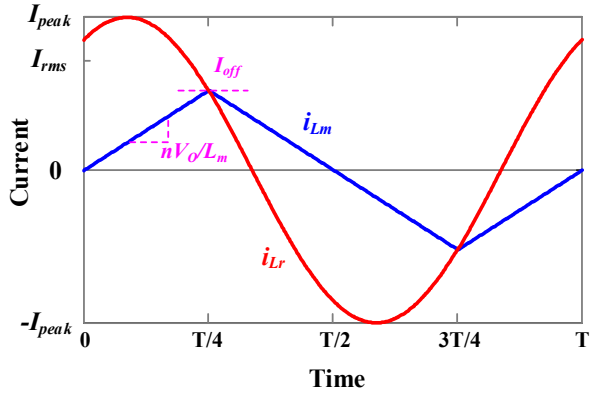


Fig. 10. Resonant tank current waveform at resonant frequency.

According to Fig. 10, from $t$ = 0 to $t$ = $T$/4, $i_{Lm}$ increases linearly with a rate of $nV_{bat}/L_m$. Thus, the turning off current of MOSFETs could be calculated as,

$$I_{off}=\frac{nV_{bat}T}{4L_m} \tag{2}$$

From $t$ = $T$/4 to $t$ = 3$T$/4, according to the law of energy conservation, the energy from the dc link is equal to the energy consumed by the load. In other words, the energy of the dc link is transferred to the load. Thus,

$$\int_{T/4}^{3T/4} i_{Lr}V_{dc}dt=V_{bat}I_{bat}\frac{T}{2} \tag{3}$$

$i_{Lr}$ is a sinusoidal function. Assuming the initial phase of $i_{Lr}$ is $\phi$, and the peak current is denoted by $I_{peak}$, $i_{Lr}$ can be represented as,

$$i_{Lr}(t)=I_{peak}\sin\left(\frac{2\pi}{T}t+\phi\right) \tag{4}$$

Since $i_{Lr}(T/4) = I_{off}$, $\phi$ can be obtained,

$$\phi=\arccos\frac{I_{off}}{I_{peak}} \tag{5}$$

Combing equations (3)–(5), $I_{peak}$ can be obtained as,

$$I_{peak}=\sqrt{\frac{n^2V_{bat}^2T^2}{16L_m^2}+\frac{\pi^2V_{bat}^2I_{bat}^2}{4V_{dc}^2}} \tag{6}$$

Since $V_{dc} \approx nV_{bat}$, the rms current can be derived as,

$$I_{rms}=\frac{I_{peak}}{\sqrt{2}}=\sqrt{\frac{n^2V_o^2T^2}{32L_m^2}+\frac{\pi^2I_{bat}^2}{16n^2}} \tag{7}$$

### B. Loss Analysis

Typically, three critical losses must be considered when analyzing the losses of LLC topology, which are a) conduction losses, b) switching losses and c) core losses from the magnetic components.

Conduction losses can be calculated as,

$$P_{cond}=\sum_{k=1}^{n}R_{k,esr}I_{k,rms}^2+4V_DI_{D,rms} \tag{8}$$

where $R_{k,esr}$ is the equivalent series resistance of each conducting component; $V_D$ is the voltage drop across each secondary diode; $I_{D,rms}$ is the rms current of the secondary diode. According to Eq. (7), $I_{k,rms}$ is a function of $L_m$. The larger $L_m$ is, the smaller $I_{rms}$ becomes; while smaller $I_{rms}$ corresponding to smaller conduction losses. Thus, conduction losses from the primary side could be reduced by increasing $L_m$.

Total turning off losses of the four primary MOSFETs can be approximated based on

$$P_{off}=\frac{(I_{off}t_{fall})^2f}{6C_{HB}}=\frac{n^2t_{fall}^2V_{bat}^2T}{96L_m^2C_{HB}} \tag{9}$$

where, $t_{fall}$ is the fall time, and $C_{HB}$ is the equivalent capacitance in the half-bridge. According to Eq. (9), $P_{off}$ is a function of $L_m$. The larger $L_m$ is, the smaller $P_{off}$ becomes. Thus, turning off losses from the primary MOSFETs could also be decreased by increasing $L_m$.

Since there are two magnetic components, namely resonant inductor and transformer, the core losses should be analyzed separately, which can be calculated as,

$$P_{fe}=kf^x\Delta B^y \tag{10}$$

where $k$, $x$, $y$ are coefficients determined by the core types and materials. $\Delta B$ is the flux density variation. According to Eq. (10), since $f_p$ is preset, core losses are mainly determined by $\Delta B$. For resonant inductor $L_r$, $\Delta B$ is calculated as,

$$\Delta B_{Lr} = \frac{L\Delta i}{2n_{Lr}A_e} = \frac{LI_{peak}}{n_{Lr}A_e} = \frac{L}{n_{Lr}A_e}\sqrt{\frac{n^2V_{bat}^2T^2}{16L_m^2} + \frac{\pi^2V_{bat}^4}{4R_L^2V_{dc}^2}} \quad (11)$$

where, $A_e$ is the effective cross-section area of the ferrite core; $n_{Lr}$ is the number of turns winded on the core, $\Delta i$ is the variation of current. According to equations (10) and (11), for a specific design, the resonant inductor core losses are determined by $L_m$. The larger $L_m$ is, the smaller core losses become. Thus, core losses from the resonant inductor could be reduced by increasing $L_m$.

In the case of a transformer, $\Delta B$ is calculated as,

$$\Delta B_{TX} = \frac{\lambda_p}{2n_{TX,p}A_e} = \frac{nV_{bat}T}{4n_{TX,p}A_e} \quad (12)$$

where, $\lambda_p$ is the volt-second on the primary side of the transformer; and $n_{TX,p}$ is the number of turns on the primary side of the transformer. According to Eq. (12), core loss of a transformer is not a function of any of the resonant parameters ($L_m$, $L_r$, and $C_r$). It could be optimized by minimizing the total ferrite losses and copper losses of the transformer.

From the analysis, $L_m$ is the most critical parameter in designing the parameters of LLC resonant network. Typically, maximizing the value of $L_m$ while keeping the ZVS feature of primary MOSFETs could minimize the primary side conduction losses, reduce primary side MOSFETs turning off losses, and the transformer core losses.

## IV. Efficiency Comparison

In order to make a comprehensive comparison, two 3.3 kW rated LLC stages compatible with 100 V to 420 V battery pack voltage are designed. The design parameters are summarized in Fig. 11. Both designs have their $f_p$ equal to 200 kHz.

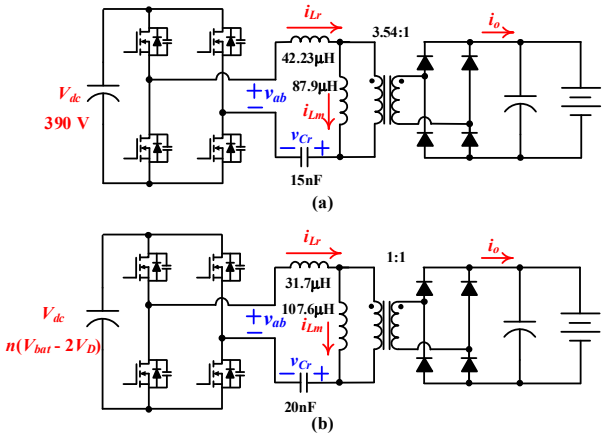


Fig. 11. Circuit parameters for efficiency comparison, (a) conventional fixed dc link voltage, (b) proposed variable dc link voltage.

Circuit performances at the lowest battery pack voltage (Point A in the charging profile: $V_{bat}$ = 100 V, $I_{bat}$ = 0.79 A) for both circuits are compared in Fig. 12; both the turning off current and circulating current are marked. According to Fig. 12, the turning off current of conventional LLC converter is 4.3 A, while the proposed LLC converter has turning off current equal to 1.2 A. This shows that switching losses are significantly reduced in the LLC converter with the proposed

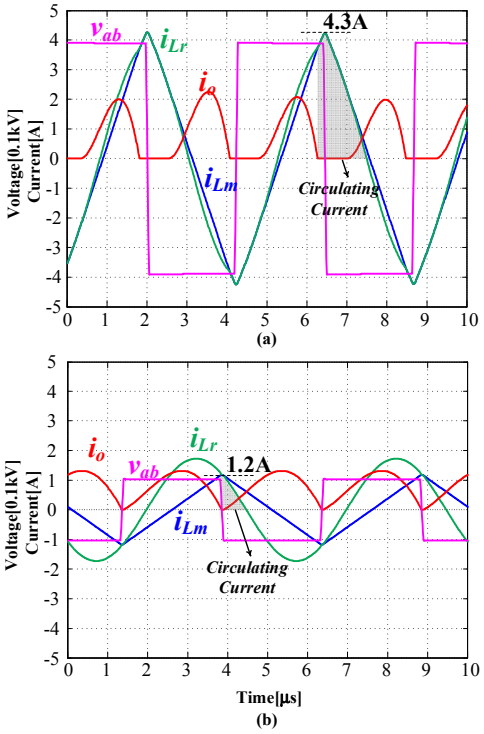


Fig.12. LLC converter performance comparison at the operating point A; a) conventional; b) proposed.

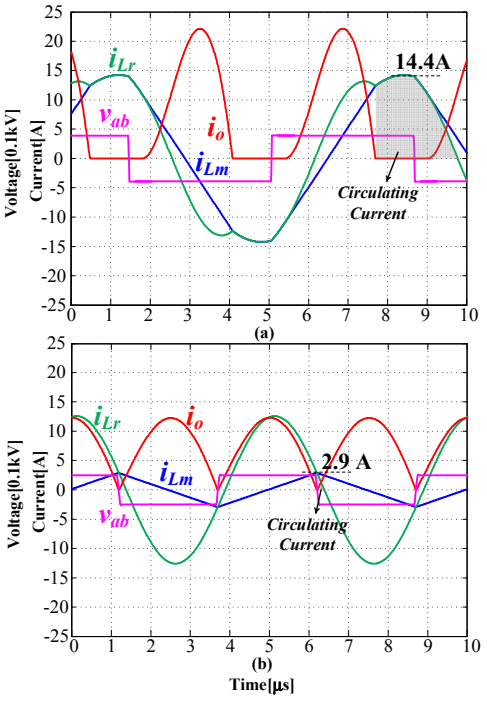


Fig. 13. LLC converter performance comparison at the operating point B; a) conventional; b) proposed.

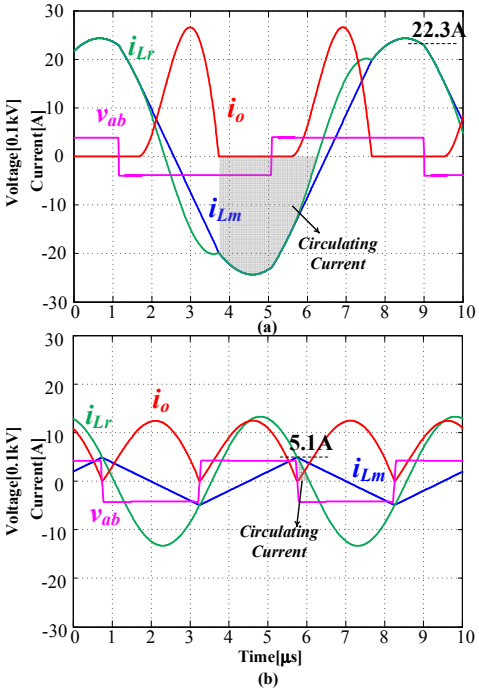


Fig. 14. LLC converter performance comparison at the operating point C; a) conventional; b) proposed.

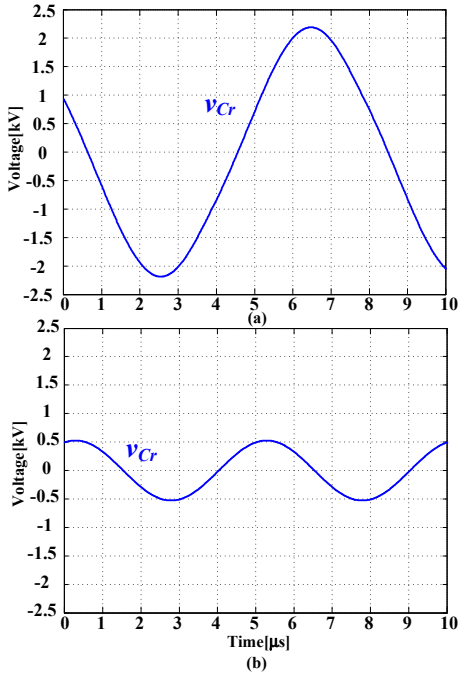


Fig. 15. Resonant capacitor voltage stress comparison at the operating point C; a) conventional; b) proposed.

approach in comparison to that of the conventional fixed dc link voltage approach. Moreover, the circulating current in the proposed circuit is much smaller than that of the conventional one.

Similarly, circuit performances in the beginning of constant current charging mode (Point B in the charging profile: $V_{bat}$ = 250 V, $I_{bat}$ = 7.86 A) are compared in Fig. 13.

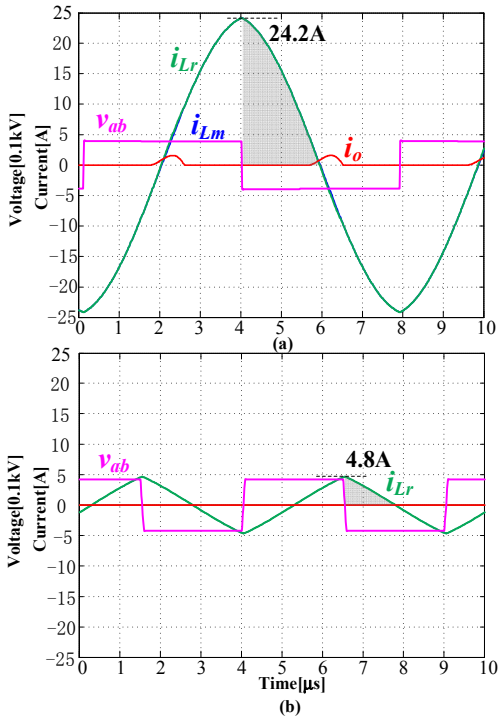


Fig. 16. LLC converter performance comparison at the operating point D; a) conventional; b) proposed.

In comparison to conventional approach, the turning off current is reduced from 14.4 A to 2.9 A. Circulating current is significantly reduced. Moreover, the current stress on the rectifier diodes is also greatly reduced.

Fig. 14 demonstrates the circuit operation at the peak power (Point C in the charging profile: $V_{bat}$ = 420 V, $I_{bat}$ = 7.86 A). In comparison to conventional approach, the turning off current is reduced from 22.3 A to 5.1 A. Circulating current is significantly reduced. The current stress on the rectifier diodes is also greatly reduced.

Fig. 15 demonstrates the voltage stress on $C_r$ at the peak power (Point C in the charging profile: $V_{bat}$ = 420 V, $I_{bat}$ = 7.86 A). In comparison to conventional approach, voltage stress on $C_r$ is greatly reduced from 2.2 kV to 0.51 kV. Practically, it is unrealistic to build a single film capacitor with 2.2 kV high frequency ac voltage rating. A film capacitor bank with multiple series capacitors must be used, which makes the resonant capacitor bulky.

Fig. 16 demonstrates the circuit operation at the lightest load (Point D in the charging profile: $V_{bat}$ = 420 V, $I_{bat}$ = 0.16 A). In comparison to conventional approach, the turning off current is reduced from 24.2 A to 4.8 A. The current stress on the rectifier diodes is also greatly reduced. For the conventional approach [see Fig. 16 (a)], although little power (67.2 W) is delivered to the battery, there is still a significant amount of circuiting current in the resonant tank. The circuiting power makes the conduction losses much higher than the power delivered.

According to the simulation data and the loss analyses described in the previous subsection, the switching losses,

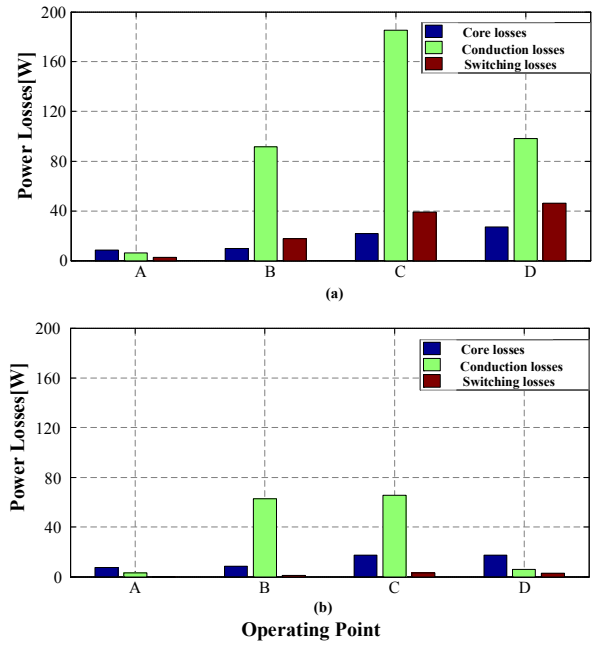

Fig. 17. Loss breakdown; a) conventional LLC converter; b) proposed LLC converter.

conduction losses, as well as core losses are calculated for the four operating points. The loss breakdown is plotted in Fig. 17. As shown in Fig. 17, both the conduction losses and switching losses are obviously reduced. At full load point (Point C: P = 3.3 kW), the conversion efficiency is improved from 93.0% to 97.4% (4.4 % improvement). At the lightest load condition (Point D: P = 6.62 W) the conversion efficiency is improved from 3.7% to 20.2% (16.5% improvement).

## V. Conclusion

In this paper, a two stage PEV battery charger based on SPEIC PFC and LLC topologies is proposed. A new control approach based on maximum efficiency point tracking technique is proposed for LLC based PEV battery chargers. With this proposed technique, dc link voltage always follows the variation of the battery pack voltage; which ensures that LLC converter is always operating close to the primary resonant frequency.

Detail modeling and loss analyses are provided for LLC converter operating at the resonant frequency. The effectiveness of the designed LLC converter with variable dc link control is experimentally compared to the one adopting a fixed dc link voltage. The simulation results show that the efficiency of the LLC converter can be improved by 4.4 % at the heaviest load condition and 16.5% at the lightest load condition.

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