Interleaved SEPIC PFC Converter Using Coupled Inductors in PEV Battery Charging Applications

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***Abstract*—In ac/dc power factor correction (PFC) applications, where a wide range dc link voltage is required, boost derived topologies are no longer the most suitable circuit topologies for universal grids. In this paper, an interleaved SEPIC PFC converter, capable of providing a wide range dc link voltage, is investigated for onboard isolated battery chargers for plug-in electric vehicle (PEV) applications. The proposed converter is well adapted to achieve the maximum efficiency point tracking of the second stage LLC topology of an onboard isolated charger. Coupled inductors are utilized to reduce the component count and to bring the benefits of reduced input ripple current, lower switching losses, less total harmonic distortion (THD), and resistance to duty cycle mismatch. A 3.3 kW interleaved and coupled SEPIC converter, generating 200V-420V dc link voltages from the universal grid, is designed and simulated to verify the proof of concept.**

Keywords—Coupled inductors, interleaved, PEV charging, PFC, SEPIC.

I. INTRODUCTION

Full bridge isolated LLC dc/dc topology has gained popularity in two stage onboard plug-in electric vehicle (PEV) battery charging applications [1]–[5]. This is mainly due to its attractive features, such as zero voltage switching and wide output voltage range [6], [7]. In [8], a maximum efficiency point tracking technique was proposed for a LLC based PEV charger. Fig. 1 illustrates the architecture of a full bridge LLC based PEV charger using the maximum efficiency point tracking technique. By making the dc link voltage variable to follow the battery pack voltage, the LLC topology can be constrained to operate in the vicinity of its resonant frequency, where the circuit losses are minimized.

In the conventional approaches, boost type (boost, interleaved boost, bridgeless boost) topologies are commonly used as the ac/dc PFC converter [9]–[13]. However, when using the maximum efficiency point tracking technique, boost type topologies are no longer suitable, because the varying dc link voltage might become lower than the grid side input voltage. Typically, this scenario happens when the battery state of charge is low and the charger is connected to a 240 V grid. Therefore, SEPIC topology, which can either boost or buck the input voltage, becomes a more suitable candidate to be deployed as the front-end ac/dc PFC converter [14], [15].

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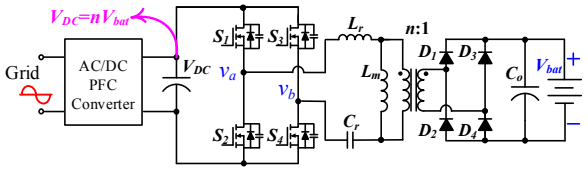

Fig.1. Architecture of a two stage PEV charger based on maximum efficiency point tracking technique of LLC topology.

A single phase SEPIC PFC converter is suitable for use at low power levels. In higher power applications, the current stresses on circuit components can become excessive. Paralleling multiple power semiconductor devices would reduce the current stress of each individual device. However, power diodes are not suitable to be operated in parallel. This is because their on-resistance and forward voltage-drop exhibit negative temperature coefficients [16]. If paralleled, the mismatch of power diodes would cause one diode to carry more current than the other. As the diode carrying more current becomes hotter, the current mismatch becomes larger until the hotter diode eventually takes over the majority of the current. Moreover, the high current stress makes the inductors bulky and difficult to design.

In order to cope with those challenges, an interleaved SEPIC PFC converter utilizing the maximum efficiency point tracking technique is proposed for PEV battery charging applications. This interleaved converter is able to process more power with reduced circuit ripples and harmonics distortion. Additionally, because the coupled inductors share a common magnetic core, the count of magnetic devices is kept the same as the single-phase topology. Moreover, using coupled inductors effectively solves the current sharing problems caused by the duty cycle mismatch.

This paper is organized as follows. Section II introduces the proposed circuit and explains its modes of operation in CCM and DCM. Section III details the attractive features of the proposed interleaved SEPIC converter using coupled inductors. The simulation results are presented and evaluated in Section IV. Finally, Section V summarizes the study.

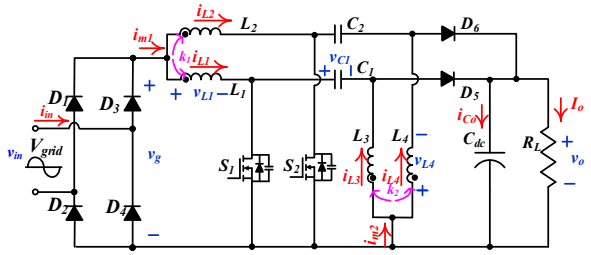

Fig. 2. Proposed interleaved SEPIC PFC converter.

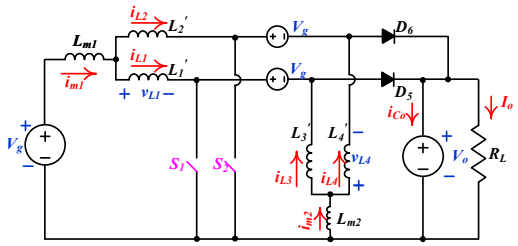

Fig. 3. Equivalent circuit of the converter.

II. OPERTING PRINCIPLE

A. Circuit Description

In the interleaved configuration, we parallel n SEPIC cells, and artificially shift the phase of the gate signals by $2\pi/n$. This paper uses a two phase interleaved SEPIC converter as a case study. Circuit analysis can be expanded to multi-phase situations. The schematic of a two phase interleaved SEPIC PFC converter using coupled inductors is plotted in Fig. 2. Inductors L_1 and L_2 are closely coupled with the same winding orientation. The coupling factor is k_1. Inductors L_3 and L_4 are closely coupled with the same winding orientation. The coupling factor is k_2.

The equivalent circuit of the interleaved SEPIC converter is plotted in Fig. 3. Each coupled inductor is equivalent to three independent inductors [17]. Assuming $L_1 = L_2$, and $L_3 = L_4$, the relationships of the inductors are described by the following equations,

$$L_{m1} = k_1 L_1 \tag{1}$$

$$L_1' = L_2' = (1-k_1)L_1 \tag{2}$$

$$L_{m2} = k_2 L_3 \tag{3}$$

$$L_3' = L_4' = (1-k_2)L_3 \tag{4}$$

where, L_{m1}, L_{m2} are the mutual inductances; L_1', L_2', L_3', and L_4' are the leakage inductances as shown in Fig. 3.

Assuming the values of SEPIC coupling capacitors (C_1 and C_2), as well as and the output filter capacitor (C_{dc}) are large enough, the ripple voltage on these capacitors can be neglected in steady state operation. Therefore, the capacitors can be replaced by equivalent voltage sources, as demonstrated in Fig. 3. It should be noted that in steady state, the average voltages on inductors is zero. Thus, according to the principle of KVL,

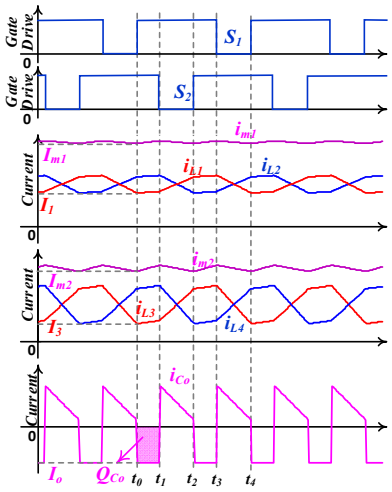

Fig. 4. Circuit waveforms of the converter in CCM.

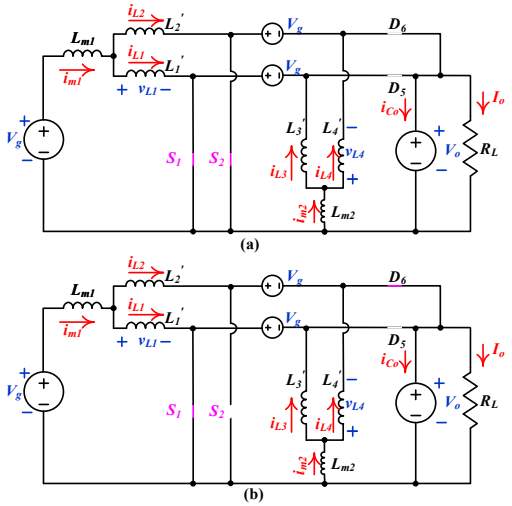

Fig. 5 Equivalent circuits of the converter in CCM; (a) Mode I; (b) Mode II

the dc voltages on SEPIC inductors must be equal to the input voltage, V_g. Modes of operation in CCM

Fig. 4 provides the circuit waveforms of the converter when the duty cycle is greater than 0.5. As marked in the figure, each switching cycle is associated with four operating modes. Due to the symmetry of the topology operation, only two operation modes during half of the switching period are discussed.

1) Mode I (t_0-t_1 in Fig 4):

At t_{o-}, MOSFET S_1 is off and MOSFET S_2 is on. Diode D_5 is on and diode D_6 is off. At t_o, S_1 is turned on and D_5 is turned off. Both i_{L1} and i_{L2} increase at the same rate, as expressed by

$$\frac{di_{L1}}{dt} = \frac{di_{L2}}{dt} = \frac{V_g}{(1+k_1)L_1} \tag{5}$$

Both L_3 and L_4 are energized by the SEPIC coupling capacitor. i_{L3} and i_{L4} are derived as,

$$\frac{di_{L3}}{dt}=\frac{di_{L4}}{dt}=\frac{V_g}{(1+k_2)L_3} \tag{6}$$

According to equations (5) and (6), the rates at which i_{L1}, i_{L2}, i_{L3}, and i_{L4} varies is smaller than the rates at the non-coupled interleaved condition (V_g/L_1 and V_g/L_3). The larger the coupling factor is, the slower the varying speed becomes. Since the input current is equals to the sum of i_{L1} and i_{L2}, the input current ripple can be calculated as,

$$\Delta i_{m1}=\frac{(d-0.5)T_sV_g}{(1+k_1)L_1} \tag{7}$$

2) Mode II (t_1-t_2 in Fig 4):

At t_1, MOSFET S_2 is turned off and MOSFET S_2 is kept on. Diode D_6 is *turned* on and diode D_5 is *kept* off. The circuit enters into *Mode II*. i_{L1} increases at the rate of,

$$\frac{di_{L1}}{dt}=\frac{V_g+k_1V_o}{\left(1-k_1^2\right)L_1} \tag{8}$$

While i_{L2} decreases at the rate of,

$$\frac{di_{L2}}{dt}=-\frac{k_1V_g+V_o}{\left(1-k_1^2\right)L_1} \tag{9}$$

According to Eq. (9), the current ripple on each individual inductor can be calculated as,

$$\Delta i_{L1}=\frac{\left(k_1V_g+V_o\right)(1-d)T_s}{\left(1-k_1^2\right)L_1} \tag{10}$$

With regard to the non-coupled interleaved condition, the current ripple in L_1 is,

$$\Delta i_{L1,non}=\frac{V_o(1-d)T_s}{L_1} \tag{11}$$

Comparing equations (10) and (11), one can tell that the coupled condition has much larger current ripple on each individual inductor. According to Eq. (10), the larger the coupling factor is, the larger the current ripple on the individual inductor becomes. Similarly, the smaller d is, the larger the current ripple on the individual inductor becomes. When the coupling factor is large enough and the duty cycle is small enough, the current ripple on individual inductor exceeds the peak current, which forces the individual branch to enter into discontinuous conduction mode (DCM). It should be noted that the overall input current, i_{Lm1}, is still continuous in this condition. The similar analysis applies to i_{L3} and i_{L4}, and similar conclusion can be made.

B. Modes of operation in DCM

Fig. 6 provides the circuit waveforms of the converter when individual branch enters into DCM while the overall circuit maintains CCM. As can be seen in Fig. 6, each switching cycle is associated with six operating modes. Due to the symmetry of the topology operation, only three operation modes during half of the switching period are discussed.

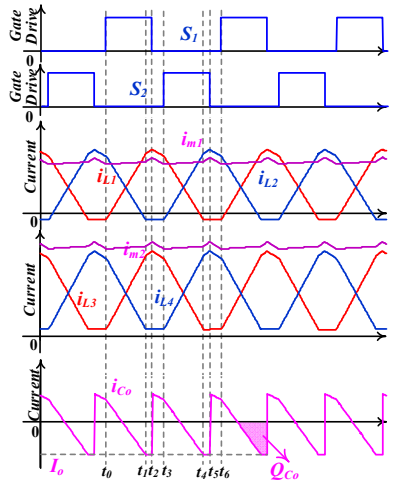

Fig. 6. Circuit waveforms of the converter in DCM.

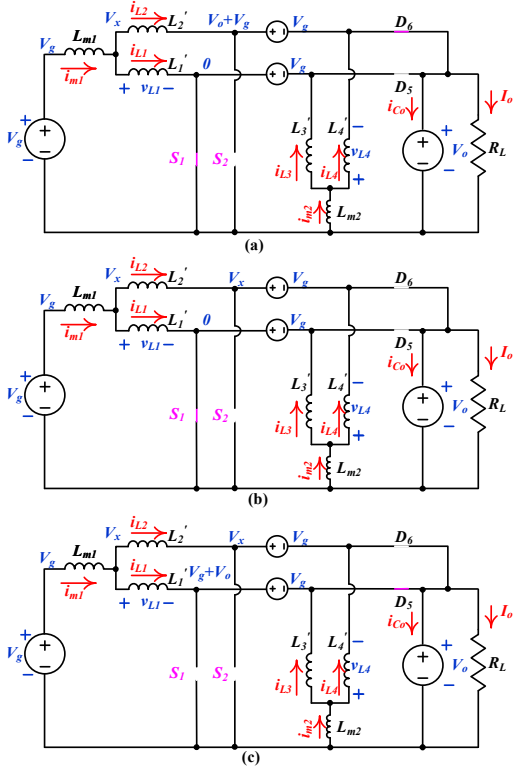

Fig. 7 Equivalent circuits of the converter in DCM; (a) Mode I; (b) Mode II; (c) Mode III.

1) Mode I (t_0-t_1 in Fig 6): At t_o-, MOSFETs S_1 and S_2 are both off. Diode D_5 is off, while D_6 is on. i_{L1} is a small negative value while i_{L3} is a small positive value. This means that there is a small current flowing through the path (L_3->C_1->L_1). At t_o, S_1 is turned on and the circuit enters into *Mode I*. Its equvalent circuit is ploted in Fig. 7(a).

It should be noted that Fig. 7(a) agrees with the Mode II which has been discussed in Section II-B. Therefore, during

Mode I, i_{L1} varies following Eq. (8). Similarly, i_{L2} varies following Eq. (9).

2) Mode II (t_1-t_2 in Fig 6):

At t_2, D_6 turns off at zero current and the circuit enters into *Mode II*. The equivalent circuit is plotted in Fig. 7(b). In *Mode II*, S_1 is the only semiconductor device kept on in the interleaved SEPIC topology. The current in L_2 and L_4 is a constant as,

$$-i_{L2} = i_{L4} = const \tag{12}$$

i_{L1} increases at the rate of,

$$\frac{di_{L1}}{dt} = \frac{V_g}{L_1} \tag{13}$$

While i_{L3} increases at the rate of,

$$\frac{di_{L3}}{dt} = \frac{V_g}{L_3} \tag{14}$$

3) Mode III (t_2-t_3 in Fig 6):

At t_2, S_1 is turned off and the circuit enters into *Mode III*. The equivalent circuit is plotted in Fig. 7(c). In *Mode III*, D_5 is the only semiconductor device kept on in the interleaved SEPIC topology. The current in L_2 and L_4 is a constant following Eq. (12).

i_{L1} decreases at the rate of,

$$\frac{di_{L1}}{dt} = -\frac{V_o}{L_1} \tag{15}$$

While i_{L3} decreases at the rate of,

$$\frac{di_{L3}}{dt} = -\frac{V_o}{L_3} \tag{16}$$

III. Circuit Features

Compared with the single phase SEPIC topology as well as the non-coupled interleaved SEPIC topology, the proposed configuration using coupled inductors demonstrates some attractive features which is detailed in this section.

A. Reduced current ripple and THD

The first benefit of the proposed architecture comes from its reduced input current ripple and reduced THD. This is mainly due to two reasons: (a) the inductor current ripples in each individual SEPIC branch cancel with each other on the input side; The current ripple cancellation effect can be clearly observed in on the waveform of i_{m1} in Fig. 4. (b) The rate at which the current varies is much lower than the non-coupled configuration, which is well demonstrated from equations (10) and (11). Due to the reduced current ripple, the harmonics components are also significantly reduced. Therefore, the proposed circuit is featured with reduced THD.

B. Reduced switching losses

The semiconductor switching losses are also effectively reduced. In CCM, This can be demonstrated by taking

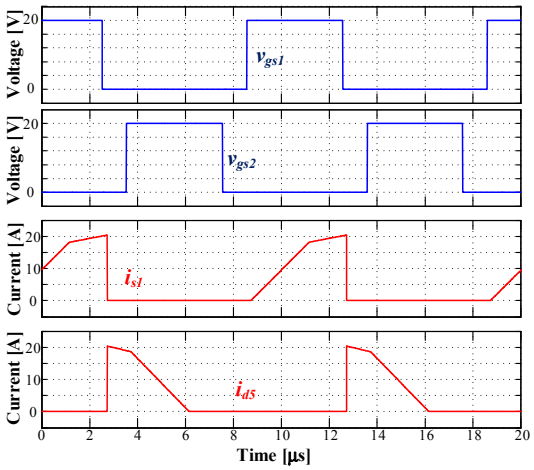

Fig. 8. Simulated MOSFET and diode currents waveforms in DCM.

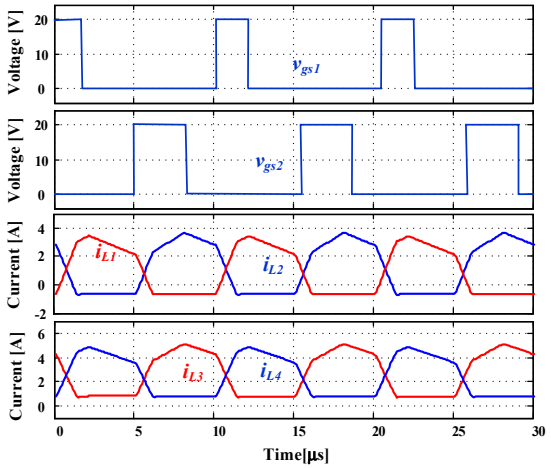

Fig. 9. Simulated results with mismatched duty cycles.

MOSFET S_1 and diode D_5 as an example. When the MOSFET S_1 is on, its drain to source current is $i_{S1} = i_{L1} + i_{L3}$. Similarly, when the diode D_5 is on, its forward current is also $i_{D5} = i_{L1} + i_{L3}$. According to Fig. 4, at t_0, inductor currents i_{L1} and i_{L3} both reach their lowest values, I_1 and I_3, respectively. Therefore, S_1 is turned on while D_5 is turned off at current $I_1 + I_3$, which is much smaller than half of the sum of i_{m1} and i_{m2} at this moment $[(I_{m1}+I_{m2})/2]$. This small transition current means small turning on losses of the power MOSFET and small turning off losses of the power diode, which are the dominant switching losses.

This switching losses reduction is also valid for DCM operation. In DCM operation, i_{L1} and i_{L2} are discontinuous while the input current (i_{m1}) is still continuous. The gate drive waveforms (v_{gs1}, v_{gs2}) and simulated current waveforms (i_{S1} and i_{D5}) are plotted in Fig. 8. According to Fig. 8, MOSFET S_1 is turned on at zero current, which means the turning on losses of power MOSFETs are reduced. Diode D_5 is turned off at zero current. Therefore, the reverse recovery losses of power diodes are eliminated.

TABLE I

DESIGN PARAMETERS OF THE PROPOSED CONVERTER

Quantity	Symbol	Parameter
Input voltage	v_{in}	85V-265V, 50Hz-60Hz
Output voltage	V_{out}	200V-420V
Rated power	P_{max}	3.3 kW
Input inductor	L_1, L_2	600 µH
Input mutual inductance	L_{1m}	480 µH
SEPIC capacitance	C_1, C_2	10 µF
Output inductor	L_3, L_4	480 µH
Output mutual inductance	L_{3m}	380 µH
Output capacitor	C_{dc}	2 mF
Switching frequency	f_s	100 kHz

C. *Reduced output voltage ripple*

Interleaving effect also brings the benefit of smaller output voltage ripple at the switching frequency. It should be noted that the switching frequency output voltage ripple is equal to the stored charge variation on the output capacitor divided by its capacitance. For single phase SEPIC converter in continuous conduction mode, the output voltage ripple is dT_sI_o/C_o. For interleaving SEPIC converter, in CCM operation, the voltage ripple can be derived as $(d - 0.5)T_sI_o/C_o$, which is much smaller than the voltage ripple of single phase converter. In the DCM operation, the output voltage ripple can be approximated as $T_sI_o/4C_o$, which is also smaller than that of the single phase converter. This reduced output voltage ripple represents reduced RMS current on the output capacitor. This can be translated into reduced conduction losses, reduced heat dissipation, and better system reliability.

D. *Resistivity to duty cycle mismatch*

Interleaving using coupled inductors also brings the benefit of the resistance to duty cycle mismatch. This could be clearly be observed in Fig. 9. The duty cycle of MOSFET S_1 is 0.2, while the duty cycle of MOSFET S_2 is 0.4. However, the differences between the inductors currents are almost negligible.

IV. RESULTS

In order to verify the proof of concept and the previous theoretical analysis, a 3.3 kW converter is designed and simulated. Design parameters are summarized in Table I. Both coupled inductors have their coupling factor equals to 0.8. The simulation is carried out assuming ideal switches.

Fig. 10 provides the simulation results when the circuit converts 120 V, 60 Hz grid voltage to 420 Vdc on the output. In this condition, the SEPIC topology operates in boost mode and the duty cycle is relatively large. According to the waveform of i_{L1}, the circuit is operating in CCM, which agrees with the theoretical analysis in Eq. (9). According to Fig. 10, the current ripples on i_{in}, is much smaller than the current ripples on i_{L1}. This well demonstrates the ripple cancellation effect. i_{in} is right in phase with v_{in}; unity power factor is

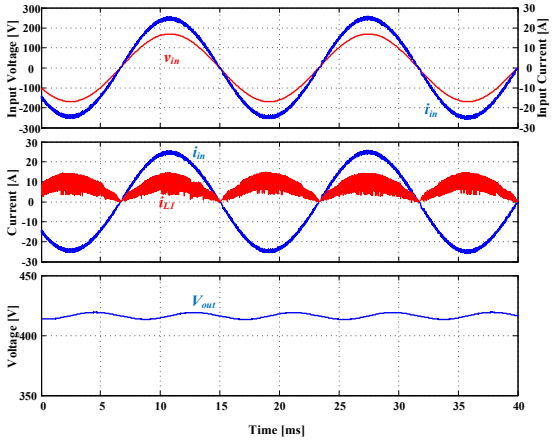

Fig. 10. Simulated waveforms for v_{in} = 120 Vac, V_o = 420 Vdc, and P_o = 1.6 kW.

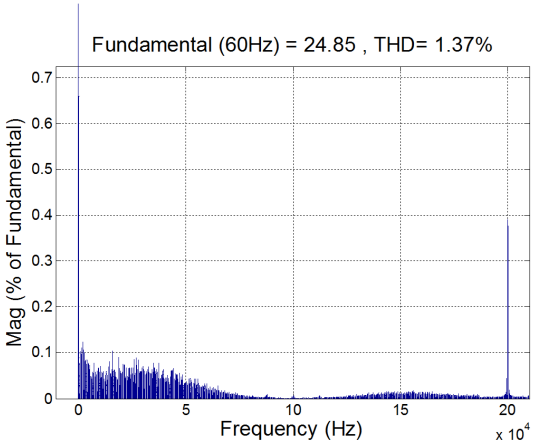

Fig. 11. FFT analysis for v_{in} = 120 Vac, V_o = 420 Vdc, and P_o = 1.6 kW.

demonstrated. Fig. 11 provides the FFT analysis of the circuit at this operating point. The total harmonic distortion (THD) is well suppressed to be 1.37%.

Fig. 12 provides the simulated waveforms when the converter gets power from 240 V, 60 Hz grid and the output voltage is 420 Vdc. The rated power (3.3 kW) is achieved at this operating point. Therefore, the electrical stresses of devices can be obtained through the simulation. According to Fig. 12, unity power factor is demonstrated. The THD is measured as 1.99%. i_{L1} is still in CCM, but its minimized value is close to cross zero. This is because the boost ratio is smaller than the previous scenario. Thus, the duty cycle is smaller. According to Eq. (9), this will push the circuit operation closer to DCM.

Fig. 13 provides the simulated waveforms when the circuit converters 240 V, 60 Hz grid voltage to 200 Vdc on the output. This corresponds to the occasion when the battery is low in state of charge [18]. According to Fig. 13, unity power factor is demonstrated. The THD is measured as 3.43%. The waveform of i_{L1} intersects with zero, which means the circuit enters into DCM. This is because the boost ratio is smaller than the previous scenario. Thus, the duty cycle is smaller. According to Eq. (9), this will push the circuit operation into DCM. In DCM

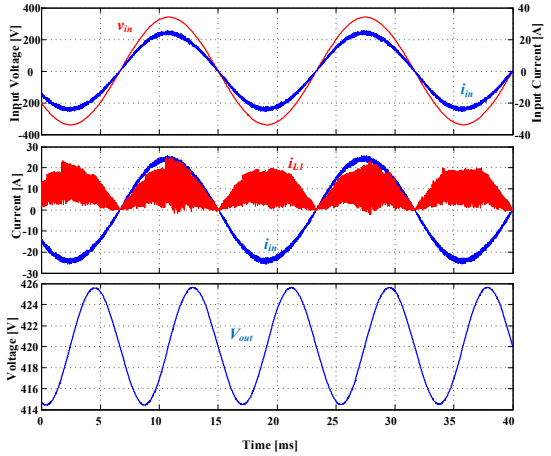

Fig. 12. Simulated waveforms for v_{in} = 240Vac, V_o =420Vdc, and P_o = 3.3 kW.

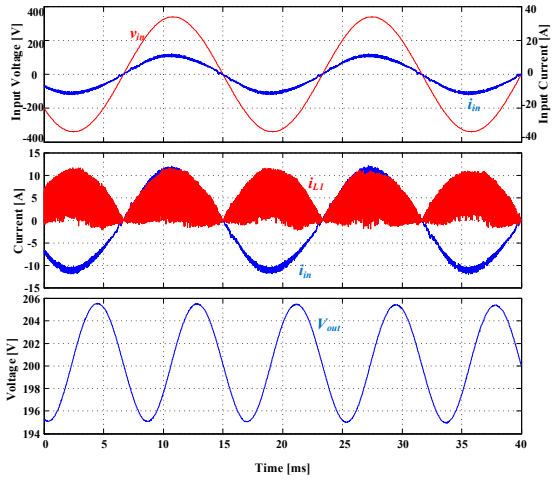

Fig. 13. Simulated waveforms for v_{in} = 240 Vac, V_o = 200 Vdc, and P_o = 1.5 kW.

operation, power MOSFETs are turned on at zero current, and the power diodes are turned off at zero current, which significantly reduces the switching losses and eliminate the reverse recovery losses.

V. CONCULSIONS

In this paper, an interleaved and coupled SEPIC converter is proposed for use with the maximum efficiency point tracking technique of LLC based onboard PEV chargers. This proposed converter offers the benefits of 1) reduced input ripple current; 2) reduced output ripple voltage; 3) less THD; 4) smaller switching losses; 5) zero current switching with a duty cycle less than 0.5; 6) resistance to duty cycle mismatch. A 3.3 kW converter prototype is designed and simulated to verify the proof of concept. The designed converter demonstrates unity power factor and low THD in different operation points in the PEV battery charging profile. The simulation results well agrees with the theoretical analysis. It is verified that small duty cycle and big coupling factor facilitate the converter to enter into DCM operation. Experimental verification of the proposed design approach lays out the future research direction.

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