A ZVS Integrated Single-Input-Dual-Output DC/DC Converter for High Step-up Applications

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***Abstract*—This paper presents a novel integrated dc/dc topology with a step-up output and a step-down output. A new control scheme is developed to regulate both outputs simultaneously. Compared with discrete configurations, the proposed integrated converter utilizes a lower number of switches due to the reuse of components. The converter characteristics are studied comprehensively. It is demonstrated that all MOSFETs are turned on at zero voltage with reduced switching losses. For the step-up stage, the converter provides a high boost ratio and is able to clamp the switch voltage spikes. For the step-down stage, the steady-state characteristics and the dynamic performances are similar to that of the conventional buck converter. Moreover, the step-down output port can be extended to multiple ports, where the single-input-multiple-output (SIMO) version of converter can be derived. A 250 W, 42 V to 390 V and 15 V converter prototype is designed, analyzed and tested. The experimental results are presented to verify the feasibility of the topology.**

Keywords—dc/dc converter; integrated converter; single-input-dual-output (SIDO); single-input-multiple-output; zero voltage switching.

I. INTRODUCTION

Multiple outputs dc/dc converters are used in a wide variety of applications, such as LED drivers [1], [2], dc nanogrids [3]–[5], portable devices [6], plug-in electric vehicles [7], multilevel inverters [8] and communication power supplies [9]. Among them, SIMO dc/dc converters have their advantage of reduced circuit complexity. Fig.1 (a) shows a typical system diagram with two discrete power stages. While Fig. 1 (b) shows an integrated dual output system implemented with a three port converter. In comparison with the discrete version, the integrated converter utilizes a lower number of switches due to the reuse of components. This leads to reduced switching losses and the removal of the redundant components.

Meanwhile, many applications such as high intensity discharge lamp ballast used in automotive headlamps, call for high step-up ratio converters [10]. The main challenges lie in a) how to extend the step-up ratio; and b) how to alleviate the voltage spikes across the switching devices introduced from the transformer leakage inductor [11].

A flyback-boost derived converter is proposed in [11]. The proposed topology provides a high voltage gain without incurring extreme duty ratios. However, the topology is only explored in single-input-single-output scenarios. In [12], the concept of SIMO was reported. A class of SIMO converters have been introduced in [13]–[16]. In [13], [14], some highly efficient SIMO dc/dc converters were proposed. However, only one active switch is employed. This makes it infeasible to regulate both outputs simultaneously. A SIMO dc/dc converter with reused switches [15] was proposed. However, it can only provide step-down outputs. This means that it is not an option for applications where step-up output is required. A family of SIMO dc/dc topologies with one step-up and multiple step-down outputs are proposed in [16]. However, the converter suffers from considerable switching losses due to the hard switching.

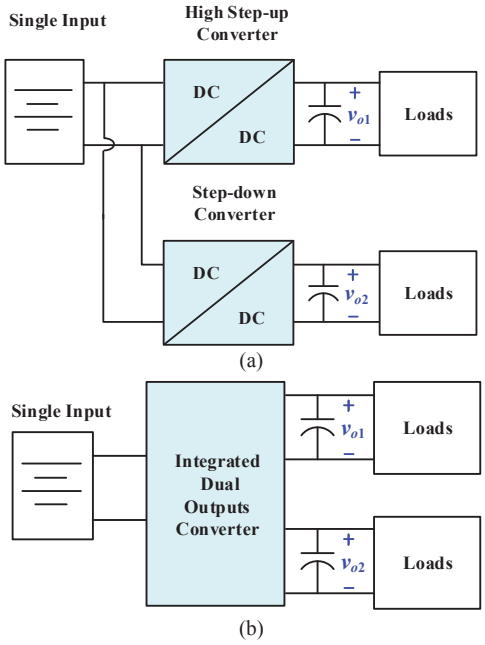

Fig. 1. Schematic of power converter architectures with dual dc outputs: (a) discrete version; (b) integrated version.

This paper proposes a novel integrated dual-output converter (as showed in the Fig. 2), which can provide one high step-up output and one step-down output. The proposed topology enjoys the benefits of a) reduced switch count compared with its discrete counterparts; b) zero voltage switching (ZVS) among

This work is sponsored in part by Shanghai Sailing Program (16YF1407600).

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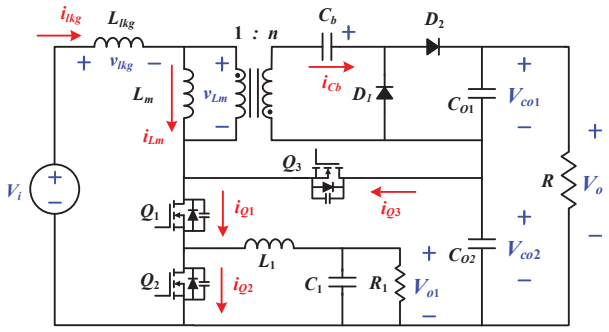

Fig. 2. Schematic of the proposed integrated SIDO converter.

all the MOSFETs and reduced switching losses; c) precise and independent control of the dual outputs; and d) the extension capability to multiple step-down output ports.

II. Proposed SIDO Converter

A. Topology Description

The proposed converter origins from the conventional flyback converter. As shown in Fig. 2, a voltage-doubler rectifier network is added on the secondary side of the flyback converter. Furthermore, a bidirectional boost converter is inserted to form a parallel-input-series-output configuration. Moreover, by adding switch (Q_2) series with Q_1 plus a LC filter network, a step-down output port is implemented. By actively controlling the duty ratios of $Q_{1\text{-}3}$, the converter provides a high step-up output and a step-down output simultaneously. The intermediate bidirectional boost structure ensures the soft switching of all the switches. Further advantages such as a) high switch working frequency, b) high device utilization rate, and c) switch voltage stress clamping can also be achieved using the proposed topology.

B. Operation Principle

The key steady state waveforms of the proposed integrated SIDO converter are plotted in Fig. 3. As shown, in each switching cycle, there are nine different operating modes. The next switching cycle is symmetrical to the first switching cycle. One specific switching period, [t_0, t_9) is extracted for detail analysis. Those nine operating modes correspond to nine equivalent circuits as plotted in Fig. 4.

The operating modes analysis is based on the assumption that C_b, C_1, C_{o1} and C_{o2} are sufficiently large, such that their voltage ripples can be ignored. Thus, those capacitor voltages are considered as dc voltages, V_{Cb}, V_{C1}, V_{Co1} and V_{Co2}, respectively.

Mode I: [t_0, t_1). At $t_{0\text{-}}$, the body diodes of Q_1 and Q_2 are conducting, which creates a zero voltage condition for the turning on of the MOSFETs. At t_0, the MOSFETs channels are turned on with ZVS. The voltage across L_m is $(V_{cb}-V_{co1})/n$. While the voltage across C_b is negative, as shown in Fig. 4(a). Mode I ends when the current through the capacitor C_b (i_{Cb}) reaches zero. In mode I, the current through the inductor L_{lkg} (i_{Llkg}) increases linearly as follows,

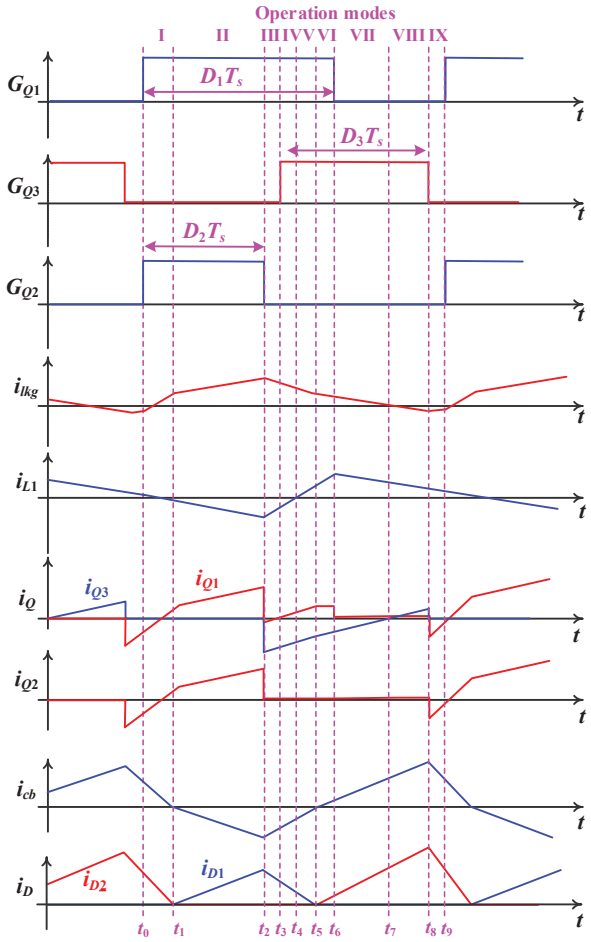

Fig. 3. Steady state operation waveforms.

$$i_{lkg}(t)=\frac{V_i+(V_{co1}-V_{Cb})/n}{L_{lkg}}(t-t_0)+i_{lkg}(t_0) \tag{1}$$

the current through the inductor L_1 (i_{L1}) decreases linearly as,

$$i_{L1}(t)=-\frac{V_{o1}}{L_1}(t-t_0)+i_{L1}(t_0) \tag{2}$$

Mode II: [t_1, t_2). At t_1, the positive terminal of C_b is connected to the coupling point of the transformer via D_1. I_{Cb} reverses its polarity to negative. D_2 is turned off and D_1 is turned on. Mode II ends when Q_2 is turned off. In mode II, i_{L1} continues to decrease, i_{lkg} increases linearly as follows,

$$i_{lkg}(t)=\frac{V_i-V_{Cb}/n}{L_{lkg}}(t-t_1)+i_{lkg}(t_1) \tag{3}$$

Mode III: [t_2, t_3). At t_2, Q_2 is turned off. Since i_{lkg} is positive, the body diode of Q_3 begins to conduct. The applied voltage across L_1 is positive. Thus, i_{L1} and i_{cb} increase linearly

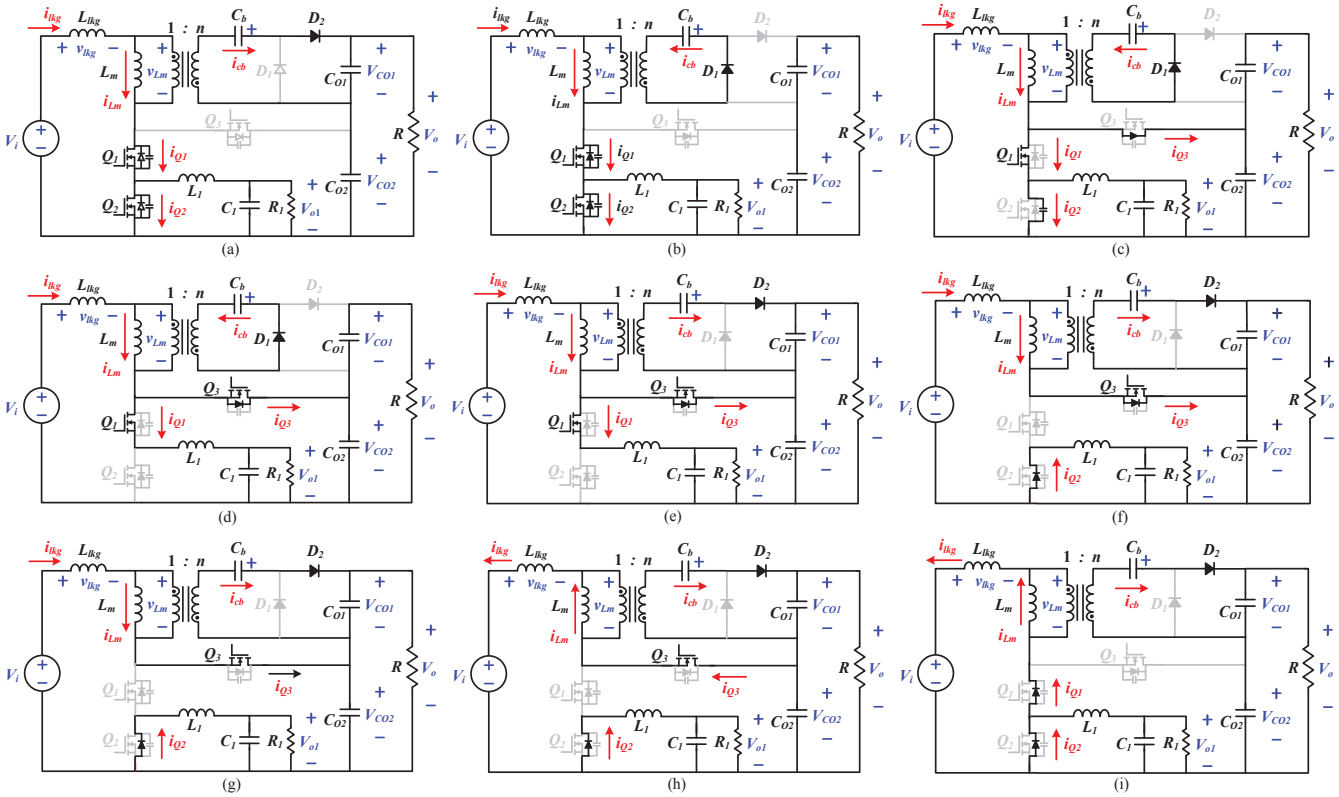

Fig. 4. Converter equivalent circuits in different operation modes.

respectively. Mode III ends when Q_3 is turned on. In mode III, i_{lkg} decreases linearly,

$$i_{lkg}(t)=\frac{V_i-V_{co2}-V_{Cb}/n}{L_{lkg}}(t-t_2)+i_{lkg}(t_2) \tag{4}$$

i_{L1} increases linearly as,

$$i_{L1}(t)=\frac{V_{co2}-V_{o1}}{L_1}(t-t_2)+i_{L1}(t_2) \tag{5}$$

Mode IV: [t_3, t_4). At t_3, Q_3 is turned on with ZVS. i_{L1} continues to increase and the $i_{\rm lkg}$ continues to decrease, respectively.

Mode V: [t_4, t_5). Before t_4, i_{L1} continues to increase linearly. At t_4, i_{L1} reverses its polarity to positive, and $i_{\rm lkg}$ continues to decrease linearly.

Mode VI: [t_5, t_6). Before t_5, i_{cb} continues to increase linearly. At t_4, $i_{\rm cb}$ reverses its polarity to positive. Meanwhile, D_2 is turned on and D_1 is turned off. Mode VI ends when Q_1 is turned off. In this mode, $i_{\rm lkg}$ decreases linearly as,

$$i_{lkg}(t)=\frac{V_i-V_{co2}+(V_{co1}-V_{Cb})/n}{L_{lkg}}(t-t_5)+i_{lkg}(t_5) \tag{6}$$

Mode VII: [t_6, t_7). At t_6, Q_1 is turned off; i_{Q1} drops to zero; and i_{L1} reaches its peak value. In mode VII, i_{L1} is positive. Thus, the body diode of Q_2 starts to conduct. Mode VII ends when i_{Q3} reaches zero. In mode VII, i_{lkg} continues to decrease linearly and i_{L1} decreases linearly as,

$$i_{L1}(t)=-\frac{V_{o1}}{L_1}(t-t_6)+i_{L1}(t_6) \tag{7}$$

Mode VIII: [t_7, t_8). At t_7, i_{lkg} and i_{Q3} change their polarities to negative and positive, respectively. Mode VIII ends when Q_1 is turned off. In this mode, i_{lkg} and i_{L1} continue to decrease linearly.

Mode IX: [t_8, t_9). At t_8, Q_3 is turned off, $i_{\rm cb}$ reaches its peak value. In this mode, i_{Q1} and i_{Q2} both change their polarities to negative and flow through the body diodes of Q_1 and Q_2. Mode IX ends when Q_1 and Q_2 are turned on, which denotes the start of the next switching period. i_{L1} continues to decrease linearly and $i_{\rm lkg}$ decreases linearly as,

$$i_{lkg}(t)=\frac{V_i-(V_{co1}-V_{Cb})/n}{L_{lkg}}(t-t_8)+i_{lkg}(t_8) \tag{8}$$

III. Circuit Analysis and Design Considerations

A. Voltage Gain

Derivation of the voltage conversion ratio is based on those approximations:

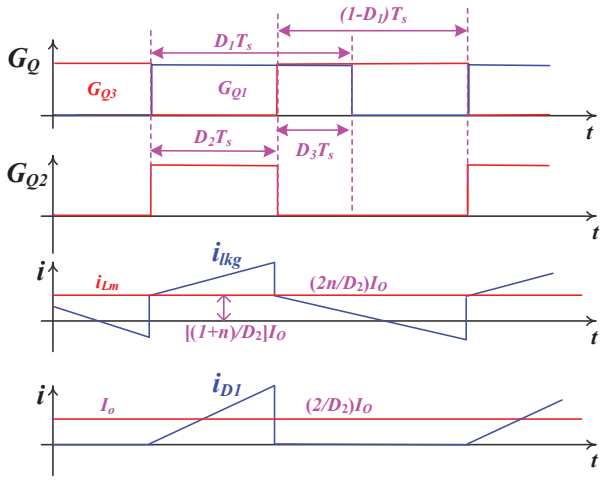

Fig. 5. Gate signals and simplified current waveforms.

a) The filtering output capacitances are sufficiently large.

b) The converter is ideal without intermediate energy losses.

c) The current ripple of the magnetizing inductor is much smaller than that of the leakage inductor and can be assumed as zero.

d) The relatively narrow time intervals, t_0-t_1, t_8-t_9 and t_2-t_5, can be assumed to be zero.

Fig. 5 shows the corresponding current waveforms under those assumptions. According to the law of energy conservation, by applying the principles of capacitor charge balance on C_b, and volt-second balance on L_{lkg} and L_m, the step-up ratio of the converter, M_1, can be derived as,

$$M_1 = \frac{V_o}{V_i} = 1 + \frac{(1-n)RD_2}{(2nL_{lkg}f_s - RD_2)(1-D_2)} \tag{9}$$

where, f_s is the switching frequency, R is the load resistance on the high voltage output, and D_2 is the duty cycle of Q_2. When n equals to zero, M_1 coincides with the step-up ratio of the classical boost converter.

The step-down ratio of the converter is,

$$\frac{V_{o1}}{V_i} = \frac{V_{o1}}{V_{Co2}} \cdot \frac{V_{Co2}}{V_i} = \frac{D_1 - D_2}{1 - D_2} \tag{10}$$

where, D_1 is the duty cycle of Q_1. From Eq. 10, it can be seen that the step-down output can be regulated by D_1 and D_2.

B. Topology Extention

The proposed dual output converter can be extended to its n outputs version by adding $n-1$ series-connected switches and LC filter networks. The single input n outputs dc/dc architecture can provide a high step-up output and n-1 step-down outputs. Fig. 6 demonstrates the schematic of the extended circuit.

According to the analysis of the dual-output converter, the n-stage step-down ratio of the converter (as shown in the shadowed area) can be derived as,

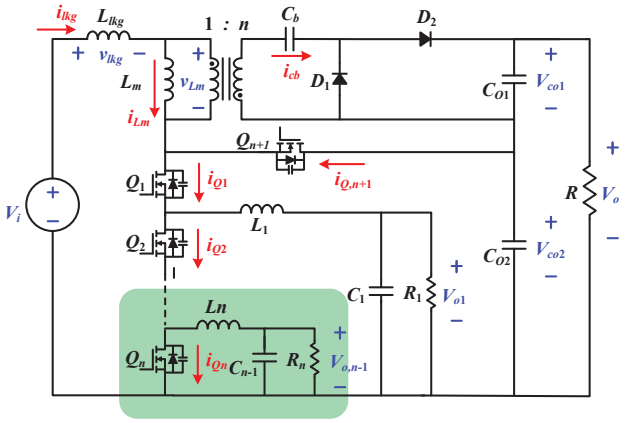

Fig. 6. Proposed integrated multiple-outputs dc/dc converter structure.

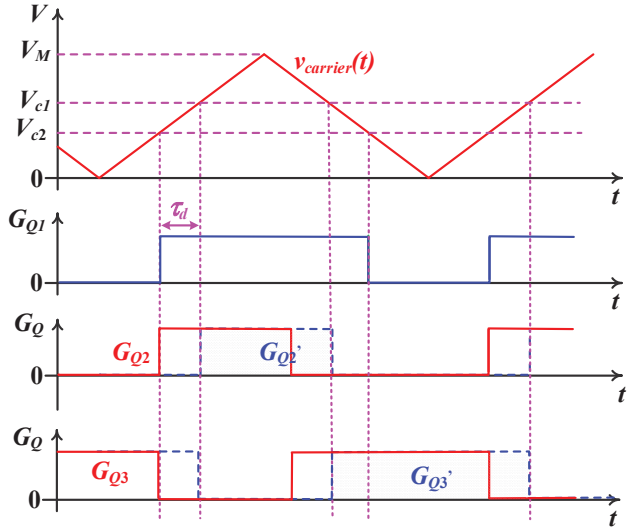

Fig. 7. PWM signals generation schematic

$$\frac{V_{o,n-1}}{V_i} = \frac{V_{o,n-1}}{V_{o,n-2}} \cdot \frac{V_{o,n-2}}{V_{C,n-3}} \cdots \frac{V_{Co2}}{V_i} = \frac{D_1 - D_2 - \cdots - D_n}{1 - D_n} \tag{11}$$

C. PWM Control Strategy

As aforementioned, D_1 and D_2 can regulate each of the individual output precisely. In this section, a simple PWM based control scheme is introduced.

The main scheme for PWM signals generation is demonstrated in Fig. 7. The modulating signals (V_{c1} & V_{c2}) are compared with the same carrier signal ($v_{carrier}(t)$). Thus, the gate signals of Q_2 and Q_3 (G_{Q2}' and G_{Q3}') are generated. In order to ensure the ZVS of Q_2, synchronous gate signals of Q_2 and Q_3 (G_{Q2} and G_{Q3}) are adopted. This means that Q_2 is turned on together with the Q_1. It should be noted that a short time delay (τ_d) must be enforced between two different carrier signals. τ_d can be found as,

$$\tau_d = \frac{(V_{c1} - V_{c2})}{2fV_M} \tag{12}$$

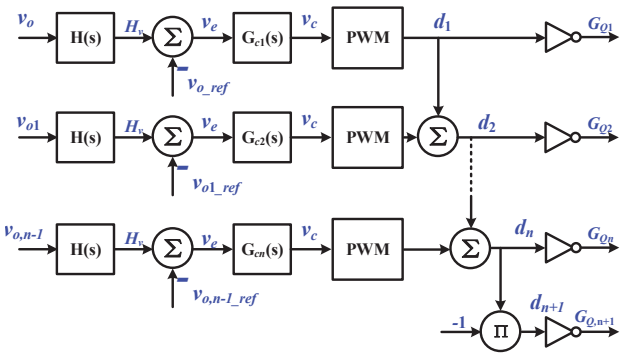

Fig. 8 PWM control schematic for multi outputs converter.

TABLE I

CIRCUIT SPECIFICATIONS AND DESIGN PARAMETERS

Quantity	Symbol	Parameter
Input voltage	V_i	42 V
Outputs voltage	V_o	400 V
	V_{o1}	15 V
Rated power	P	260 W
Primary side inductor	L_{lkg}	10 µH
Secondary side inductor	L_1	50 µH
Magnetizing inductor	L_m	300 µH
Secondary side capacitor	C_b	100 µF
Output capacitor 1	C_{o1}	100 µF
Output capacitor 2	C_{o2}	100 µF
Switching frequency	f_s	100 kHz

where, f is the frequency of the carrier signal.

The PWM signal generation scheme for multi outputs converter is shown in Fig. 8. The output voltage V_o is sampled by a voltage sensor with its s-domain gain equal to $H(s)$. Then H_v is compared with a reference signal ($v_{o,ref}$) to generate the error signal (v_e). The modulating signal of Q_1 equals to v_e times the compensator gain, $G_{c1}(s)$. Then it is fed into the pulse-width modulator to generate the PWM signal d_1. For the other PWM signals generations, due to the integrated structure, the error amplifier (EA) output of the higher stage is the sum of the EA output of the previous stage and the present EA value. The gate signal of Q_{n+1} is complementary with that of Q_n. Since G_{Q1} and G_{Q2} can be regulated independently, the step-up and step-down outputs can be controlled independently.

IV. RESULTS

A 250 W, 42 V input, 390 V, 15 V outputs converter is designed. The specifications and design parameters of the prototype are summarized in Table I.

Fig. 9 (a) shows that how the stepped up voltage varies with the variation of D_2. As shown, the high output voltage increases with the increase of D_2. A wide output voltage range from 250 V to 500 V is mapped to the range of D_2 from 0.5 to 0.8. Fig. 9 (b) demonstrates the variation of the step-down voltage with D_2 (D_1 is constant); while Fig. 9 (c) shows how the step-down voltage varies with D_1 (D_2 is constant). The simulation results agree well with the theoretical predictions.

Fig. 10 demonstrates the gate-source voltage and the drain-source voltage waveforms of Q_2 and Q_3. As shown, v_{DS2}

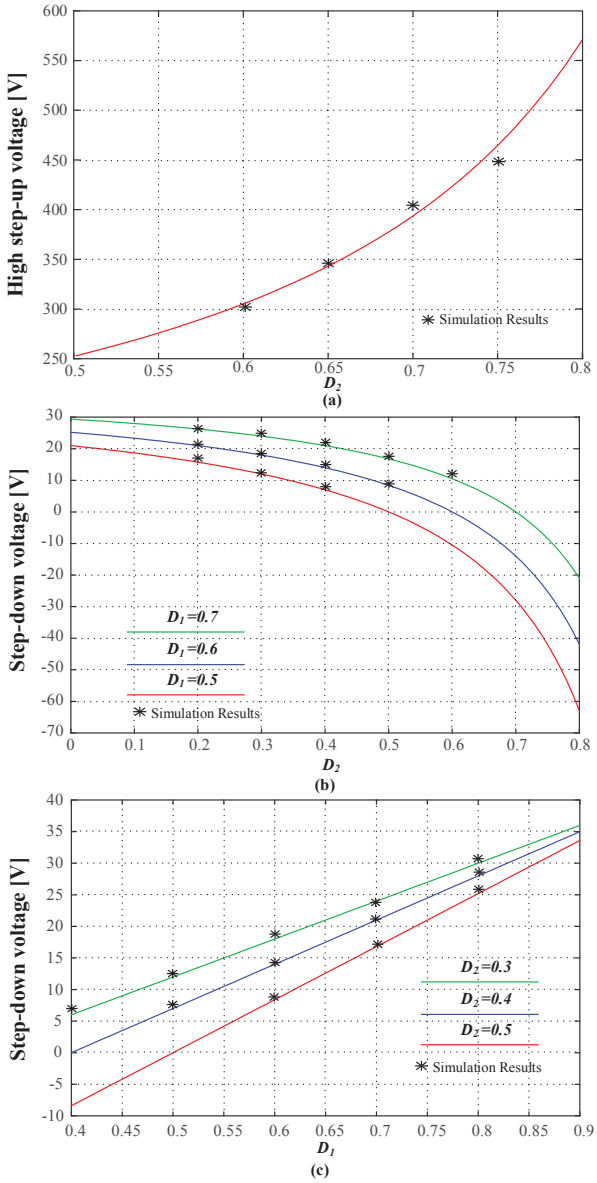

Fig. 9. Converter performances: theoretical predictions compared with simulation results: a) high step-up voltage versus D_2; b) step-down voltage versus D_2; c) step-down voltage versus D_1.

and v_{DS3} drop to zero before the conduction of MOSFET channels. i_{lkg} contributes to discharge the MOSFET parasitic capacitors. Therefore, ZVS is achieved during the MOSFET turn-on process. Similar ZVS phenomenon also applies to Q_1, as shown in Fig. 11.

Fig. 11 shows the voltage waveforms of MOSFET Q_1 and the current waveforms of the output rectifiers (D_1 & D_2). As can be seen from the figure, the ZVS of the switch Q_1 and the zero current turn-off of each rectifier is achieved.

Fig. 12 shows the waveforms of the Vi, V_o, V_{o1}, as well as i_{Llkg} at the rated power. The output voltage waveforms are very clean without high frequency ringing. The waveform of i_{Llkg} agrees well with the aforementioned steady state analysis.

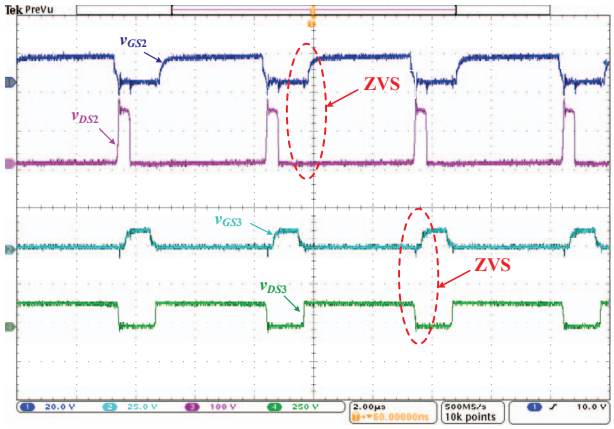

Fig. 10. Voltage waveforms of the MOSFETs at full load.

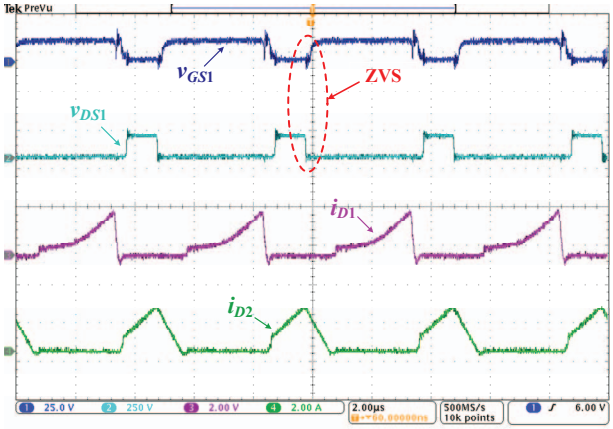

Fig. 11. Voltage waveforms of the MOSFET Q_1 and the current waveforms of the output rectifiers.

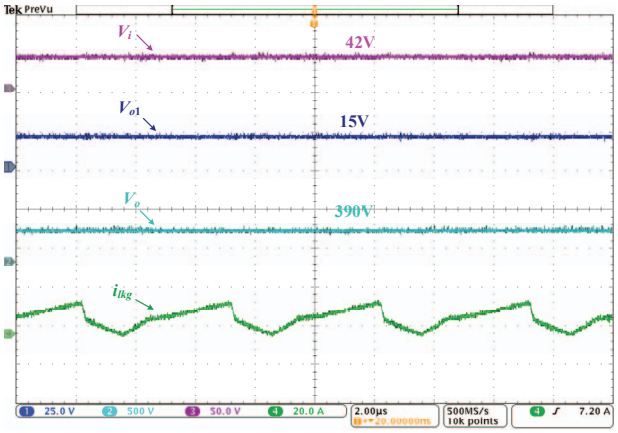

Fig. 12. The input and output voltages and the primary leakage current waveforms.

V. Conclusions

To improve the performance of the conventional high step-up converters in SIMO applications, a novel integrated single-input-dual-outputs dc/dc topology with one high step-up output and one step-down output is proposed in this paper. Steady state analyses are conducted, and the voltage conversion ratios are derived. Moreover, by adding another series-connected switches and LC filter networks, this dual-output topology can be easily extended to multiple outputs. Compared with the traditional SIMO converters, this novel topology has the advantages in reduced switching losses for all power MOSFETs are turned on with ZVS. Experimental results are provided to highlight the merits of this converter. The proposed converter can be applied to high frequency applications.

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