A Pulse Width Modulated LLC Type Resonant Topology Adpated to Wide Output Voltage Range

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***Abstract*—In a two stage LLC based plug-in electric vehicle (PEV) onboard charger, the dc link voltage is usually kept constant while the battery pack voltage varies in a wide range. This makes it extremely difficult to optimally design the second stage pulse frequency modulated (PFM) LLC resonant converter. In this paper, a modified pulse width modulated (PWM) LLC resonant topology is proposed and investigated in PEV charging applications. The proposed converter is able to achieve wide output voltage range, while maintaining the switching frequency of the full bridge constant and equal to the resonant frequency. In comparison with the conventional LLC topology, only one auxiliary MOSFET is added. Zero-voltage-switching (ZVS) is realized among all power MOSFETs. A 1.2 kW converter prototype, generating 250V-420V output voltages from the 390 V dc link, is analyzed, designed, and simulated to verify the proof of concept.**

Keywords— fixed frequency; LLC; PWM; ZVS; onboard charging; PEV

I. INTRODUCTION

A typical PEV onboard charger consists of two stages: a) the first stage ac/dc converter for rectification and power factor correction, and b) the second stage dc/dc converter for voltage/current regulation and galvanic isolation[1]–[3]. LLC resonant topology has attractive features, such as: a) wide zero voltage switching (ZVS) range, b) wide output voltage range, and c) reduced electromagnetic interferences [4]. Therefore, it is deemed as a good candidate to implement the second stage dc/dc converter of the PEV onboard chargers [5]–[7].

In [8], a 10 kW LLC resonate converter was designed to charge a 250 V- 450 V battery pack and achieved 96% peak load efficiency at 420 V. However, when the output voltage deviates from 420 V, the conversion efficiency degrades fast. Similar phenomenon is also observed in the other literatures [9]–[13]. This is because LLC topology only demonstrates optimum efficiency performance around the resonant frequency (f_r) between its resonant inductor (L_r) and capacitor (C_r). However, in order to be adapted to the wide voltage gain variation range, the switching frequency (f_s) must swing in a wide range and deviate from f_r. This phenomenon can be observed clearly from Fig. 1, which shows the dc voltage gain of LLC converter adapted to wide output voltage range. As shown, the desired output voltage window [V_{min}, V_{max}] on the gain axis is mapped to an ultra-wide switching frequency range

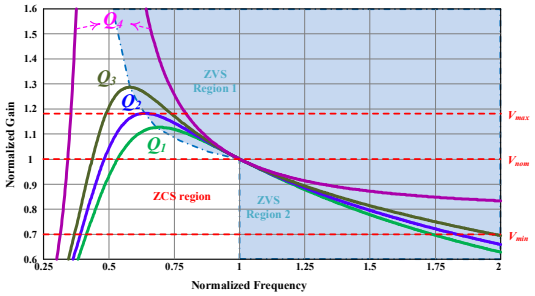

Fig. 1. DC voltage characteristics of conventional LLC converter adapted to wide output voltage range.

in the frequency axis. Therefore, it is extremely difficult to optimally design the LLC converter.

To alleviate this problem and to narrow down the switching frequency range of LLC topology, different alternative techniques were investigated in literature [14]–[16]. In [14], phase shift controlled MOSFETs are introduced to the secondary side of LLC topology, mainly for compensating the switching frequency deviation during the hold-up time. In [15], the first stage ac/dc PFC converter of the LLC based PEV charger is designed to have variable output dc link voltage. This dc link voltage linearly follows the battery pack voltage. Therefore, the LLC switching frequency variation is significantly narrowed down. In [15], the LLC topology is integrated with a two-phase interleaved boost circuit. The latter provides the boost feature to the modified circuit and successfully squeezes the switching frequency of the LLC converter.

In this paper, a novel pulse width controlled LLC topology is proposed. The proposed converter partially utilizes the voltage doubler architecture on the secondary side rectification stage. By inserting an actively controlled MOSFET and a passive controlled diode to the voltage doubler rectifier, the output voltage of the converter can be modulated by the duty cycle of the auxiliary MOSFET. Therefore, the main LLC topology can operate at its resonant frequency. This proposed converter demonstrates benefits including: a) optimum efficiency of the main LLC power circuit; b) ZVS turning-on of auxiliary MOSFET; c) ZCS turning-off the secondary side diodes; d) reduced circuit control complexity; and e) reduced circulating current and conduction losses.

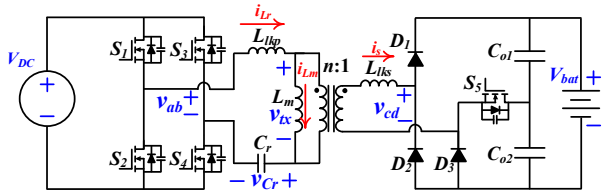

Fig. 2. Proposed PWM LLC topology.

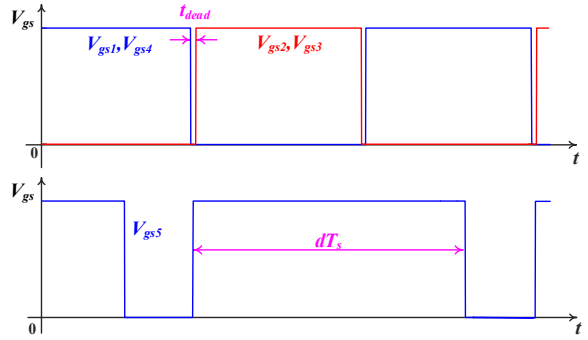

Fig. 3. Switch pattern of the actively controlled MOSFETs.

II. Proposed PWM LLC Type DC/DC Converter

A. Topology Description

The schematic of the proposed PWM LLC resonant converter is demonstrated in Fig. 2. This topology is derived from the full bridge LLC topology with voltage doubler rectification stage. However, compared with the voltage doubler rectification, an auxiliary diode-MOSFET bridge (D_3 and S_5) is added on the secondary side (see Fig. 2). By actively controlling the duty ratio of S_5, the output voltage changes accordingly. Therefore, this converter can be modulated by the pulse width of M_5.

Moreover, the transformer is designed to have a secondary side leakage inductance, L_{lks}. This modification adds those benefits to the circuit: a) the sharp current variation slope on the secondary side semiconductors is it mitigated; b) the ZCS turning off of diode D_1 is facilitated; and c) the pulse width modulation capability of the voltage gain is enhanced.

B. Operation Principle

In the proposed converter, the primary side full bridge functions as a constant frequency square wave generator. The upper and lower power MOSFETs are turned on and off complementarily with certain deadband (t_{dead}), to prevent the circuit shoot through. This switching frequency is fixed and equal to the resonant frequency between the transformer primary leakage inductance and the resonant capacitance:

$$f_s = \frac{1}{2\sqrt{L_{lkp}C_r}} \qquad (1)$$

The switching pattern of MOSFETs S_1-S_5, is plotted in Fig. 3. It should be noted that the switching frequency of MOSFET S_5 is equal to f_s. Therefore, the primary side MOSFETs can be guaranteed with both ZVS and optimized circulating currents. On the secondary side, the turning on moment must be

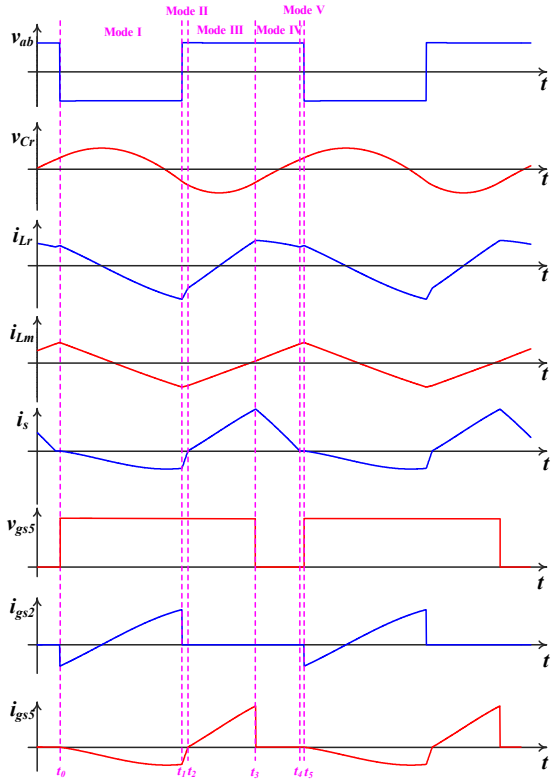

Fig. 4. Steady state operation waveforms of the proposed converter.

synchronized within the deadband, when the MOSFETs in the primary side full bridge inverter are all off. Typically, the duty cycle of M_5, d, should be constrained within the range of [0.5, 1]. This is mainly due to two facts associated with $d < 0.5$: a) the auxiliary MOSFET loses its ZVS feature; and b) the output will be a constant voltage; the circuit loses its PWM feature.

The steady state waveforms of the proposed converter is plotted in Fig. 4. In each switching period, the steady state operation can be divided into 5 operation modes. Those operation modes are given in Fig. 5.

Mode I: [t_0, t_1). Mode I begins in the deadband at t_0 when S_5 is tuned on. In the beginning of Mode I, i_{Lr} charges and discharges the output capacitors of S_1-S_4. Thus, v_{ab} is inverted from V_{DC} to -V_{DC}. After t_0, S_2 and S_3 are both turned on. During Mode I, L_r resonates with C_r. The secondary side current, i_s, is negative and flows through D_2 and the body diode of the auxiliary MOSFET, D_{S5}. It should be noted that: $t_1 - t_0 = T_s/2$.

Mode II: [t_1, t_2). When the switch pattern of S_1-S_4 is inverted at t_1, the circuit operation enters into Mode II. Similarly, at the beginning of Mode II, i_{Lr} discharges and charges the output capacitors of S_1-S_4. Thus, v_{ab} is inverted from -V_{DC} to V_{DC}. D_{S5} and D_2 continue to conduct in mode II. During Mode II, V_{DC} on the primary side and $-V_{Co2}$ on the secondary side jointly enforce a steep di/dt on the secondary side leakage inductor L_{lks}. Thus, i_s increases from negative to zero in a short time period, which marks the end of Mode II.

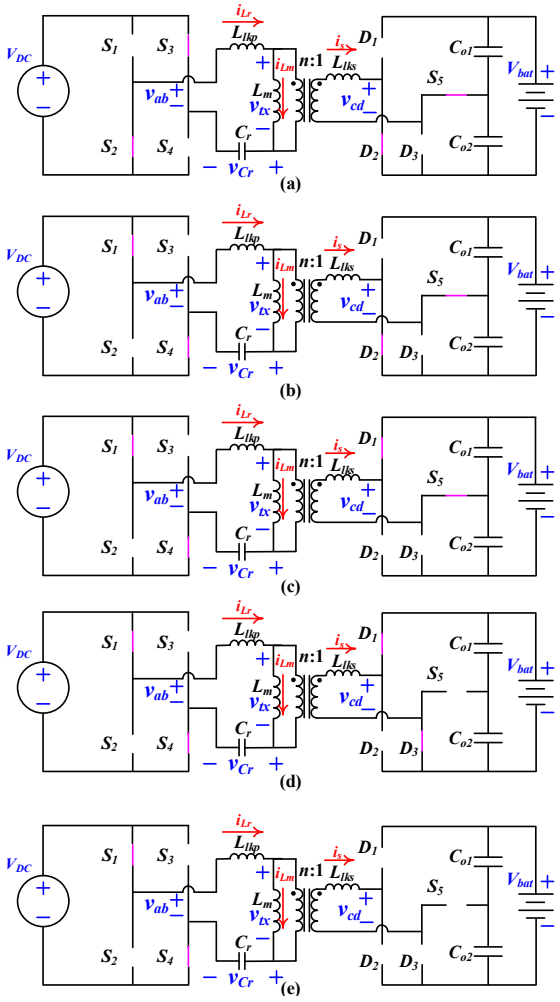

Fig. 5. Operation modes of the converter; a) Mode I: $t_0 \le t < t_1$; b) Mode II, $t_1 \le t < t_2$; c) Mode III, $t_2 \le t < t_3$; d) Mode IV, $t_3 \le t < t_4$; e) Mode V, $t_4 \le t < t_5$.

Mode III [t_2, t_3). Mode III starts when i_s reaches zero at t_2. After t_2, the current conduction on the secondary side is switched from D_{S5} and D_2 to D_1 and S_5. Therefore, S_5 is turned on at ZVS. V_{Co1} is connected to the secondary side of the transformer. In Mode III, the effect of V_{DC} on i_s is partially cancelled by V_{Co1}. Thus, although i_s continues to increase, the growth rate is much slower; this can been clearly seen in Fig. 4. $S_{2,3,5}$, and D_1 are the conducting semiconductors. Mode III ends at t_3 when S_5 is turned off. It should be noted that: $t_3 - t_1 = (d - 0.5)T_s$.

Mode IV [t_3, t_4). Mode IV starts as S_5 is turned off. Since the inductor current is continuous, its path is switched from S_5 to D_3. Hence, V_{bat} is connected to the secondary side of the transformer directly. Since V_{bat} is much larger than V_{Co1}, it induces i_s to decrease in this operation mode, as can be seen in Fig. 4. Mode IV ends when i_s reaches zero.

Mode V [t_4, t_5). At t_4, i_s reaches zero and the circuit enters into Mode V. Since M_5 is still off, i_s stays at zero. Thus, all the semiconductors on the secondary side are off. Mode V ends when the switch pattern of S_1-S_4 is inverted again, which marks the start of next switching period.

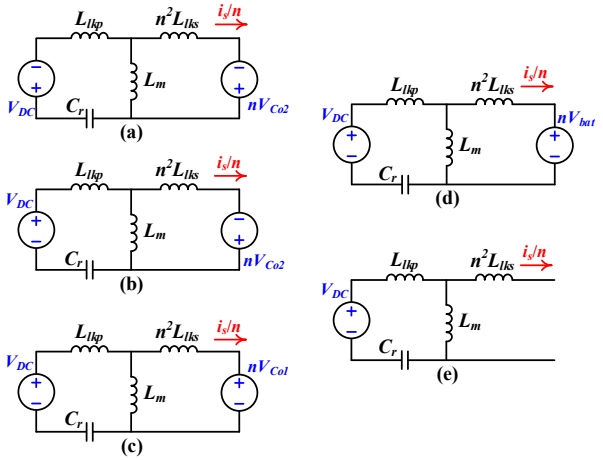

Fig. 6. Equivalent circuit model of the converter; a) Mode I: $t_0 \le t < t_1$; b) Mode II, $t_1 \le t < t_2$; c) Mode III, $t_2 \le t < t_3$; d) Mode IV, $t_3 \le t < t_4$; e) Mode V, $t_4 \le t < t_5$.

III. Circuit Modeling and Analysis

A. Equivalent Circuit Model

Based on the steady state analysis in Section II-B, the equivalent circuit model of the proposed topology can be obtained. Assuming that both output filtering capacitances (C_{o1} and C_{o2}) are sufficiently large, the voltage on each capacitor could be considered as a constant. Therefore, C_{o1} and C_{o2} can be equivalent to two constant voltage sources, whose voltages are denoted as V_{Co1} and V_{Co2}, respectively. Moreover, the voltage source and the impedance on the secondary side of the transformer can be pushed to the primary side with ratios n and n^2, respectively. The resultant equivalent circuit model of the converter is plotted in Fig. 6. The circuit model is composed by an input voltage source, a two port impedance network, as well as an output voltage source. The output voltage source varies step-by-step with the transitions of operation modes.

B. Piecewise Linear Current Approximation

As mentioned earlier, the full bridge inverter generates a square wave, v_{ab}. Its Fourier series is expressed as,

$$v_{ab}(t) = \sum_{n=1,3,5,7..} \frac{4V_{DC}}{n\pi} \sin(2\pi n f_s t) \qquad (2)$$

f_s is equal to the resonant frequency between C_r and L_{lkp}. This means that the impedance of C_r and L_{lkp} is equal to zero at f_s. Thus, the first harmonic component of the square wave is transmitted to the magnetizing inductor without degradation. Conventionally, first harmonic approximation technique is widely used to model the LLC topology operating at its resonant frequency [17].

In this case, to facilitate the circuit analysis, it is assumed that the voltage applied to L_m is approximately equal to the input voltage source without degradation. Hence, the magnetizing inductor current i_{Lm} decreases at the rate of $-V_{dc}/L_m$ in Mode I; while i_{Lm} increases at the rate of V_{DC}/L_m in

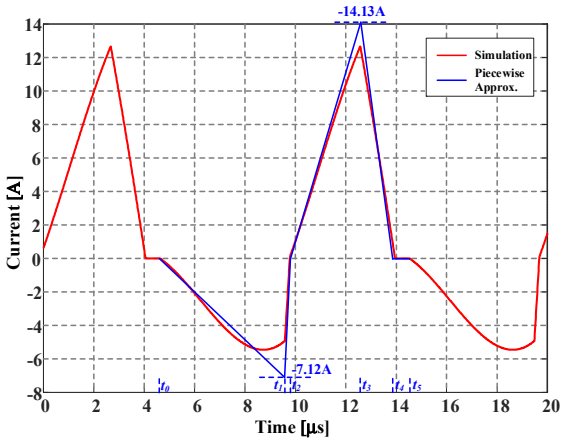

Fig. 7. Piecewise linear approximation of i_s and its comparison with the simulated waveform.

Modes II-V. The accuracy of this approximation can be roughly evaluated from the linearity of i_{Lm}, as shown in Fig. 4.

Based on this approximation, i_s changes piecewise linearly. The rate di_s/dt changes step-by-step with the transition of operation modes. In Mode I,

$$i_s(\mathrm{t}) = \frac{-V_{DC}/n + V_{Co2}}{L_{lks}}(\mathrm{t}-\mathrm{t}_0) \tag{3}$$

Since the duration of mode I is $T_s/2$, $i_s(\mathrm{t}_1)$ can be easily calculated based on Eq. (3). It should be noted that $i_s(\mathrm{t}_1)$ denotes the peak current of D_2.

In Mode II, the input voltage source revert its polarity, V_{DC} and V_{Co2} jointly push i_s(t) to zero very fast.

$$i_s(\mathrm{t}) = \frac{V_{DC}/n + V_{Co2}}{L_{lks}}(\mathrm{t}-\mathrm{t}_1) + i_s(\mathrm{t}_1) \tag{4}$$

The duration of Mode II is the initial current $i_s(\mathrm{t}_1)$ divided by the slope of i_s(t) in this mode, as,

$$t_2 - t_1 = \frac{V_{DC}/n - V_{Co2}}{V_{DC}/n + V_{Co2}}\frac{T_s}{2} \tag{5}$$

In Mode III, the output voltage source is transited to nV_{Co1}, i_s(t) begins to increase from zero.

$$i_s(\mathrm{t}) = \frac{V_{DC}/n - V_{Co1}}{L_{lks}}(t - t_2) \tag{6}$$

Since the turning off of S_5 denotes the end of Mode III, the duration of Mode III is dT_s-t_2. It should be noted that $i_s(\mathrm{t}_3)$ denotes the peak current of D_1 and S_5.

In Mode IV, the secondary side of transformer sees the sum of V_{Co1} and V_{Co2}.

$$i_s(\mathrm{t}) = \frac{V_{DC}/n - V_{bat}}{L_{lks}}(t - t_3) + i_s(t_3) \tag{7}$$

The duration of Mode IV is the initial current $i_s(t_3)$ divided by the slope of $i_s(t)$ in this mode, as,

$$t_4 - t_3 = \frac{V_{DC}/n - V_{Co2}}{V_{bat} - V_{DC}/n}(dT_s - t_2) \tag{8}$$

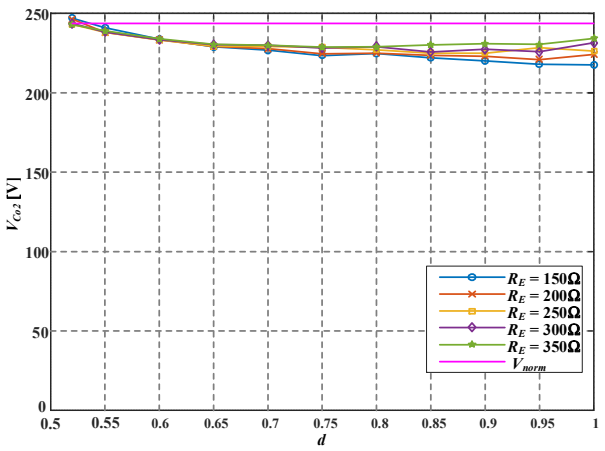

Fig. 8. Simulated V_{Co2} versus duty cycle under different effective load conditions and their comparison with V_{norm}.

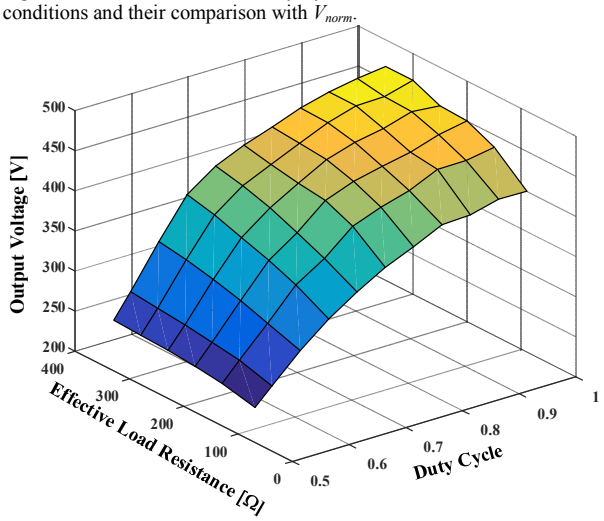

Fig. 9. Voltage gain versus equivalent R_L and d.

In Mode V, the voltage applied to L_{lks} is equal to zero. The duration of Mode V is $T_s - t_4$.

$$i_s(\mathrm{t}) = 0 \tag{9}$$

The data obtained based on equations (3-9) and the simulated data are plotted and compared in Fig. 7 to verify the accuracy of the proposed piecewise linear current approximation method. As shown in Fig. 7, t_2 and t_4 agrees very well with the simulation. While there is a small error on $i_s(t_1)$ and $i_s(t_3)$; this error is considered as acceptable.

C. Voltage Gain

According to the law of energy conservation and assuming the converter is ideal without intermediate energy losses, the input energy is equal to the energy delivered to the battery pack. Therefore,

$$\int_{t_0}^{t_0+T_s} v_{ab}(\mathrm{t}) i_s(\mathrm{t})\,\mathrm{dt} = V_{bat} I_{bat} T_s \tag{10}$$

By applying the piecewise linear current approximation model discussed in Section III-B, one can obtain,

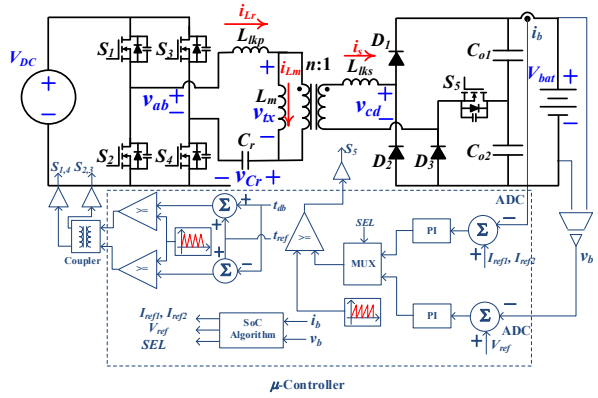

Fig. 10. Digital control diagram of proposed PWM LLC type converter in PEV battery charging applications.

$$\frac{i_s(t_1)V_{Co2}(t_2-t_1)}{2}+\frac{i_s(t_3)V_{Co1}(t_3-t_2)}{2}+\frac{i_s(t_3)V_{bat}(t_4-t_3)}{2}=V_{bat}I_{bat}T_s \tag{11}$$

Where $V_{bat} = V_{Co1} + V_{Co2}$, and I_{bat} is determined by the charging power. It should be noted that the proposed analysis methodology is also valid to the resistive load.

Based on Eq. (11), by substituting the previous derived expressions, there are still 3 unknowns left, which are V_{Co1}, V_{Co2}, and V_{DC}, respectively. Therefore, it is difficult to theoretically predict the voltage gain of the circuit based on the proposed model. On the other hand, it is interesting to note that V_{Co2} is a weak function of both the effective load and the duty cycle. Indeed, V_{Co2} is always close to the normalized voltage V_{norm}, as defined,

$$V_{norm}=\frac{V_{DC}}{n} \tag{12}$$

This phenomenon can be clearly observed from the Fig. 8, which provides the simulated data of V_{Co2} versus the duty cycle under different load conditions. According to Fig. 8, V_{Co2} slightly decreases with the increase of duty cycle; it is always slightly lower than but close to V_{norm}. Also, V_{Co2} demonstrate very good load independence performance. Thus, one can consider V_{Co2} is a constant which is approximately equal to V_{norm}. By adopting this approximation, the theoretical voltage gain can be easily calculated.

Fig. 9 plots the output voltage versus the effective load resistance, and the duty cycle. The data is obtained from software simulation, which is based on the design parameters provided in Table I. As shown in Fig. 9, the output voltage is a strong function of the duty cycle and a weak function of the effective load resistance. This means that the voltage gain can be easily regulated by the pulse width modulation.

IV. Controller Design

The digital control scheme of the proposed converter is plotted in Fig. 10. As demonstrated in the diagram, control of the circuit in the application of PEV battery charging can be implemented using a microcontroller. On the primary side of the transformer, those four MOSFETs are driven by four channel PWM signals issued by the microcontroller. No feedback is required to control the full bridge inverter. On the secondary side, the transducers sample the battery charging current, charging voltage information and send it to the microcontroller. While the CPU estimate the state of charge and determine the charging mode. In constant current charging mode, the current PI control loop is activated to maintain constant charging current. While in constant voltage charging mode, the voltage PI control loop is activated to maintain constant charging voltage. In comparison with the conventional LLC topology which utilizes the pulse frequency modulation, the control scheme in this proposed converter is much simpler. Moreover, this control algorithm can also be implemented using analog controller. This controller is easy to be integrated into an application specific integrated circuit.

TABLE I

DESIGN PARAMETERS OF THE PROPOSED CONVERTER

Quantity	Symbol	Parameter
Input voltage	V_{DC}	390V
Output voltage	V_{out}	250V-420V
Rated power	P_{max}	1.2 kW
Primary side inductor	L_{lkp}	13.8 μH
Secondary side inductor	L_{lks}	13.8 μH
Magnetizing inductor	L_m	158 μH
Resonant capacitor	C_r	180 nF
Output capacitor 1	C_{o1}	100 μF
Output capacitor 2	C_{o2}	100 μF
Switching frequency	f_s	100 kHz
Transformer turns ratio	n	1.6

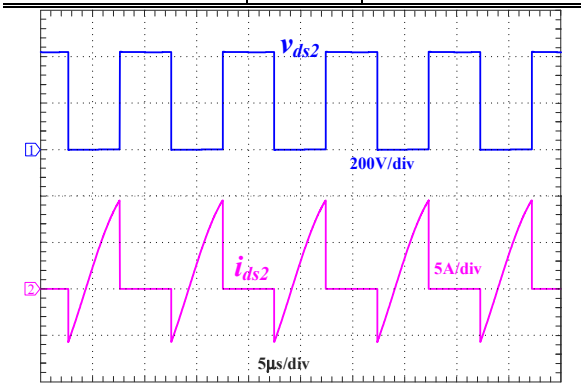

Fig. 11. ZVS turning-on of primary side MOSFET.

V. Results

Based on the proposed topology and the circuit analysis, a converter rated at 1.2 kW is designed and simulated to charge a 250 V - 420 V battery pack. The input is 390 VDC, which is the typical output voltage of the ac/dc power factor correction stage. The design parameters are provided in Table I. The simulation is conducted in Simulink.

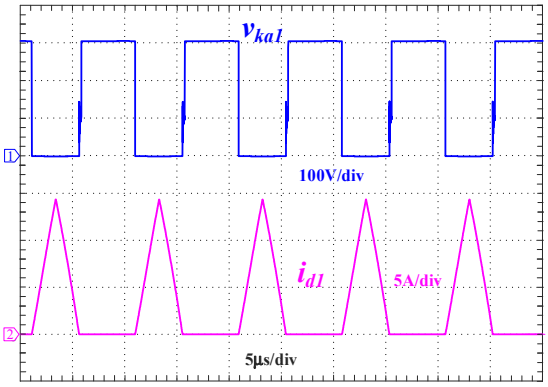

Fig. 12. ZCS turning-off of secondary side diode D_1.

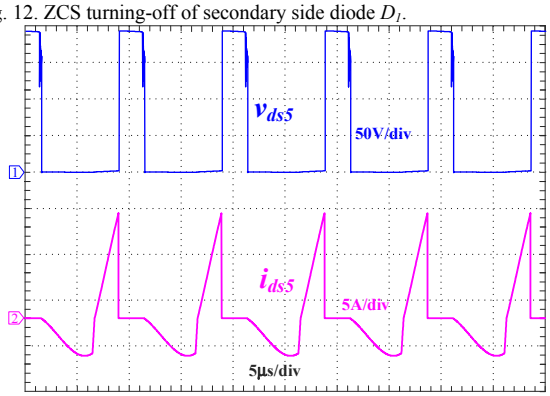

Fig. 13. ZVS turning-on of auxiliary MOSFET.

Fig. 11 demonstrates the voltage and current waveforms of the primary side MOSFET, S_2. As shown, the body diode conducts before the conduction of S_2, which provides zero voltage condition for the turning on of the MOSFET channel. Therefore, ZVS is achieved during the MOSFET turn-on process. Similar waveforms apply to $S_{1,3,4}$, too.

Fig. 12 shows the voltage and current waveforms of the secondary side diode D_1. As shown, D_1 is turned off with small di/dt, which significantly mitigates the diode reverse recovery problems. With regards to D_3, it has the identical turning off process as D_1 with small di/dt. However, it should be noted that D_2 suffers from the large di/dt of i_s during operation mode II. The slope is provided in Eq. 4. Typically, D_2 should be designed using fast recovery power diode.

Fig. 13 illustrates the voltage and current waveforms of auxiliary MOSFET, S_5. As shown, the body diode of the S_5 conducts before the conduction of MOSFET channel, which guarantees the MOSFET ZVS turning-on.

VI. CONCLUSIONS

In this paper, a PWM LLC type resonant converter is proposed for use in PEV onboard chargers. The proposed converter demonstrates the benefits of a) optimized LLC switching frequency; b) ZVS of all MOSFETs; c) ZCS turning-off the rectification diodes; d) reduced circuit control complexity; and e) reduced circulating current. A 1.2 kW converter prototype is designed to verify the proof of concept. The proposed converter topology is not only useful for PEV battery charging application, but also valid for applications where wide voltage gain range is desired.

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