

A Single Stage AC/DC Converter for Low Voltage Energy Harvesting

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Abstract—In this paper, a novel ac/dc converter is proposed for low voltage, low power rectification applications. The proposed converter manages the energy harvested from micro-scale electromagnetic transducers. It integrates the conventional Boost and Buck-Boost topologies with a shared inductor, a bidirectional switch and two split filtering capacitors. The Boost and the Buck-Boost topologies function in the positive and negative half input cycles, respectively. The inductor is energized by being shorted with the input source through the MOSFET channel without using the diodes. This enables active rectification of low amplitude (below 0.7 V) ac voltages. Theoretical analysis, design considerations and control method are detailed. A 45 mW circuit prototype, which converts a 0.4 V peak, 100 Hz ac voltage to 3.3 V dc is designed and tested to verify the proof of concept.

Keywords—ac/dc conversion; Boost, Buck-Boost; energy harvesting; low voltage, low power

I. INTRODUCTION

In recent years, low voltage and low power electronic devices for a variety of applications such as wireless sensor nodes and wearable devices have been increasingly reported in the literature [1]–[7]. In general, kinetic energy is generated from ambient vibrations and random displacements of mechanical and biological systems [8]. Electromagnetic, piezoelectric, and electrostatic transducers are commonly employed to convert the kinetic energy into electricity [9]. Micro-scale electromagnetic generators are suitable candidates to supply power to low-power self-sustainable electronic devices due to their better power densities [10].

A typical electromagnetic generator consists of a coil, a permanent magnet (PM), and a spring [11], [12]. Ambient vibrations introduce the relative displacements between the PM and the coil. The coil cuts through the magnetic flux alternatively and induces an ac voltage output. Due to the size limitation, the output of micro-scale electromagnetic generator is typically a low amplitude (below 0.4 V) and low frequency ac voltage [13]. However, most of the electronic devices require a 2 V -3.3 V dc [14]. Therefore, it is critical to design a power electronic interface, which efficiently converts this low amplitude ac voltage to a boosted and regulated dc voltage.

Traditional ac/dc topologies generally consist of two stages [13], [15]: front stage diode bridge rectifier and a cascaded dc/dc converter. However, the main disadvantages of the two-stage topologies lie in: a) unavoidable diode voltage drop, which

makes it infeasible in low voltage input applications; b) significant power losses in the front end diode bridges. Multiple direct ac/dc topologies have been reported in recent years. A two-switch H-bridge topology, which integrates two Boost converters in low voltage energy harvesting applications, is proposed in [16]. However, when the switch is off, the inductor current continues to flow via two diodes. This deteriorates both the boost ratio and conversion efficiency. A four-switch topology, which also consists of two Boost converters, is proposed in [17]. However, it has higher switch counts and requires a complicate and lossy polarity detector. Two more direct ac/dc topologies are proposed in [18], [19]. The circuit in [18] consists of two Boost converters; while the circuit in [19] consists of a Boost converter and a Buck-Boost converter. However, both converters require two inductors.

A much simpler circuit, which integrates Boost and Buck-Boost topologies while utilizing a single inductor, is proposed in [20]. However, similar to the four-switch topology in [17], it requires a complicated and lossy polarity detector. This increases the control complexity and power consumption. To address those problems, a direct ac/dc power conditioning circuit, which consists of a Boost converter and a Buck-Boost converter, is proposed in this paper, as shown in Fig. 1. In this topology, there is a bidirectional switch, which is composed of a p-MOSFET and an n-MOSFET. Those two MOSFETs are turned on and off simultaneously. Meanwhile, two split capacitors and two diodes are used to realize the operating mode transitions. This topology demonstrates the benefits of a) reduced circuit size; b) simplified control circuit; and c) the removal of the complicated and lossy polarity detector.

The operation modes of converter are described in Section II. Detailed theoretical analyses are provided in Section III. Design considerations and procedures are discussed in Section IV. The simulation results are presented in Section V. Experiment results are reported in Section VI. Section VII concludes the paper.

II. OPERATION PRINCIPLE

This study considers only the micro-scale electromagnetic generators with low output voltage. The internal resistance of a micro-scale electromagnetic generator originates from the coil resistivity. In order to simplify the circuit analysis, it is assumed that the internal resistance of micro-scale electromagnetic generator is much smaller than the input impedance of converter

This work is sponsored in part by Shanghai Sailing Program (16YF1407600).

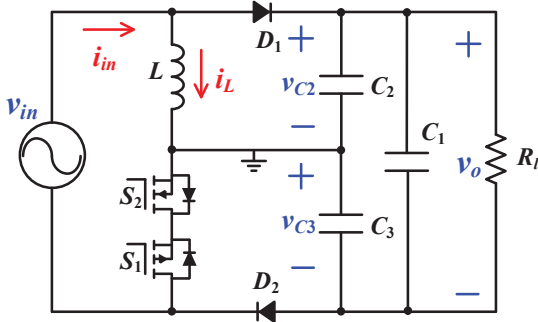


Fig. 1. Schematic of the proposed single stage rectifier.

and therefore can be ignored. In this study, a 0.4 V and 100 Hz sinusoidal ac voltage is used to emulate the output of the micro-scale electromagnetic generator.

As shown Fig. 1, in the proposed topology, only one inductor is utilized. In order to rectify the ac input to a dc voltage, the switch should be able to conduct and block currents in both directions during the on and off states, respectively. Since a MOSFET is a single quadrant switch, i.e. in on state, MOSFET channel can conduct bidirectionally; while in off state, it can only block unidirectional drain to source voltage. This is due to the existence of its body diode. Therefore, a p-MOSFET and an n-MOSFET are placed in series with their body diodes back to back, to function as a four-quadrant switch. It should be noted that turning on and off of those two MOSFETs are always synchronized.

In the positive half-cycle of the input voltage v_{in} , it operates as a Boost converter (including L , D_2 , and C_3). In the negative half-cycle of v_{in} , it operates as a Buck-Boost converter (including L , D_1 , and C_2). The discontinuous conduction mode (DCM) operation has the benefits of reduced switching losses and mitigated diode reverse recovery. Therefore, this converter is designed to operate in DCM. In DCM operation, the converter has three operating modes in each half-cycle, as shown in Fig. 2. Modes I-III correspond to the positive half-cycle, while modes IV-VI correspond to the negative half-cycle.

Mode I: When the switch is turned on, the inductor is energized by the input source. The inductor current increases linearly from zero. The switch is turned on with zero current. Therefore, switching losses are reduced. Meanwhile, both diodes are reverse biased. The output capacitors supply power to the load.

Mode II: When the switch is turned off, i_L freewheels via D_2 . C_3 is charged while C_2 is discharged. The voltage across the inductor equals to the difference between input voltage and lower capacitor voltage (v_{C3}), which is a negative value. Therefore, i_L decreases linearly until it crosses zero.

Mode III: When i_L becomes zero, D_2 turns off naturally with a small di/dt . This significantly mitigates the diode reverse recovery loss. The capacitors discharge themselves through the load. Given that the input voltage is still positive, the converter returns to Mode I as soon as the switch turns on.

Mode IV: Modes IV-VI happen when v_{in} is negative. Mode IV is similar to mode I as soon as the switch turns on. i_L linearly

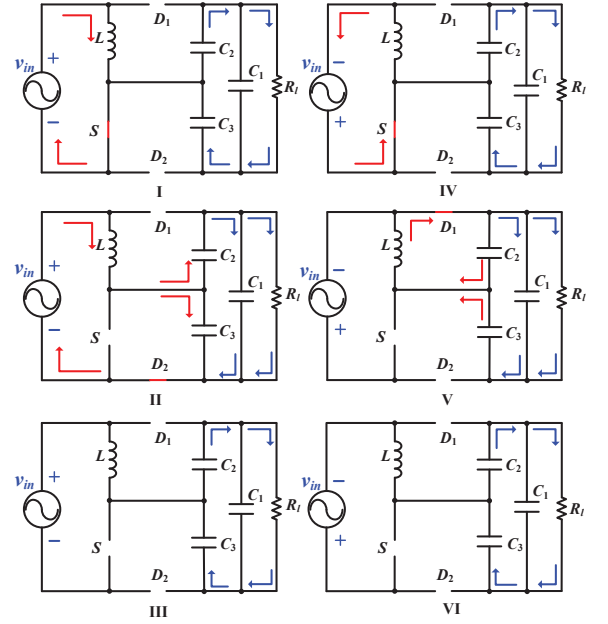


Fig. 2. Operating modes in DCM condition.

deviates from zero; the inductor is energized by the input source. The switch is also turned on at zero current. On the other hand, both diodes are reverse biased. The output capacitors supply power to the load.

Mode V: When the switch is turned off, i_L continues to freewheel via D_1 . C_2 is charged while C_3 is discharged. The voltage across the inductor equals to v_{C3} . Therefore, i_L increases linearly until it crosses zero.

Mode VI: When the inductor current increases to zero, D_1 turns off automatically. This avoids the reverse recovery losses of the diode. In this condition, the capacitors supply power to load again. Given that the input voltage is still negative, the converter returns to Mode IV.

According to the operating modes analyses, in DCM operation, both the MOSFETs turning on and the diodes turning off occur at zero current. Therefore, the switching losses are significantly reduced.

III. THEORETICAL ANALYSIS

In the proposed converter, two split capacitors, C_2 and C_3 , are used. The C_3 is charged and C_2 is discharged in Boost operation; while C_2 is charged and C_3 is discharged in Buck-Boost operation. Assuming that the capacitor is large enough to keep the voltage constant, the voltages of C_2 and C_3 are constants and equal to the half of output voltage. The switching frequency is much larger than the frequency of the input source. Therefore, the input voltage could be considered as a constant during each switching period. Hence, v_{in} can be expressed as,

$$v_{in}(t) = V_p \sin(2\pi t / T_{in}) \quad (1)$$

where, T_{in} is the period of input ac source. V_p is the amplitude of v_{in} . The input current is equal to the inductor current in Boost operation. However, in Buck-Boost operation, the input current becomes zero when the switch is turned off, as shown in Fig. 3.

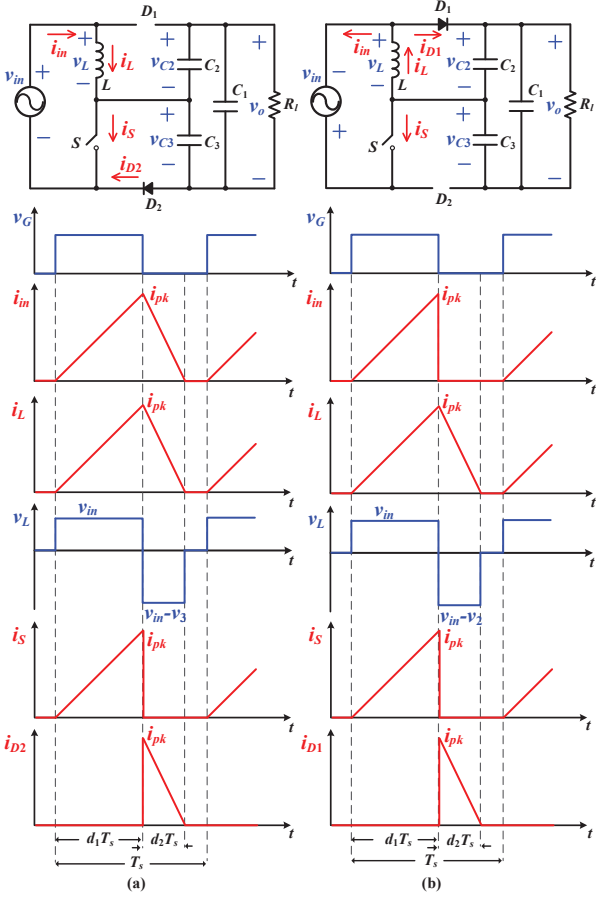


Fig. 3. Critical steady state waveforms.

T_s is the switching period, and d_1 is the duty cycle. In Boost mode, the peak value of the input current can be expressed as,

$$i_{PK}(t) = d_1 T_s v_{in} / L \quad (2)$$

According to the inductor volt-second balance,

$$v_{in} d_1 T_s = (v_o / 2 - v_{in}) d_2 T_s \quad (3)$$

The average input power in each switching period is derived as,

$$p_{in} = v_{in} i_{PK} (d_1 + d_2) / 2 \quad (4)$$

The input energy of the positive half-cycle is derived as,

$$E_{in} = \int_0^{T_{in}/2} v_{in} i_{PK} T_s (d_1 + d_2) / 2 dt \quad (5)$$

According to equations (1-5),

$$E_{in} = \int_0^{T_{in}/2} \frac{v_{in}^2 T_s d_1^2}{2L} \left(1 + \frac{v_{in}}{v_o / 2 - v_{in}} \right) dt \quad (6)$$

where, $v_o/2$ is much larger than the average value of v_{in} from $0-T_{in}/2$; the last term could be ignored. Hence, E_{in} is expressed as,

$$E_{in} \approx \frac{V_p^2 T_s d_1^2 T_{in}}{8L} \quad (7)$$

According to Eq. (7), the input energy is inversely proportional to L and proportional to d_1^2 and T_s . Assuming all components are ideal, the output energy should be equal to the input energy in the same time scale. The output energy of the positive half-cycle can be derived as,

$$E_{out} = \frac{v_o^2 T_{in}}{2R_L} = \frac{V_p^2 T_s d_1^2 T_{in}}{8L} \quad (8)$$

where, R_L is the load resistance. Therefore, the output energy can be controlled by duty cycle and switching frequency. It should be noted that Eq. (8) also applies to Buck-Boost mode. This is due to the fact that similar approximation in Eq. (7) can be extended to Buck-Boost mode.

IV. DESIGN PROCESS

In order to optimize the converter performances, the voltage gain and efficiency should be derived. According to Eq. (8), the voltage gain can be derived as,

$$\frac{v_o}{V_p} = \frac{d_1}{2} \sqrt{\frac{T_s R_L}{L}} \quad (9)$$

According to Eq. (9), the output voltage can be controlled by duty cycle and switching period. Besides, the converter is supposed to operate in DCM to reduce the switching losses. In Boost mode, the DCM criteria can be expressed as,

$$i_{PK} - (1 - d_1)(v_o / 2 - v_{in}) T_s / L < 0 \quad (10)$$

To make sure that the converter can operate in DCM under all input voltages, it should be ensured that,

$$V_p < (1 - d_1) v_o / 2 \quad (11)$$

Based on Eq. (9) and Eq. (11), the DCM condition can be expressed as,

$$d_1 (1 - d_1) \sqrt{T_s R_L / L} - 4 > 0 \quad (12)$$

The same analysis can be used in Buck-Boost mode, and the DCM condition can be expressed as,

$$(1 - d_1) \sqrt{T_s R_L / L} - 4 > 0 \quad (13)$$

Assume that,

$$Y_{DCM} = d_1 (1 - d_1) \sqrt{T_s R_L / L} - 4 \quad (14)$$

$$T = \sqrt{T_s R_L / L} \quad (15)$$

According to Eq. (12) and Eq. (13), when the duty cycle is close to zero, the Boost converter operates in CCM and the Buck-Boost converter operates in DCM. When the duty cycle is close to unity, both the Buck-Boost converter and the Boost converter operate in CCM. Thus, if Y_{DCM} is positive, the proposed converter must operate in DCM. As shown in Fig. 4, operating state of converter is determined by d_1 , L and T_s . Larger T corresponds to wider duty cycle range. T can be kept constant by simultaneously reducing T_s and L . Higher switching

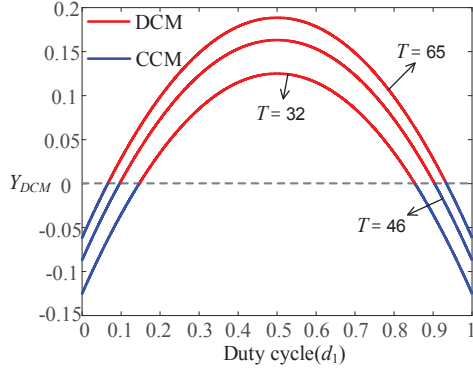


Fig. 4. The DCM conditions of the proposed converter.

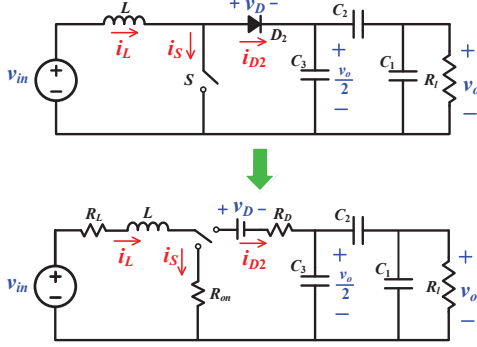


Fig. 5. Equivalent circuit in Boost mode with $v_{in} > 0$.

frequency helps to reduce the size of passive components and to increase the converter power density. However, higher switching frequency also increases the switching losses and core losses. A tradeoff among the size of passive components, the switching loss and DCM criteria should be taken into account in the design procedure.

The efficiency analysis of the converter operating as a boost converter for the positive input voltage is based on the following assumptions:

(1) In forward bias condition, the diode is modelled as a constant voltage source V_D in series with a resistor R_D . Moreover, the switching losses in the diode are neglected.

(2) Inductor current varies linearly. The equivalent series resistance R_L of the inductor is independent of its operating temperature.

(3) Power losses corresponding to the capacitors' equivalent series resistances are neglected.

When the converter operates in Boost mode, the equivalent circuit is shown in Fig. 5. The current waveforms i_L , i_D , i_S are shown in Fig. 3(a). The root mean square value of the inductor current over the whole switching cycle can be expressed as,

$$I_{L,RMS}^2 = \frac{1}{T_S} \int_0^{T_S} i_L^2(t) dt = \frac{i_{PK}^2 (d_1 + d_2)}{3} \quad (16)$$

The switch and the diode currents can be calculated in the same manner,

$$I_{S,RMS}^2 = \frac{1}{T_S} \int_0^{T_S} i_S^2(t) dt = \frac{i_{PK}^2 d_1}{3} \quad (17)$$

$$I_{D,RMS}^2 = \frac{1}{T_S} \int_0^{T_S} i_D^2(t) dt = \frac{i_{PK}^2 d_2}{3} \quad (18)$$

The inductor average current can be derived as,

$$I_L = \frac{1}{T_S} \int_0^{T_S} i_L(t) dt = \frac{i_{PK} (d_1 + d_2)}{2} \quad (19)$$

The diode average current can be expressed as,

$$I_D = \frac{1}{T_S} \int_0^{T_S} i_D(t) dt = \frac{i_{PK} d_2}{2} \quad (20)$$

The inductor loss can be expressed as,

$$P_{RL} = R_L I_{L,RMS}^2 = \frac{(d_1 + d_2) R_L i_{PK}^2}{3} \quad (21)$$

The MOSFET conduction loss is expressed as,

$$P_{RS} = R_{ON} I_{S,RMS}^2 = \frac{d_1 R_{ON} i_{PK}^2}{3} \quad (22)$$

The diode power loss is,

$$P_D = v_D I_D + R_D I_{D,RMS}^2 = \frac{d_2 v_D i_{PK}}{2} + \frac{d_2 R_D i_{PK}^2}{3} \quad (23)$$

The two MOSFETs are turned on and off simultaneously. Since they are turned on with zero current, the switching loss can be ignored.

The input current is equal to the inductor current. Hence, the input power can be expressed as,

$$P_{in} = v_{in} I_{in} = \frac{1}{2} (d_1 + d_2) v_{in} i_{PK} \quad (24)$$

The efficiency of converter can be expressed as,

$$\eta = 1 - \frac{P_{RL} + P_{RS} + P_D}{P_{in}} \quad (25)$$

Based on the above equations, we can get,

$$\eta \approx 1 - \left[\frac{2d_1 T_S (R_L + R_{ON})}{3L} - \frac{4R_{ON}}{3} \sqrt{\frac{L}{R_L T_S}} + \frac{4v_D}{V_P d_1} \sqrt{\frac{L}{R_L T_S}} \right] \quad (26)$$

According to Eq. (26), the greater R_L , R_{ON} , and v_D are, the smaller the efficiency is. With R_L , R_{ON} , and v_D equal to 0.1Ω , 0.1Ω , and 0.3 V respectively, the relationship between efficiency and duty cycle is illustrated in Fig. 6. Higher duty cycle corresponds to higher power level. When the duty cycle is bigger than 0.35, the efficiency decays with the increase of duty cycle. Moreover, the efficiency is also dependent on T . In order to achieve a high power level and a high efficiency, the tradeoff

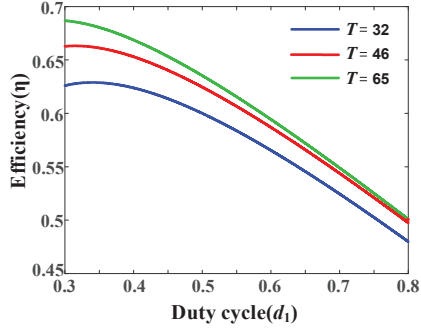


Fig. 6. Efficiency versus duty cycle and T .

TABLE I
PARAMETERS OF COMPONENTS

Component	Symbol	Parameters
Split capacitor	C_2, C_3	47 μF
Output capacitor	C_1	100 μF
N-channel MOSFET	S_2	20 V, 4.2 A
Load Resistance	R_l	240 Ω
P-channel MOSFET	S_1	20 V, 4.2 A
Schottky Diode	D_1, D_2	40 V, 3 A

between duty cycle and T should be considered in the design process. In this study, T is equal to 32.

V. SIMULATION RESULTS

To validate the steady state analysis of the proposed converter, a converter model is built in Simulink. The input voltage source is set as a 0.4 V, 100 Hz sinusoidal voltage. The circuit parameters are shown in Table I. A 240 Ω resistor is used to emulate the load. The switching frequency of the converter is 50 kHz. The output voltage is designed as 3.3 V. This system realizes closed loop control by detecting v_{c2} and comparing it with the reference voltage. The error is compensated by the proportional-integrator (PI) controller module to obtain the desired duty cycle. The simulation results are shown in Fig. 7. According to Fig. 7 (a), the proposed converter can boost 0.4 V amplitude ac voltage to 3.3 V dc voltage with small ripple. During a step change of the load resistance, the duty cycle decreases to maintain a constant output voltage, as shown in Fig. 7 (b).

VI. EXPERIMENT RESULTS

In order to minimize the size of proposed circuit, surface mounted devices are adopted. Schottky diodes with low forward voltage drop are used to reduce the diode losses. To minimize the conduction losses, low voltage rating MOSFETs with low on resistances are adopted. The n-MOSFET is IRLML2502; and p-MOSFET is IRLML6401. Tantalum capacitors are selected as the filtering capacitors since they have small leakage current and compact size. In this study, the micro-scale electromagnetic generator is emulated by a 0.4 V, 100 Hz ac voltage source. The output voltage is 3.3 V. The duty cycles of the converter are about 0.75 at 50 kHz. The ratings of selected components are shown in Table I.

The experiment results are shown in Fig. 8 and Fig. 9. As seen in Fig. 8, the input voltage is a 0.4 V and 100 Hz sinusoidal

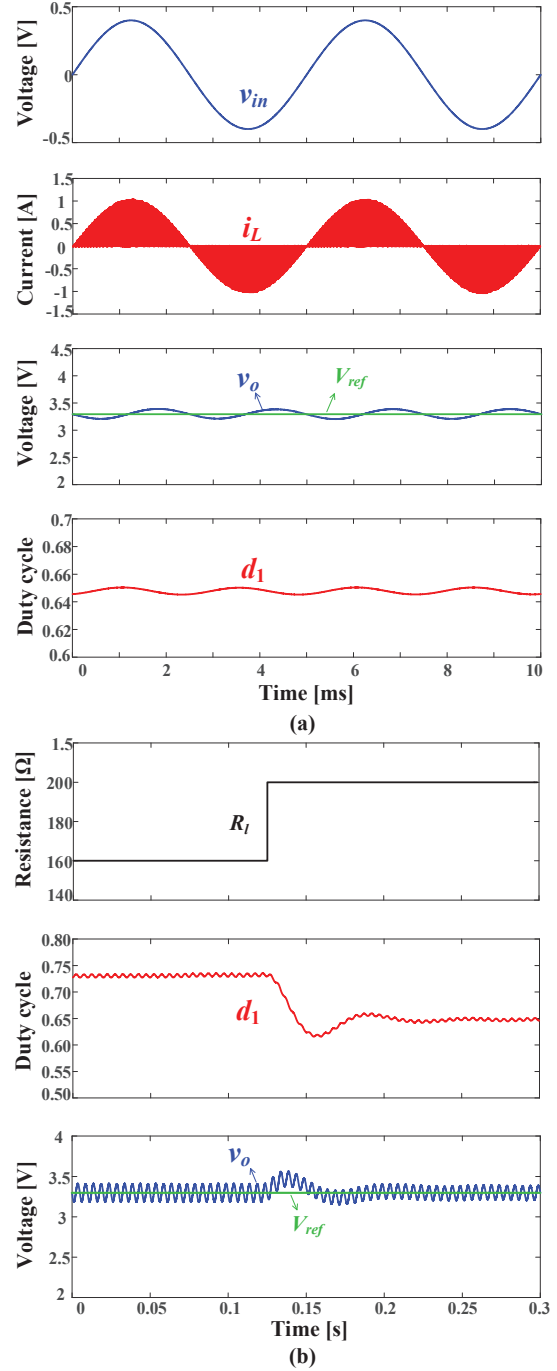


Fig. 7. Simulation results (a) steady state operation, b) load step response.

ac voltage. The inductor current envelop is synchronized with the input voltage at steady state. The inductor current for Boost mode operation is shown in Fig. 9. DCM operation can be observed.

VII. CONCLUSION

A novel ac/dc topology is proposed in this paper. The proposed single stage converter is able to rectify and step up low amplitude ac voltages. Therefore, it is suitable to be used in low-power micro-scale EM energy harvesting applications. This

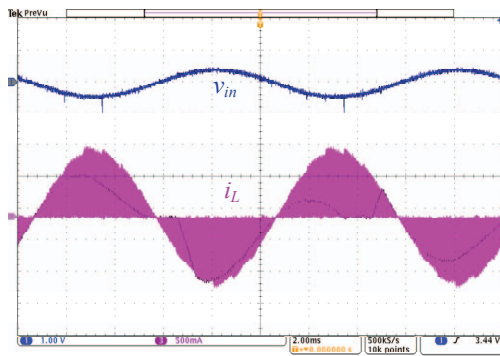


Fig. 8. From top to bottom: input voltage (1 V/div), inductor current (0.5A/div); time 2 ms/div.

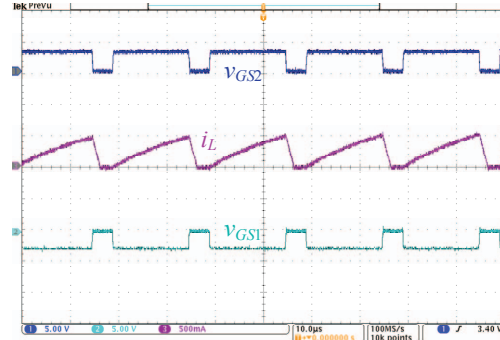


Fig. 9. Circuit waveforms in Boost mode operation, from top to bottom: gate source voltage of S_2 (5 V/div), inductor current (0.5 A/div), gate source voltage of S_1 (5V/div); time 10 μ s/div.

topology integrates the conventional Buck-Boost converter and Boost converter into a single stage with shared inductor and a four-quadrant switch. The proposed converter successfully avoids the introduction of complicated and lossy polarity detector. DCM operation is adopted to decrease the switching losses and to improve the efficiency. The operation and performance of the proposed converter is validated by simulation and experiment results. The designed prototype rectifies a 0.4 V 100 Hz ac input to a 3.3 V dc voltage. At 45 mW output power, the measured efficiency is 48%. Future efforts will focus on improving the efficiency.

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