Three-port Bidirectional CLLC Resonant Converter Based Onboard Charger for PEV Hybrid Energy Management System

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***Abstract*—In the hybrid energy management systems of plug in electric vehicles (PEVs), a power electronic interface (PEI) is required to interface among the grid side dc link, the onboard battery pack, and the ultra-capacitor (UC) bank. In this paper, an integrated three-port PEI is proposed for use in such applications. The PEI integrates the interleaved bidirectional buck/boost topology with the bidirectional CLLC resonant topology. Due to circuit reuse, the circuit components count is effectively reduced. The interleaved structure offers the benefits of increased power rating and reduced output ripples. The high power density UC bank smooths the current transients of the battery remarkably, which helps to extend the battery lifetime. Moreover, zero voltage switching (ZVS) and zero current switching (ZCS) are achieved among all power MOSFETs and diodes, respectively. A scaled down prototype rated at 1 kW is designed, optimized and tested to charge one 150 V to 250 V battery pack. By hybridizing the pulse-frequency modulation (PFM) and the pulse-width modulation (PWM), the switching frequency range is confined within 60.2 kHz-99.7 kHz. The output voltage/current ripples are well suppressed to meet the battery charging requirements. 96.14% conversion efficiency at rated power and good overall efficiency performance are reported.**

***Keywords*—CLLC*; plug-in electric vehicles (PEV); pulse-frequency modulation (PFM); pulse-width modulation (PWM); soft switching*.**

I. Introduction

Using battery/UC hybrid energy storage system (HESS) in PEVs could effectively increase the electric mileage, optimize the size of the energy storage system, and boost the battery life cycles [1]–[4]. A general structure of the PEV power management system with onboard charger and battery/UC HESS is illustrated in Fig. 1. As shown, an onboard charger is installed to charge the battery pack. Moreover, dc/dc converters are required in the HESS to interface different energy sources including the battery, UC, as well as the grid side dc link. Typically, these two modules are well separated.

The output characteristics of the PEV onboard charger should be matched with the charging requirements of the battery. A typical lithium-ion battery cell is typically featured with a 2.5 V~4.2 V voltage range. Thus, the dc/dc converter of the onboard charger should generate a wide voltage range. Moreover, the output voltage and current ripples should be suppressed to extend the lifetime of battery pack. Last but not the least, high conversion efficiency is expected when designing the dc/dc converter. LLC resonant converter is a popular topology in battery charging applications. This is mainly due to its features including soft switching and wide adjustable output voltage [5]–[7]. As the derivative of LLC resonant topology, CLLC resonant converter is also proposed in literature to achieve bidirectional power flow between vehicle and grid [8]–[10].

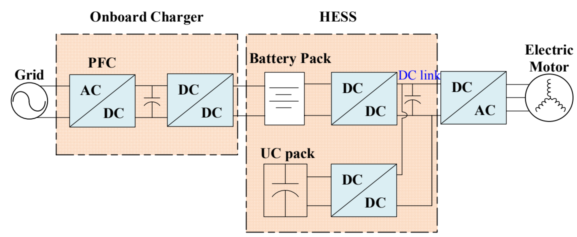

Fig. 1. Typical structure of the PEV power management system with onboard charger and battery/UC HESS.

For HESS part, the performance of the dc/dc converter determines the system efficiency and power management optimization. The topologies of HESS have been researched over the past few years. In [11], the battery pack is directly paralleled with the UC bank. This method simplifies the system complexity. However, it reduces the utilization of the energy stored in the UC. An active cascaded HESS is proposed in [12], where a dc/dc converter is added between the battery pack and the UC. However, since battery pack is connected directly to the dc link, the dc link voltage cannot be changed. A parallel active battery/UC system is proposed in [13]. Its disadvantage mainly lies in that more than one converters are needed and the system power density degrades. To cope with this issue, multi-input topologies are proposed to reduce the cost of the overall system [14].

In a different perspective, if the PEIs of the onboard charger and HESS are integrated, more advantages can be obtained including reduced cost, increased power density and improved efficiency. Following this insight, a three-port CLLC resonant converter based PEI is proposed in this paper. This PEI provides an integrated solution for the onboard charging system of the PEV battery/UC HESS. This multifunctional integrated PEI is able to effectively manage the power flows from a) grid to battery, b) battery to UC, c) UC to battery, and d) battery to grid.

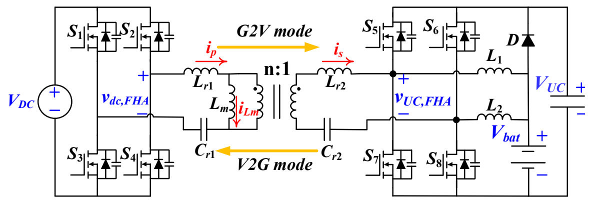

Fig. 2. Proposed three-port bidirectional CLLC resonant converter based onboard charger.

The paper is organized as follows: Section II provides a comprehensive analysis of the proposed PEI. Detailed design considerations are presented in Section III. Section IV shows the simulation and experimental results. Finally, Section V concludes this work.

II. Analysis of the Proposed Converter

A. Topology Description

The schematic of the proposed PEI is shown in Fig. 2. Indeed, it is the integration of a bidirectional full-bridge CLLC resonant converter and an interleaved bidirectional boost/buck converter. The secondary side power MOSFETs not only function as the rectification stage of the resonant converter, but also act as active switches and free-wheeling diodes of the interleaved converter. The CLLC resonant topology is adopted to enable a) a wide output voltage range, b) soft switching conditions of power MOSFETs, and c) bidirectional power flow capability. Interleaving structure is introduced to reduce battery charging current ripple and inductor size [15]. The high power density UC bank smooths the current transients of the battery. This would help to extend the battery lifetime.

This topology is featured with three working modes: a) grid to vehicle (G2V) mode when S_1~S_6 work as active switches and the grid charges the battery pack; b) vehicle to grid (V2G) mode when S_5~S_8 function as active switches and battery pack feeds power to the grid; and c) PEV driving mode when the primary side and resonant network is idle. In this paper, research efforts are concentrated on the topology verification and its implementation in G2V mode, where the PEI functions as an onboard charger.

B. Gain Analysis using the FHA model

In PEV G2V (charging) mode, on the primary side MOSFETs operate complementarily to generate a square wave (amplitude $\pm V_{dc}$, frequency f_s). This square wave is fed into the resonant network. On the secondary side, the UC functions as the intermediate input source for the interleaved buck converter, while the battery pack works as the load. S_5 and S_6 conduct as the active switches for the interleaved buck converter. Meanwhile, S_7 and S_8 are utilized as free-wheeling diodes. By modulating the switching frequency (f_s) and varying the duty cycle of S_5 and S_6, the desired charging voltage/current can be achieved.

Fig. 3 shows the equivalent circuit of the proposed charger using the first harmonic approximation (FHA) method. $V_{dc,FHA}$ is the root-mean-square (rms) value of $v_{dc,FHA}$, the fundamental component of v_{dc}. Similarly, $V_{UC,FHA}$ is the rms value of $v_{UC,FHA}$. They can be expressed as,

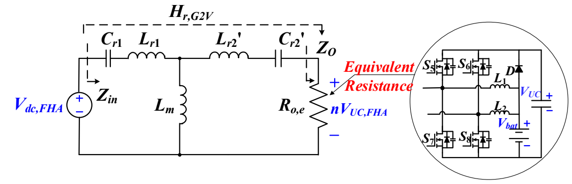

Fig. 3. The equivalent circuit for G2V (buck) mode under FHA.

$$V_{dc,FHA}=\frac{2\sqrt{2}}{\pi}V_{DC} \qquad V_{UC,FHA}=\frac{2\sqrt{2}}{\pi}V_{UC} \tag{1}$$

In charging mode, the interleaved buck converter can be equivalent to a resistor, whose resistance is,

$$R_{o,e}=\frac{8n^2}{\pi^2}\cdot\frac{R_{bat}}{D^2} \tag{2}$$

where, R_{bat} is the equivalent impedance of the battery pack using the first-order RC equivalent-circuit model of battery cell and D is S_5 and S_6's duty cycle.

The resonant network of the converter is composed of the series resonant capacitors C_{r1} and C_{r2}', the series resonant inductors L_{r1} and L_{r2}', and the magnetizing inductor L_m. The transfer function of the resonant network can be expressed as,

$$\begin{aligned} H_r &= \frac{V_{UC,FHA}}{nV_{dc,FHA}}=\frac{1}{n}\cdot\frac{Z_o}{Z_{in}} \\ &= \frac{1}{n}\cdot\frac{(R_{o,e}+Z_{C_{r2}'}+Z_{L_{r2}'})//Z_{Lm}}{Z_{C_{r1}}+Z_{L_{r1}}+(R_{o,e}+Z_{C_{r2}'}+Z_{L_{r2}'})//Z_{Lm}} \\ &\cdot\frac{R_{o,e}}{R_{o,e}+Z_{C_{r2}'}+Z_{L_{r2}'}} \end{aligned} \tag{3}$$

where, $L_{r2}' = n^2 L_{r2}$ and $C_{r2}' = C_{r2} / n^2$.

The gain of the resonant network is derived as:

$$\|H_r(f_n)\|=\frac{1}{n}\cdot\frac{1}{\sqrt{a^2+b^2}} \tag{4}$$

where,

$$a=k(1-\frac{1}{f_n^2})+1 \tag{5}$$

$$b=-Q\left[(kp+p+1)\cdot f_n-\left(kp+\frac{1+k}{q}+1\right)\cdot f_n^{-1}+\frac{k}{q}\cdot f_n^{-3}\right] \tag{6}$$

f_n can be represented by the first resonant frequency f_r; Q is the quality factor; and k is the ratio between the magnetizing inductance and the leakage inductance, respectively.

$$f_n=\frac{f_s}{f_r},\ f_r=\frac{1}{2\pi\sqrt{L_{r1}C_{r1}}},\ Z_r=\sqrt{\frac{L_{r1}}{C_{r1}}},\ Q=\frac{Z_r}{R_{o,e}},$$

$$k=\frac{L_{r1}}{L_m},\quad p=\frac{L_{r2}'}{L_{r1}},\ q=\frac{C_{r2}'}{C_{r1}}. \tag{7}$$

The gain of the interleaved buck converter in continuous conduction mode (CCM) is D. Using equations (1), (3) and (4), the gain of the whole charger can be obtained as,

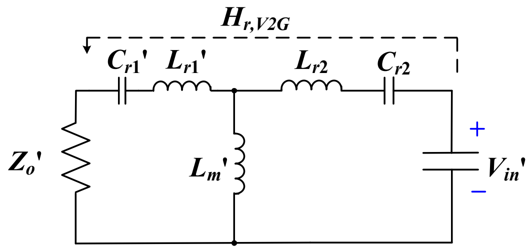

Fig. 4. The equivalent circuit for V2G (boost) mode under FHA.

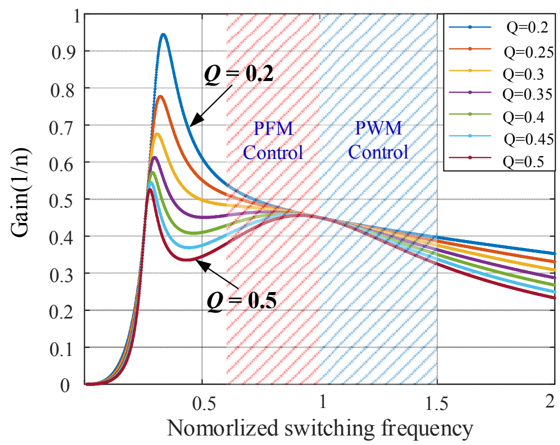

Fig. 5. Gain curves for G2V(buck) mode.

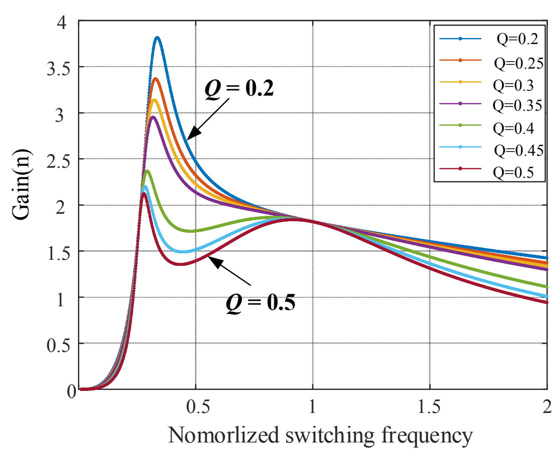

Fig. 6. Gain curves for V2G(boost) mode.

$$\begin{aligned}\|G(f_n)\|_{G2V} &= \left|\frac{V_{bat}(s)}{V_{DC}(s)}\right| = \left|\frac{D\cdot V_{UC}(s)}{V_{DC}(s)}\right| \\ &= D\cdot\|H_r(f_n)\| = \frac{D}{n}\cdot\frac{1}{\sqrt{a^2+b^2}}\end{aligned} \tag{8}$$

According to Eq. (4-8), by modulating the switching frequency and duty cycle of the buck converter, a desired output voltage can be obtained. Specific modulating methods will be given in the following part.

Similarly, the equivalent circuit for V2G (discharging) mode is shown in Fig. 4. In this model, $L_{r1}' = L_{r1} / n^2$ and $C_{r1}' = n^2 C_{r1}$ while $L_m' = L_m / n^2$, $R_{o,e}' = 8R_o / n^2\pi^2$. Note that in this mode S_7 and S_8 conduct as the active switches with the duty cycle D' for the interleaved boost converter. Gain of the whole charger under V2G mode can be derived as

$$\|G(f_n)\|_{V2G} = \frac{n}{1-D'}\cdot\frac{1}{\sqrt{c^2+d^2}} \tag{9}$$

where,

$$c = k'(1-\frac{1}{f_n'^2})+1$$

$$d = -Q'\left[(k'p'+p'+1)\cdot f_n' - \left(k'p'+\frac{1+k'}{q'}+1\right)\cdot f_n'^{-1} + \frac{k'}{q'}\cdot f_n'^{-3}\right]$$

$$f_n' = \frac{f_s}{f_r'},\ f_r' = \frac{1}{2\pi\sqrt{L_{r2}C_{r2}}},\ Z_r' = \sqrt{\frac{L_{r2}}{C_{r2}}},$$

$$Q' = \frac{Z_r'}{R_{o,e}'},\ k' = \frac{L_{r2}}{L_m'},\ \ p' = \frac{L_{r2}}{L_{r1}'},\ q' = \frac{C_{r2}}{C_{r1}'}. \tag{10}$$

Figs. 5 and 6 show the gain curves versus normalized frequency for G2V and V2G mode under different loads, respectively.

C. Soft Switching Conditions

In V2G mode, regarding the primary side active switches, the current should be sufficiently large to discharge the output capacitors of the four switches during the dead band. The dead time can be determined by,

$$t_{dead} \geq 8C_{oss} f_s L_m \tag{11}$$

where, t_{dead} is the dead time, and C_{oss} is the equivalent output capacitance of active switches.

Meanwhile, the duty cycle of S_5 and S_6 should be modulated to fit the desired voltage gain of the interleaved buck converter. It should be noted that S_5 and S_6 are switched with 180° phase difference. In order to realize ZVS, a synchronous rectifying technique is adopted and the duty ratio is constrained to be less than 0.5. Switch pattern of the actively controlled MOSFETs can be seen in Fig. 7.

D. Control Strategy

Conventionally, the dc link voltage of a two-stage PEV onboard charger is set as constant. This means the dc/dc converter should have a wide gain range to fit the wide battery pack voltage range. For PFM converters, this means a wide frequency range is required. This wide frequency range forces the converter operation to deviate from its optimal frequency.

To cope with this issue, this paper proposes an optimal PFM+PWM control strategy to ensure both soft switching and wide output range characteristics. This strategy is illustrated in Fig. 7. The control method is to utilize PFM control strategy to achieve higher voltage gain, and to utilize PWM control strategy to decrease the output voltage. Specifically speaking, switching frequency of S_1~S_6 is reduced simultaneously under the original fixed duty cycle D

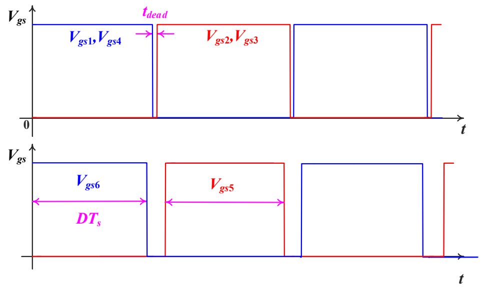

Fig. 7. Switch pattern of the actively controlled MOSFETs in G2V mode.

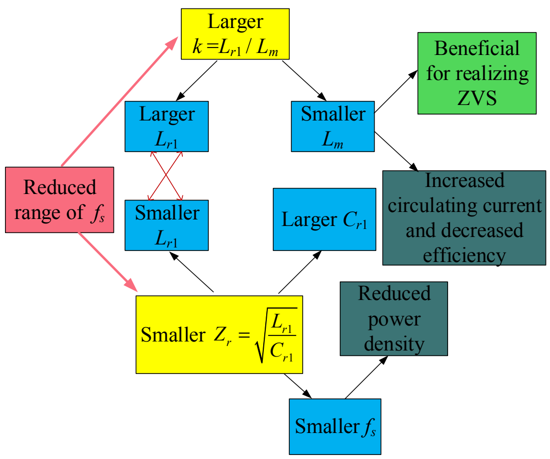

Fig. 8. Diagram of the design considerations.

of S_5 and S_6 to achieve higher voltage gain; while D of S_5 and S_6 is decreased when all switches work at resonant frequency f_r, in order to realize lower voltage gain. Thus, a wide output range can be achieved skillfully. The specific modulation range will be given in Section IV.

III. Parameter Optimal Design Procedure

As analyzed in Section II, the voltage gain in Eq. (8) is the function of multiple parameters. However, it is difficult to solve all of these parameters simultaneously. This is because there are different constrains for different parameters. The relationship between design considerations of those parameters is shown in Fig. 8. To solve this design challenge, we firstly choose a desired resonant frequency, and then select the other parameters according to a certain iteration process. Therefore, the optimization design procedure is outlined by the following steps.

1) Choose a proper value for resonant frequency f_s.

2) Determine L_m according to Eq. (11).

3) Sweep parameter $k = L_{r1}/L_m$ under full load condition. The diagram of converter gain is illustrated in Fig. 9. As shown, in order to accommodate a wide output range and a relatively narrow frequency modulation range, parameter k should be designed as large as possible.

4) Sweep parameter $Z_r = \sqrt{L_{r1}/C_{r1}}$ under full load condition. The gain plot is shown in Fig. 10. As shown, when

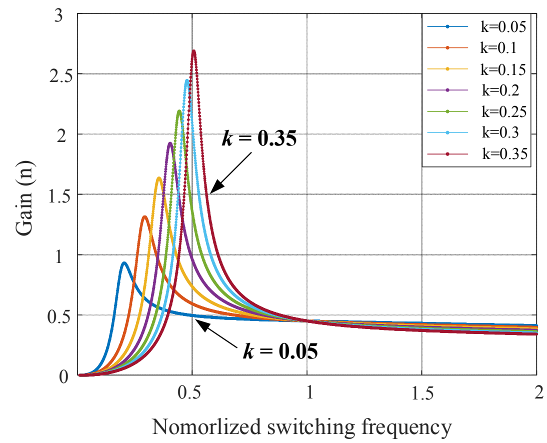

Fig. 9. Curves of gain versus switching frequency with different values of k.

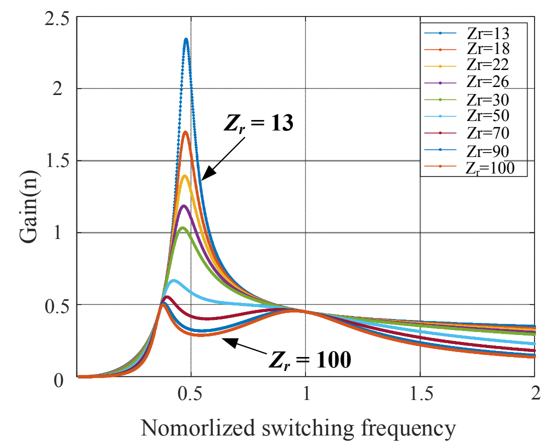

Fig. 10. Curves of gain versus switching frequency with different values of Z_r.

Z_r is sufficiently large, there will be two local maximum points on the gain curve. This is unfavorable for the purpose of output voltage modulation. Hence, a smaller Z_r is desired. On the other hand, a smaller Z_r could also accommodate a wide output range and a narrow frequency range.

5) Determine L_{r1} and C_{r1} according to Eq. (7). In order to realize relatively symmetric bidirectional charging characteristics, we set the transformer turns ratio as unity. The resonant capacitors and inductors on both sides are designed with identical values.

6) Calculate the attainable maximum dc gain according to Eq. (4-8). If the dc gain under the specific situation fulfills the requirement, we proceed to the next step. Otherwise, we go back to step 3) to reset a new k.

7) Choose proper value for L_1 and L_2 in the interleaved buck converter. Firstly, assume the converter is working in CCM. Then the inductance can be calculated utilizing the following equation,

$$L = (V_{UC,\max} - V_{bat}) \cdot \frac{V_{bat}}{V_{UC,\max}} \cdot f_s \cdot \frac{1}{LIR \cdot I_{bat,\max}} \tag{12}$$

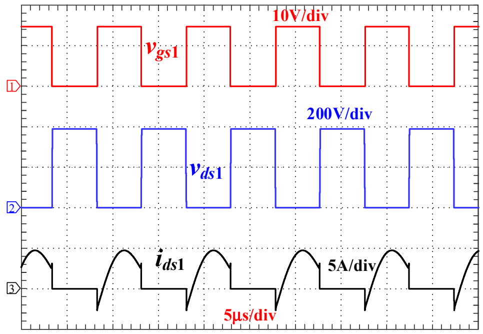

Fig. 11. ZVS turning-on of primary side MOSFET S_1.

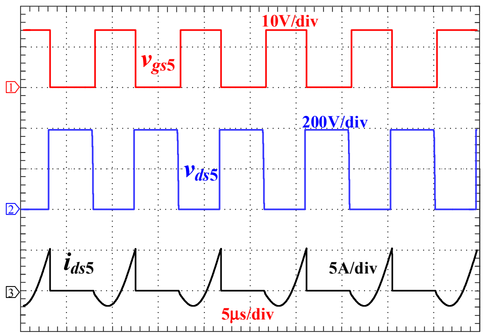

Fig. 12. ZVS turning-on of secondary side MOSFET S_5.

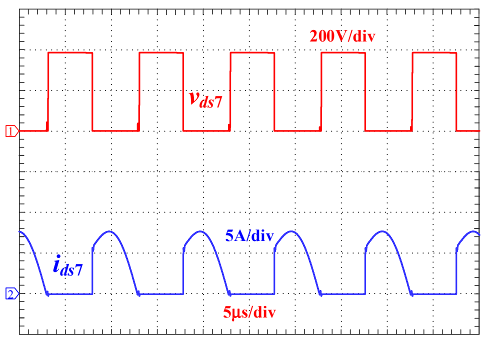

Fig. 13. ZCS turning-off of body diode of S_7.

where, LIR is the inductor-current ratio expressed as a percentage of I_{bat}. An LIR of 0.3 represents a good tradeoff between efficiency and load-transient response [16].

IV. Simulation and Experimental Results

In order to validate the concept, a converter model is designed in Simulink to charge a 150 V~250 V battery pack. The design parameters are listed in Table I.

Fig. 11 illustrates the voltage and current waveforms of the primary side MOSFET S_1. It is shown that the body diode conducts prior to gate source pulse. This provides zero voltage condition for the turning on of the MOSFET. Therefore, ZVS is achieved during the MOSFET turn-on process. The turning on conditions of S_2, S_3, and S_4 are similar to that of S_1.

Fig. 12 demonstrates the voltage and current waveforms of the active switch for the interleaved buck/boost converter, S_5. Likewise, the body diode of the S_5 conducts before the

Table I

Design Parameters

Parameter	Symbol	Quantity
Input voltage	V_{DC}	390V
Output voltage	V_{out}	150V-250V
Rated power	P_{max}	1 kW
Resonant inductor	L_{r1}, L_{r2}	20.5 μH
Resonant capacitor	C_{r1}, C_{r2}	122 nF
Magnetizing inductor	L_m	210 μH
Ultracapcacitor	C_{UC}	1760 μF
Resonant frequency	f_r	99.7kHz
Duty cycle	D	0.36 ~ 0.46
Switching frequency	f_s	60.2 ~ 99.7 kHz
Transformer turns ratio	n	1
MOSFET	S_1~S_8	C3M0120090D

conduction of MOSFET channel, which guarantees the MOSFET ZVS turning-on. It is the same case with S_6.

Fig. 13 shows the voltage and current waveforms of S_7. In G2V mode, S_7 functions as a freewheeling diode without being controlled. As shown, S_7 turns off with small di/dt, which guarantees ZCS turning-off of its body diode. Similarly, S_8 could also realize ZCS turning-off.

By hybridizing PFM and PWM control strategy, switching frequency of the converter is constrained between 60.2 kHz and 99.7 kHz. And the duty cycle D of the interleaved buck converter ranges from 0.36 to 0.46. Both conditions facilitate the 150V~250V wide output voltage range. Fig. 14 shows control signals of S_2 and S_5 under the switching frequency of 60.2 kHz and the duty cycle of 0.46. 250 V output voltage can be achieved in this situation. Fig. 15 shows the control signals of S_2 and S_5 under resonant frequency (99.7 kHz). The duty cycle of S_5 and S_6 is 0.36. It is shown that 150V output voltage is achieved.

A 1 kW prototype is implemented to verify the theoretical analysis and simulation results. Parallel arrays of eight 220-μF electrolytic capacitors are used to emulate the UC bank while battery pack is emulated by a programmable electric load (Chroma Model 63212). Critical steady state voltage and current waveforms are captured in Figs. 16 and 17. Fig. 16 shows v_{ds1}, v_{gs1}, and the transformer primary side current i_p. It is shown that ZVS is achieved during the MOSFET turn-on process. Fig. 17 shows v_{ds5}, v_{gs5}, and the transformer secondary side current i_s. We can easily find that ZVS of the active switch for the interleaved buck converter is achieved. Moreover, there is no steep change of i_s. This means that the reverse recovery process can be eliminated during the turning off of S_7 and S_8. Therefore, soft switching is realized among all switches. Thus, the switching loss is effectively reduced.

The PFM+PWM hybrid control strategy also brings benefits. This is validated in experimental measurement. With only PFM control, the switching frequency need to swing within [60.2 kHz, 150 kHz] to achieve identical output voltage range.

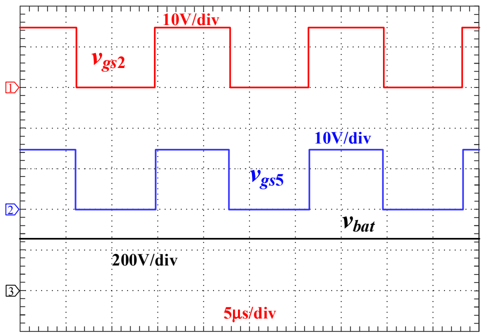

Fig. 14. Simulated waveforms of v_{gs2}, v_{gs5} and output voltage v_{bat} under 250 V output voltage.

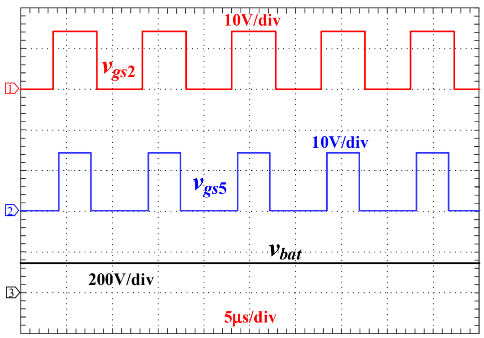

Fig. 15. Simulated waveforms of v_{gs2}, v_{gs5} and output voltage v_{bat} under 150 V output voltage.

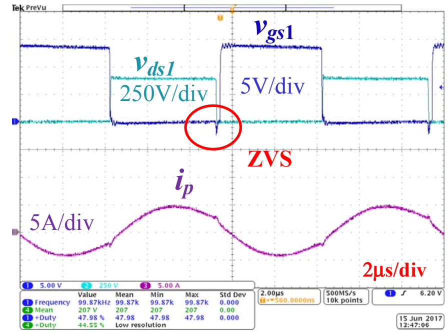

Fig. 16. Experimental waveforms of v_{ds1}, v_{gs1} and the transformer primary side current i_p.

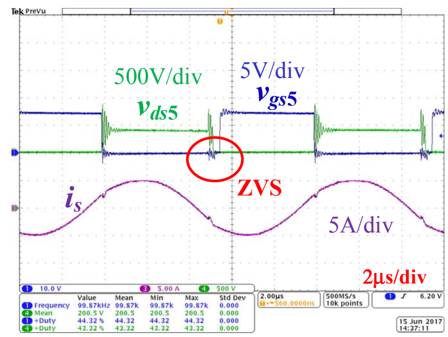

Fig. 17. Experimental waveforms of v_{ds5}, v_{gs5} and the transformer secondary side current i_s.

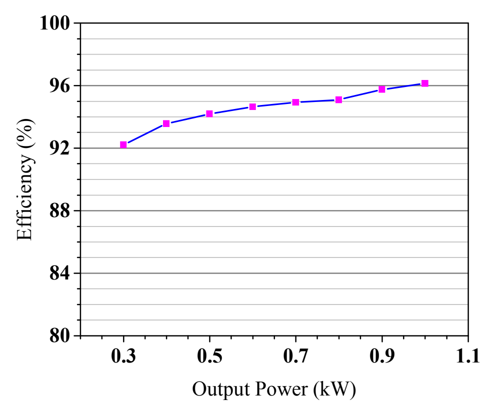

Fig. 18. Conversion efficiency versus output power.

A high precision power analyzer (N4L PPA4530) is used to calibrate the conversion efficiency of the prototype. Fig. 18 shows the measured efficiency versus output power under constant 190V output voltage. 96.14% peak conversion efficiency is captured with 390V input voltage at rated 1 kW. Moreover, with the reduction of output power, there is no sharp drop of conversion efficiency. 94.19% efficiency is achieved under 500W output power and the data is 92.21% for 300W output power. Worst scenario efficiency is also considered as acceptable. The efficiency for 250 V output voltage is 93.9% while it is 94.37% for 150 V output voltage, both at rated 1 kW output power.

V. Conclusions

This paper proposes a novel PEI for HESS in PEV applications. It is the integration of a CLLC resonant converter and an interleaved bidirectional buck/boost converter. The proposed PEI provides advantages including a) a wide output voltage range for battery charging via combination of PFM+PWM; b) all switches working in soft switching state under all load conditions; c) increased power rating and reduced output voltage/current ripples, and d) bidirectional working modes. Parameter optimal design procedure is presented to facilitate the design process. A converter prototype rated at 1 kW is designed and implemented for G2V mode. Results have been given to verify the theoretical analysis and simulation results. 96.14% peak conversion efficiency is reported at rated power.

In future work, experiment with UC bank will be implemented to verify the benefits of the proposed PEI. Power losses and efficiency will be analyzed. V2G working pattern will be further investigated.

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