A LLC Type Resonant Converter Based on PWM Voltage Quadrupler Rectifier with Wide Output Voltage

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Abstract—In a typical plug-in electric vehicle onboard charger, the input voltage of the second stage dc/dc converter is usually kept constant while the battery pack voltage varies in a wide range with the change of battery state of charge. In this application, it is extremely difficult to tune the operation of traditional LLC resonant converter close to its resonant frequency. In this paper, a novel pulse width modulated (PWM) LLC type resonant converter based on voltage quadrupler rectifier is proposed. The proposed converter always operates at the resonant frequency and is able to achieve a wide output voltage range. Zero-voltage-switching (ZVS) and zero-current-switching (ZCS) are realized among all power MOSFETs and all power diodes, respectively. A 1.3 kW converter prototype, generating 250 V–420 V output voltage from the 390 V dc link, is analyzed and designed to verify the effectiveness and the advantages of the converter.

Keywords—LLC; plug-in electric vehicle; PWM; voltage quadrupler; wide output voltage; ZVS

I. INTRODUCTION

A typical plug-in electric vehicle (PEV) onboard battery charger consists of two stages: a) the front end ac/dc converter for rectification and power factor correction, and b) the second stage dc/dc converter for voltage/current regulation and galvamic isolation[1]–[4]. High power density, and high efficiency are desired features for onboard chargers. Thus, the conversion efficiency of both stages should be improved together. Since the front-end non-isolated PFC typically utilizes standard topology and is highly efficient, the main challenge is to improve the efficiency of the second stage dc/dc converter [5].

As shown in Fig. 1, this second stage dc/dc converter is usually composed of a high frequency inverter, an optional resonant network for resonant converter, a high frequency transformer, the rectifier network, as well as the output port filter network.

The LLC resonant converter is considered as a good candidate to be employed in the second stage dc/dc converter of the PEV onboard chargers[6]–[8]. This is mainly because in LLC resonant converters, all the active switches can achieve ZVS and all the diodes turn off with ZCS over the entire load range [9]–[11]. While in the application of PEV onboard charging, the output voltage should be in a wide voltage variation range (typically 250V - 420V for battery vehicles). To make the LLC topology adaptable to this wide voltage range, different methods have been proposed in [12]–[14].

Since LLC converter is a pulse frequency modulated topology, this means switching frequency (fs) must swing in a wide range to fit this wide voltage gain range. This phenomenon can be observed clearly from the curves of LLC resonant converter output voltage versus normalized switching frequency in Fig. 2. This wide fs range makes fs deviate from the resonant frequency (fo); the conversion efficiency degrades fast.

To alleviate this problem, different modified LLC type topologies are investigated [15]–[17]. In [15], the converter actively reconfigures its secondary side rectifier from voltage-doubler structure to voltage-quadrupler structure according to different load conditions. However, it still employs frequency modulation without eliminating the above mentioned issue. For [16], phase shift control is adopted on the secondary side. This compensates the switching frequency deviation in hold-up mode. In [17], a pulse width controlled topology in secondary side is proposed to regulate the output voltage; fs is constant and equal to fo. However, the voltage stresses of the secondary side components are high and equal to the output voltage. Thus, it is not a preferred candidate for high voltage applications.

In this paper, a novel LLC type resonant topology is proposed. This proposed converter achieves an ultra-wide
output voltage range with $f_s$ fixed and tuned to $f_r$. The charging voltage and current are regulated by modulating the duty cycle of the secondary side MOSFET. This proposed converter demonstrates benefits including: a) optimum operation of the main LLC power circuit; b) ZVS turning on of all active switches; c) ZCS turning off of diodes on the secondary side; d) reduced circuit control complexity; f) reduced components voltage stresses on the second side; and e) reduced circulating current and conduction losses.

II. PROPOSED CONVERTER

A. Topology Description

The schematic of the proposed converter is plotted in Fig. 3. The primary side structure of this topology is the same as the full bridge LLC resonant converter: all switches have a constant duty cycle close to 0.5. To prevent the circuit shoot through, the upper and lower power MOSFETs are turned on and off complementarily with certain deadband ($t_{dead}$). The secondary side structure is derived from conventional voltage quadrupler rectifier, which is composed of six diodes, four capacitors and one two-quadrant switch. As shown, an active switch (S3) is added on the secondary side. And the output voltage can be regulated by actively controlling the duty cycle of S5. Therefore, the main LLC topology can always operate at its resonant frequency.

B. Operation Principle

In the proposed converter, the primary side full bridge generates a constant frequency (equals to $f_r$) square waveform. While on the secondary side, S5’s switching frequency is also equals to $f_r$.

If the duty cycle of $S_1$, $d$ is below 0.25 or higher than 0.75, the output will be a constant voltage. This means that the converter loses its PWM feature. Therefore, to maintain an effective pulse width modulation, $d$ should be constrained within the range of [0.25, 0.75]. However, it is also worth to mention that: a) when $d$ is within [0, 0.25), the converter secondary side is equivalent to a voltage-doubler rectifier (VDR); b) when $d$ is within (0.75, 1], the converter secondary side is equivalent to a voltage-quadrupler rectifier (VQR).

1) VDR Mode: The key waveforms in VDR mode ($d=0$) is shown in Fig. 4(a). In this mode, the operation principle is similar to the conventional LLC resonant converter. The equivalent circuit is plotted in Fig. 5(a). If $d$ is 0, S5 functions as a diode, and $D_{3,4}$ are off. According to the conventional LLC resonant converter operation, all the switches and diodes can achieve ZVS and ZCS, respectively. Meanwhile, voltage balance for $C_3$ and $C_4$ can be easily achieved. Therefore, the voltages across $C_3$ or $C_4$ are equal to half of the output voltage. In this mode, the output voltage is defined as,

$$ V_o = \frac{2V_{DC}}{n} $$

(1)

where $n$ is the transformer turn ratio.

2) VQR Mode: The key waveforms of the converter in the VQR mode ($d=1$) are shown in Fig. 4(b). In this mode, the operation principle is also similar to the conventional LLC resonant converter. The equivalent circuit is shown in Fig. 5(b). If $d$ is 1, S5 is on and $D_{3,4}$ are off. The circuit operation is similar to that in the VDR mode. All the MOSFETs and diodes can achieve ZVS and ZCS, respectively. Meanwhile, the voltages across $C_3$ and $C_4$ are equal to half of output voltage. The sum of the voltages across $C_3$ and $C_4$ also equals to half of output voltage. The output voltage is defined as,

$$ V_o = \frac{4V_{DC}}{n} $$

(2)

3) Normal Mode: It should be noted that there is a secondary resonant frequency ($f_m$) in the LLC resonant tank. This corresponds to the resonance where the magnetizing inductor ($L_m$) participates.
One specific switching period, $t_6$, $t_7$, and $i_f$ reach zero. Meanwhile, $i_L$ intersects with $i_{DS}$. In the mode VI, the zero current turn-off of rectifier $D_3$ is achieved.

Mode VII $[t_6, t_7]$. Mode VII begins at $t_6$ when $S_{2,3}$ are turned off simultaneously. In the beginning of Mode VII, $i_f$ discharges and charges the output capacitors of $S_{1,4}$, and then flows through the body diodes of $S_3$ and $S_5$. Thus, $V_{dc}$ is inverted from $-V_{dc}$ to $V_{dc}$ while $i_f$ is kept zero.

Mode VIII $[t_7, t_8]$. At $t_7$, $S_{1,4}$ are both turned on with zero voltage. The voltage across $L_m$ is $nV_1$. During Mode VIII, on the secondary side, $D_5$ and $D_8$ continue to conduct, and $i_f$ changes to positive. $i_L$ continues to increase linearly since the voltage across the $L_m$ is positive. Mode IX ends when $S_5$ is turned off.

Mode X $[t_8, t_9]$. Mode X starts as $S_5$ is turned off at $t_8$. Since $i_f$ continues, the current path is switched from $S_5$ to $D_7$. Hence, the voltage across $L_m$ is $n(V_1 + V_3)$. $i_L$ continues to increase linearly in this operation mode. Mode X ends when $i_f$ reaches zero.

Mode XI $[t_9, t_{10}]$. At $t_9$, $i_f$ reaches zero. Meanwhile, $D_{2,3,6}$ turn off with zero current. Mode XI ends when $S_1$ and $S_4$ are turned off.

Mode XII $[t_{10}, t_{11}]$. Mode XII begins in the deadband at $t_{11}$. Similarly, $i_f$ discharges and charges the output capacitors of $S_1$ and $S_4$, and then flows through the body diodes of $S_2$ and $S_5$. Mode XII ends when the switch pattern of $S_5$ is inverted again, which denotes the start of the next switching period.

The switching frequency is designed above $f_m$ to ensure that the resonant tank works in the inductive region. This would facilitate the ZVS condition for all switches.

The key steady state waveforms of the converter in the normal mode $d = 0.5$ are plotted in Fig. 6. As shown, the time delay, $\tau = 0.25T_m$, is enforced between the turning on of $S_2$ and $S_4$. In each switching cycle, there are 12 different operating modes. One specific switching period, $[t_6, t_{12}]$, is extracted for detail analysis. Those operating modes correspond to 12 equivalent circuits as plotted in Fig. 7.

The operating modes analysis is based on the assumption that $C_{1,2}$ are sufficiently large such that their voltage ripples can be ignored. Thus, those capacitor voltages are considered as dc voltages, $V_{1,2}$, respectively.

Mode I $[t_0, t_1]$. At $t_0$, the body diodes of $S_2$ and $S_1$ are conducting. This creates a zero voltage condition for the turning on of the MOSFETs. At $t_0$, the MOSFETs ($S_2$ & $S_5$) channels are turned on with ZVS, and $S_4$ is off. The voltage across $L_m$ is $n(V_1 - V_3)$. As shown in Fig. 6, the secondary side current, $i_f$, is negative, the body diode of $S_5$ and $D_3$ start to conduct. Mode I ends when the current through the inductor ($i_{DS}$) reaches zero.

Mode II $[t_1, t_2]$. Mode II begins at $t_1$ when $D_3$ begins to conduct. The current through $L_m$ ($i_{DS}$) continues to decrease linearly.

Mode III $[t_2, t_3]$. Mode III begins at $t_2$ when $i_f$ changes to be negative. $L_f$ continues to resonate with the resonant capacitor ($C_r$), $i_f$ keeps flowing through the body diode of $S_5$. Mode III ends when the $S_5$ is turned on.

Mode IV $[t_3, t_4]$. At $t_3$, $S_5$ is turned on with ZVS. In the previous mode, $i_f$ goes through the body diode of $S_5$. Before the $S_5$’s channel conducts, the voltage across $S_5$ has been discharged to be zero. Hence, ZVS can be achieved on $S_5$. In mode IV, $i_f$ goes through the channel of $S_5$ instead of its body diode.

Mode V $[t_4, t_5]$. At $t_4$, the current through the rectifier $D_3$ ($i_{DS}$) reaches zero. In this mode, the zero current turn-off of rectifier $D_3$ is achieved. $D_3$ is off during this mode.

Mode VI $[t_5, t_6]$. Mode VI begins at $t_5$ when $i_{DS}$ and $i_f$ reach zero. Meanwhile, $i_L$ continues with $i_{DS}$. In the mode VI, the zero current turn-off of rectifier $D_3$ is achieved.

Mode VII $[t_6, t_7]$. Mode VII begins at $t_6$ when $S_{2,3}$ are turned off simultaneously. In the beginning of Mode VII, $i_f$ discharges and charges the output capacitors of $S_{1,4}$, and then flows through the body diodes of $S_3$ and $S_5$. Thus, $V_{dc}$ is inverted from $-V_{dc}$ to $V_{dc}$ while $i_f$ is kept zero.

Mode VIII $[t_7, t_8]$. At $t_7$, $S_{1,4}$ are both turned on with zero voltage. The voltage across $L_m$ is $nV_1$. During Mode VIII, on the secondary side, $D_5$ and $D_8$ continue to conduct, and $i_f$ changes to positive. Mode VIII ends when $i_f$ reaches zero.

Mode IX $[t_8, t_9]$. At $t_8$, $i_f$ begins to change its polarity to positive. $i_L$ continues to increase linearly since the voltage across the $L_m$ is positive. Mode IX ends when $S_5$ is turned off.

Mode X $[t_9, t_{10}]$. Mode X starts as $S_5$ is turned off at $t_9$. Since $i_f$ continues, the current path is switched from $S_5$ to $D_7$. Hence, the voltage across $L_m$ is $n(V_1 + V_3)$. $i_L$ continues to increase linearly in this operation mode. Mode X ends when $i_f$ reaches zero.

Mode XI $[t_{10}, t_{11}]$. At $t_{10}$, $i_f$ reaches zero. Meanwhile, $D_{2,3,6}$ turn off with zero current. Mode XI ends when $S_1$ and $S_4$ are turned off.

Mode XII $[t_{11}, t_{12}]$. Mode XII begins in the deadband at $t_{11}$. Similarly, $i_f$ discharges and charges the output capacitors of $S_1$ and $S_4$, and then flows through the body diodes of $S_2$ and $S_5$. Mode XII ends when the switch pattern of $S_5$ is inverted again, which denotes the start of the next switching period.
III. CHARACTERISTICS AND DESIGN CONSIDERATIONS

A. Equivalent Circuit Model

Based on the steady state analysis in Section II-B, the equivalent circuit model of the proposed topology can be obtained. The following analysis is based on the assumption that the relatively narrow time intervals, \(t_5-t_7\) and \(t_1-t_2\), can be neglected. Moreover, the voltage source and the impedance on the secondary side of the transformer can be pushed to the primary side with certain ratio. The resultant equivalent circuit model of the converter and the corresponding current waveforms are plotted in Fig. 8 and Fig.9, respectively.

B. Voltage Conversion Relationship

As shown in Fig. 8, in State I, the input voltage source reverts its polarity. \(L_r\) resonates with \(C_r\). This is similar to VQR mode as analyzed in Section II-B. The peak value of \(i_{Lm}\) is,

\[
i_{Lm_{-peak}} = \frac{V_{dc}}{4L_r f_r}
\]

In State II, the output voltage source is changed from \(nV_{C2}\) to \(nV_{C1}\). \(i_{Lm}(t)\) begins to increase from \(-i_{Lm_{-peak}}\). \(i_{Dp}(t)\) increases from zero. According to the bottom figure in Fig. 9, the average of \(i_{Dp}(t)\) equals to the output current, \(i_o\). Therefore, the peak value of the current through \(D_h\) is,

\[
i_{Dh_{-peak}} = \frac{4V_o}{3R(d - 0.25)}
\]

Thus, the peak value of \(i_{Lr}\) is,

\[
i_{Lr_{-peak}} = \frac{8V_o}{3Rn(d - 0.25)}
\]

Assuming the voltage on \(C_r\) is sine wave, its peak value is

\[
V_{C_r_{-peak}} = \frac{8\sqrt{2}\pi L_r f_r V_o}{nR}
\]

In State III, the output voltage source is changed to \(nV_{C4}\). \(i_{Lr}(t)\) begins to decrease from \(i_{Lr_{-peak}}\). In State IV, no power is delivered to the secondary side.

Based the law of energy conservation and assuming the converter is ideal without intermediate energy losses, the input energy is equal to the energy delivered to the battery pack. Thus, the output voltage can be derived as,
Fig. 9 plots the output voltage versus the effective load resistance, and the duty cycle. As shown in Fig. 9, the output voltage is a strong function of the duty cycle and a weak function of the effective load resistance. This means that the voltage gain can be easily regulated by the pulse width modulation.

\[ V_o = \frac{12 V_{in} R n D}{4 L_m f_r D + f_r} + \frac{4 V_{in}}{n} \]

\[ (8) \]

Fig. 9. Gate signals and simplified current waveforms.

C. Design Consideration

\( f_r, Q \) and \( L_m \) are the resonant frequency, quality factor, and inductor ratio.

\[ f_r = \frac{1}{2\pi \sqrt{L_r C_r}} \]

\[ Q = \sqrt{\frac{L_r}{n^2 R}} \]

\[ (9) \]

\[ (10) \]

Fig. 10. Voltage gain versus equivalent \( R \) and \( D \).

The LLC module always operates at \( f_r \) and has no voltage regulation capability. Thus, since the increase of \( L_m \) reduces the circuiting current, \( L_m \) should be designed to be as large as possible. While the upper limit of \( L_m \) can be found based on the ZVS requirement.

According to the aforementioned operational principles analysis, once the output capacitance of MOSFET (\( C_{oss} \)) is discharged to zero and the body diode of the MOSFET is in the ON-state during \( t_{dead} \), ZVS of switch is achieved. Fig. 11 illustrates the output capacitance charging/discharging processes for primary-side MOSFETs. In Fig. 11, \( i_{Lm, peak} \) is the peak value of \( i_{Lm} \), and can be calculated by Eq.4.

In order to improve the accuracy of analysis, the transformer primary side parasitic capacitance \( C_{tr} \) should be considered. Thus,

\[ L_m = \frac{L_m}{L_r} \]

\[ (11) \]

where, \( R \) is the output load resistance. \( f_r, Q \) and \( L_m \) can be designed based on the first-harmonic approximation method. The detail design consideration has been discussed comprehensively in [18], [19].

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In order to improve the accuracy of analysis, the transformer primary side parasitic capacitance \( C_{tr} \) should be considered. Thus,

\[ L_m \leq \frac{i_{dead}}{8 \left( C_{oss} + \frac{1}{2} C_0 \right) f_r} \]

\[ (12) \]

A tradeoff should be made between the \( L_m \) and \( i_{dead} \).

IV. RESULTS

To verify the effectiveness of the proposed converter, a 390 V input, 250 V - 420 V output, 1.3 kW, 100 kHz converter prototype is designed and tested. The specifications and design parameters are summarized in Table I.
Theoretical predicted output voltage curve versus $d$ is plotted in Fig. 12, where the simulated and experiment data is also marked. As shown in Fig. 12, with the duty cycle increases, the output voltage increase. The theoretical predicted results generally agree with the simulation and experiment results. It should be noted that the error is mainly due to the approximation and simplification adopted in the circuit modeling.

Fig. 13 shows the converter operation in VDR mode at $f_r$. As can be observed, the ZVS of the switch $S_4$ is achieved. $i_L$ lags $v_{ab}$ under 390 V input.

Fig. 14 shows the converter operation in VQR mode at $f_r$. At this operating point, waveforms of $i_L$ and $v_C$ are captured. The waveforms prove that the LLC resonant tank is inductive.

Figures 15 and 16 demonstrate the circuit operations at normal mode with output equals to 420 V. As shown in Fig. 15, the body diode of the $S_5$ conducts before the conduction of MOSFET channel. This guarantees the ZVS turning on of $S_5$. As shown in Fig. 16, $v_{ds1}$ and $v_{ds3}$ drop to zero before the conduction of MOSFET channels. $i_L$ contributes to charge and to discharge the parasitic capacitors of MOSFETs. Therefore, ZVS is achieved both on the primary side MOSFETs. The measured conversion efficiency reaches 92.62%.

V. CONCLUSIONS

In this paper, a novel PWM LLC type resonant converter is proposed for use in PEV onboard chargers. The circuit operation principles are analyzed. The advantages of the proposed converter are detailed. The converter can always operate at its resonant frequency by adopting pulse width modulation on the secondary side. Meanwhile, it is worth to mention that hybridizing pulse width and frequency modulations is also feasible. This hybridization increases the output voltage range with reduced normalized voltage gain range of the LLC topology. A 1.3 kW converter prototype is designed to verify the

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<th>Symbol</th>
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<tr>
<td>$V_i$</td>
<td>Input voltage</td>
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</tr>
<tr>
<td>$V_o$</td>
<td>Output voltage</td>
<td>250 V – 420 V</td>
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<tr>
<td>$L_r$</td>
<td>Resonant inductor</td>
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<tr>
<td>$C_r$</td>
<td>Resonant capacitor</td>
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<td>$n$</td>
<td>Transformer turns ratio</td>
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proof of concept. The proposed converter topology is not only useful for PEV battery charging application, but also worthy approaching in applications where wide voltage gain range is desired.

REFERENCES


