A Novel Soft-Switching Secondary-Side Modulated Multioutput DC–DC Converter With Extended ZVS Range

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***Abstract*—In this paper, a novel soft-switching secondary-side modulated dc–dc structure with extended zero voltage switching (ZVS) range is proposed. In a simple manner, this structure can be extended to provide isolated multioutputs with independent voltage regulation capability. Besides, the secondary side can be bidirectional to interface with energy storage elements such as batteries and ultracapacitors. The proposed topology is suitable for high voltage gain or high output dc-link voltage, low-power, and multioutput applications. The primary-side full-bridge switches operate complementarily to generate a two-level square wave. Therefore, the circulating energy is significantly smaller than conventional phase-modulated full-bridge converters. The output voltage is regulated by controlling the duty cycle of the auxiliary MOSFET on the active/semiactive rectifier, which offers a simple control. Moreover, the ZVS operation range of full-bridge MOSFETs is enhanced due to the volt-second balance of magnetizing inductance and the secondary-side control. All the secondary-side rectifying diodes turn OFF with limited *di/dt*. A 1-kW prototype generating two 390 V, 330–400 V outputs from a 130–180 V dc link is designed to serve as a proof of concept. The full-load efficiency is 95.6% at 100 kHz switching frequency.**

***Index Terms*—Multioutput, pulsewidth modulation (PWM), secondary-side control, zero voltage switching (ZVS).**

I. Introduction

WIDE voltage regulation range, galvanic isolation, and small volume size are important features of power converters that are demanded in many applications, such as the ones interfacing renewable energy sources and those adopting dynamic loads, energy storage units, etc. [1]. In general, power electronic converters can be divided into two main categories according to circuit/control schemes: pulsewidth modulation (PWM) controlled converters and frequency-controlled resonant converters. Compared with resonant converters, PWM converters demonstrate advantages including structure/design simplicity and ease of control. Among various types of PWM converters, the phase-shifted full-bridge (PSFB) converter is preferred in medium/high power and high voltage applications due to its simplicity, wide output voltage regulation, galvanic isolation, and soft-switching features. However, the conventional PSFB converter has the following well-known issues: narrow zero voltage switching (ZVS) range for the lagging-leg switches, large circulating currents, duty-cycle loss, and excessive voltage ringing of the rectifying diodes [2], [3].

Many techniques have been proposed to improve the circuit performance of PSFB converters. In [4] and [5], switched-capacitor or capacitor-diode-diode clamping circuits are used to eliminate the secondary-side parasitic ringing. In [6] and [7], capacitive output filters without an output inductor are employed. Since they do not have an output inductor, the secondary-side ringing and duty-cycle loss problems are solved naturally. Also, some techniques are proposed to improve ZVS performance of the lagging-leg switches in PSFB converters. The converter presented in [8] use a saturable inductor for ZVS range extension. However, even with a saturable inductor, it is still difficult to achieve ZVS at very light load. To ensure a wider ZVS range for MOSFETs, auxiliary energy storage elements are necessary. In [9] and [10], the soft-switching energy comes from the inductors in auxiliary legs. In [11]–[13], the soft-switching energy is provided by the externally added transformer. In [14]–[16], the LLC tank integrated to the PSFB converter provides the energy required for ZVS. In summary, all of the topologies presented in [9]–[15] require extra components to supplement energy for ZVS range extension, particularly at light load.

A more efficient and simpler way to extend ZVS range is to utilize the energy stored in magnetizing inductance by gapping the transformer. However, the magnetizing current in the PSFB converter is dependent on the phase-shift angle. To ensure the ZVS condition with large phase shift, magnetizing inductance should be small, which causes higher circulating current and more conduction losses. Besides, the magnetizing energy can be used for ZVS operation only when the secondary-side current decreases to zero and L_m participates in the resonance with MOSFET output capacitances and leakage inductance during the deadtime. These ZVS limitations with reduced L_m in conventional PSFB converters have been described in [17] and [18] and accordingly, secondary-side control is proposed. With

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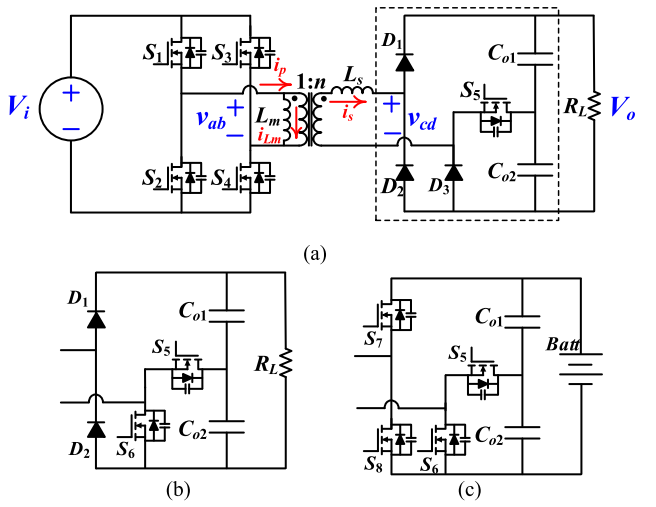

Fig. 1. Proposed full-bridge dc–dc converter. (a) With semiactive rectifier. (b) Active rectifier. (c) Bidirectional rectifier.

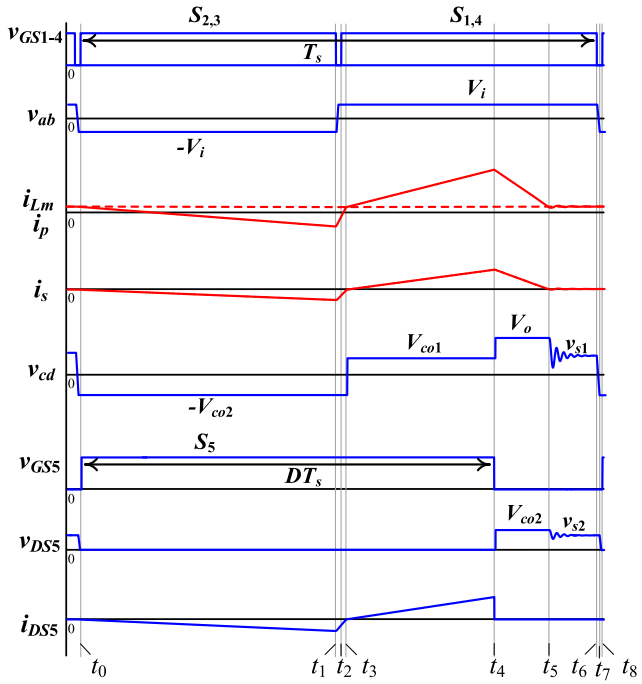

Fig. 2. Key steady-state waveforms.

secondary-side control, primary-side switches can work with fixed zero or small phase shift. The advantages include: 1) magnetizing current is independent of voltage regulation; and 2) secondary-side switches let the secondary side open-circuited during the switching transitions. Consequently, they can achieve ZVS down to no load with little conduction loss penalty.

In this paper, a novel soft switching dc–dc converter also with secondary-side control is proposed. The primary full-bridge switches operate in a complementary manner without phase shift. Hence, the circuiting current is significantly reduced. The output voltage regulation is achieved by controlling the duty cycle of the secondary-side auxiliary MOSFET in the voltage doubler rectifier. It inherits the benefits of capacitive filters shown in [5] and [6] with clamped diode voltage stresses. The proposed topology operates in discontinuous current mode; hence, it is a good solution for high voltage gain or high output voltage, low-power applications. Besides, like [17] and [18], it demonstrates enhanced ZVS performance due to secondary-side control. The volt-second balance of L_m helps to suppress imbalance of primary switches and further enhance ZVS range. Turn-OFF *di/dt* of all the secondary-side rectifying diodes is limited by the leakage inductance. With the secondary-side voltage regulation feature, this converter can be extended to provide multiple outputs with the shared primary switching network and transformer core. Besides, the secondary side can be bidirectional; hence, the proposed structure can be used in a variety of bidirectional applications. One such application is the PV power converter interface, where a multiport converter is required between the PV panel, dc link, and energy storage element [19], [20].

II. Description of the Proposed Converter

Fig. 1 shows the circuit configuration of the proposed full-bridge dc–dc converter with secondary-side control (FB-SC). Primary-side switches S_{1-4} operate complementarily without phase shift. Inductor L_s represents the leakage inductance equivalent to the transformer secondary side. Secondary-side diodes and capacitors D_1, D_2, C_{o1}, and C_{o2} construct the conventional voltage doubler rectifier. As shown in Fig. 1(a), D_3–S_5 is the proposed auxiliary bridge, and the duty cycle of S_5 is controlled to regulate the output voltage. The operation of D_3 and S_5 are in complementary. Hence, D_3 can be replaced by S_6, as shown in Fig. 1(b), to convert the semiactive rectifier to active rectifier. The driving signals of S_5 and S_6 are easy to realize by a half-bridge driver with no need for extra current sensors to adjust soft-turn-ON. With some deadtime, S_5 or S_6 are turned ON while the current passes through their body diodes; therefore, they can both be turned ON under ZVS.

As shown in Fig. 1(c), to interface with energy storage elements, $D_{1,2}$ are replaced with $S_{7,8}$. When power flows into the battery, $S_{7,8}$ work as synchronous diodes. Conversely, S_5 is controlled to be always ON and S_6 is always OFF. The square-wave output is generated by C_{o1}, C_{o2}, and $S_{7,8}$ to draw energy from the battery. In the mode analysis and experiments, the semiactive rectifier is adopted.

The transformer core has no airgap in experiments, and practically, L_m is a very large value, while not infinite. The volt-second balance of large L_m introduces a self-balance mechanism. One feature of the self-balance phenomenon is a small dc current offset passing through L_m (i_{Lm}). i_{Lm} causes a negligible difference in conduction losses of S_{1-4}; while it is helpful to avoid the transformer saturation due to the mismatch of S_{1-4} and their drivers. Moreover, i_{Lm} plays an important role to enhance ZVS range for S_{1-4}. i_{Lm} is shown in the following mode analysis and key steady waveforms. The detailed explanation of the self-balance mechanism is provided in Section III.

A. Operation Principles

1) i_s in Discontinuous-Conduction Mode (DCM): In most cases, secondary-side current i_s in the FB-SC converter

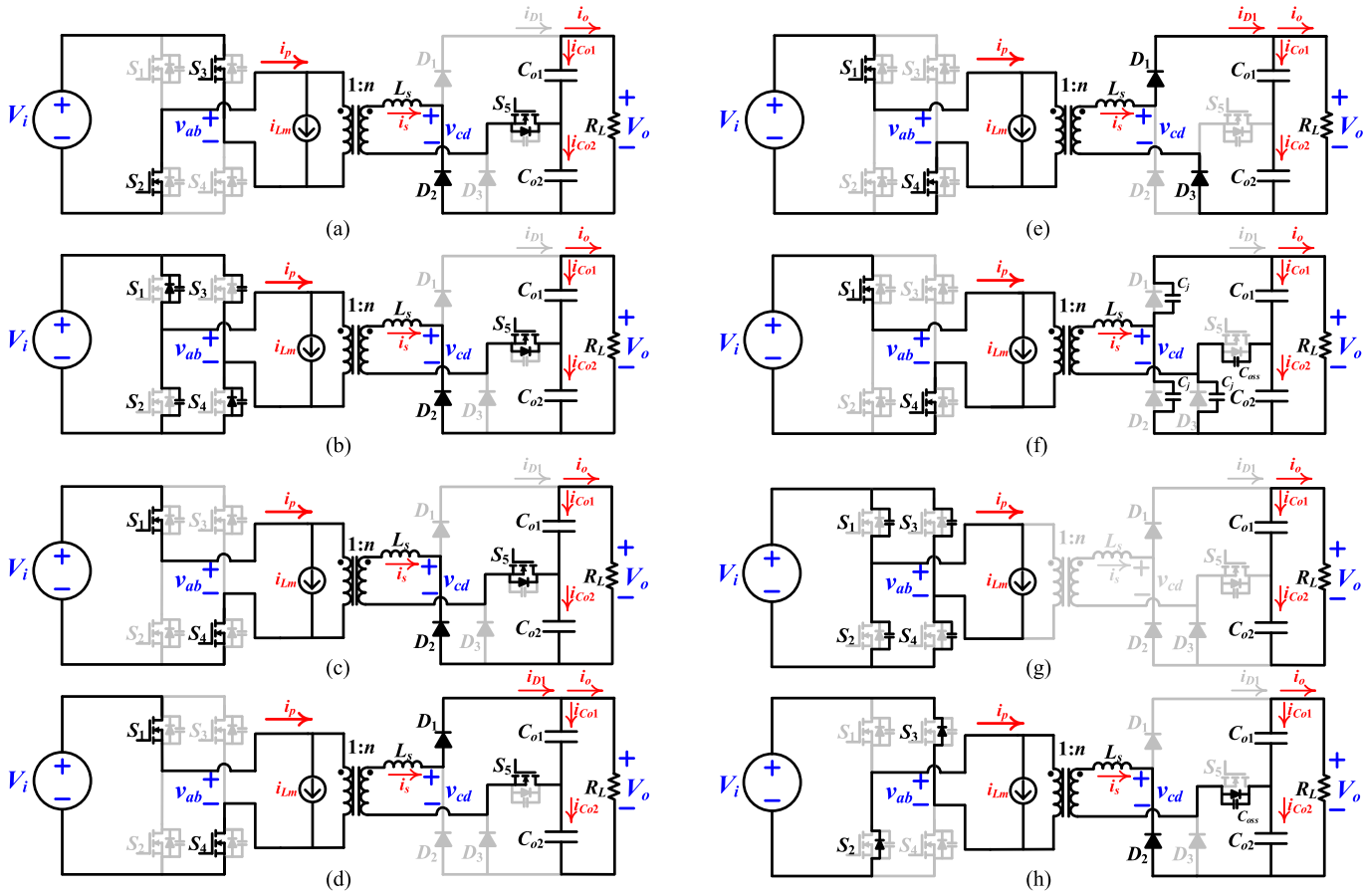

Fig. 3. Equivalent circuits with respect to modes of operation. (a) Mode I. (b) Mode II. (c) Mode III. (d) Mode IV. (e) Mode V. (f) Mode VI. (g) Mode VII. (h) Mode VIII.

operates in DCM. The key steady-state waveforms in DCM are shown in Fig. 2. Each switching period can be divided into eight operation modes. Primary-side switches S_{1-4} operate complementarily with certain deadtime, while S_5 is modulated with a variable duty cycle (D). The equivalent circuits are plotted in Fig. 3. Secondary-side capacitors C_{o1} and C_{o2} are large and construct the capacitor filter; hence, the voltages across them can be assumed constant, which are denoted as V_{Co1} and V_{Co2}. As mentioned above, the small dc offset current passing through L_m is marked as i_{Lm}.

Mode I $(t_0, t_1]$*:* At t_0, switches $S_{2,3,5}$ are turned ON. Secondary-side current i_s is negative and its absolute value increases. On the secondary side, D_2 and S_5 conduct; hence, the change in i_s is expressed as

$$\frac{di_s(t)}{dt} = \frac{1}{L_s}\left(-nV_i + V_{C_{o2}}\right). \tag{1}$$

Mode II $(t_1, t_2]$*:* It is the deadtime of S_{1-4}. First, the negative i_p discharges and charges the output capacitors (C_{oss}) of $S_{1,4}$ and $S_{2,3}$, respectively. Then, the body diodes of $S_{1,4}$ conduct and v_{ab} is equal to V_i.

Mode III $(t_2, t_3]$*:* At t_2, $S_{1,4}$ are turned ON under ZVS. The absolute value of i_s decreases linearly and its slope can be expressed as

$$\frac{di_s(t)}{dt} = \frac{1}{L_s}\left(nV_i + V_{C_{o2}}\right). \tag{2}$$

At the end of Mode III, i_s becomes zero.

Mode IV $(t_3, t_4]$*:* Secondary-side current i_s increases from zero and becomes positive. On the secondary side, D_1 and S_5 conduct; hence, the change in i_s can be expressed as

$$\frac{di_s(t)}{dt} = \frac{1}{L_s}\left(nV_i - V_{C_{o1}}\right). \tag{3}$$

Mode V $(t_4, t_5]$*:* At t_4, S_5 is turned OFF. Secondary-side current i_s goes through D_3 instead of S_5. Accordingly, the change in i_s is expressed as

$$\frac{di_s(t)}{dt} = \frac{1}{L_s}\left(nV_i - V_{C_{o1}} - V_{C_{o2}}\right). \tag{4}$$

At t_5, i_s reaches zero.

Mode VI $(t_5, t_6]$*:* At t_5, i_s decreases to zero and the circuit enters into DCM operation. As shown in Fig. 3, D_{1-3} and S_5 are all reverse biased and can be viewed as capacitors (C_j, C_{oss}). There is a DCM resonance between these capacitors and circuit inductors. The resonant voltages and currents (v_{cd}, v_{DS5}, i_p, and i_s) are shown in Fig. 2 and also shown in the experimental results. After the resonance, i_s stays zero, and the transformer secondary side remains open-circuited. Secondary-side voltage

v_{cd} and v_{DS5} become two dc voltages, which are decided by the ratio of (C_j, C_{oss}). It should be noted, with the increase of *D*, this time interval decreases, and even disappears.

Mode VII $(t_6, t_7]$*:* After switches $S_{1,4}$ are turned OFF, the deadtime interval for S_{1-5} starts. Primary-side current i_p charges and discharges C_{oss} of $S_{1,4}$ and $S_{2,3}$, respectively. Secondary-side voltage v_{cd} decreases with v_{ab}, which causes i_s to discharge C_j of D_2 and C_{oss} of S_5. Because i_s is close to zero and much smaller than i_p, the secondary side can still be regarded as open-circuited and v_{ab} can be expressed as

$$v_{ab}(t) = V_i - \frac{i_{L_m}}{C_{\text{oss}}}(t - t_6). \tag{5}$$

Mode VIII $(t_7, t_8]$*:* When v_{DS} of $S_{2,3}$ decreases to zero, v_{ab} decreases from V_i to $-V_i$ synchronously. Then, the body diodes of $S_{2,3}$ conduct and a negative voltage is applied to L_s. Hence, the absolute value of i_s increases and discharges C_{oss} of S_5. Finally, v_{DS5} of S_5 becomes zero and its body diode starts to conduct. The next switching period starts with the zero voltage turning-ON of $S_{2,3,5}$.

2) i_s in Boundary/Continuous-Conduction Mode (BCM/CCM): When *D* increases and approaches 1, the time interval of mode VI decreases and i_s enters into BCM or CCM. In BCM, at the end of Mode V, $i_s = 0$, while in CCM, $i_s > 0$. The extreme case is when $D = 1$, the semiactive rectifier operates as a voltage doubler rectifier and the output voltage reaches the peak value. Note that in CCM, S_5 is turned ON with positive current, losing its soft-switching feature. Hence, to ensure the ZVS performance of S_5, DCM or BCM operations are more preferred for this converter.

B. Voltage Conversion Ratio

The voltage regulation of the proposed FB-SC converter is achieved by PWM control of S_5. In this section, the relationship between *D* of S_5, equivalent load resistance (R_L), and the normalized voltage conversion ratio $(G = V_o/nV_i)$ is derived. Circuit parameters (*n*, L_s, V_i, and T_s) are regarded as known variables. The switching deadtime is much shorter than T_s; hence, modes II, VII, and VIII are ignored here. Besides, in Mode VI, i_s is equal to zero. Fig. 4 shows the simplified equivalent circuits of the rest modes (I, III, IV, and V). In Mode I, the absolute value of negative i_s increases from zero and at the end i_s reaches the negative peak value; in Mode III, the absolute value of i_s decreases to be zero; in Mode IV, i_s increases to reach the positive peak value; and in Mode V, i_s returns to zero. The corresponding changing rate i_s are expressed in (1)–(4). Assuming that the time interval of modes III and V are t_{III} and t_{V}, respectively, the volt-seconds of L_s in modes I, III and modes IV, V should both be zero at steady state

$$\frac{T_s}{2}\left(-nV_i + V_{C_{o2}}\right) + t_{\text{III}}\left(nV_i + V_{C_{o2}}\right) = 0 \tag{6}$$

$$\left[(D - 0.5)T_s - t_{\text{III}}\right]\left(nV_i - V_{C_{o1}}\right) + t_V\left(nV_i - V_{C_{o1}} - V_{C_{o2}}\right) = 0. \tag{7}$$

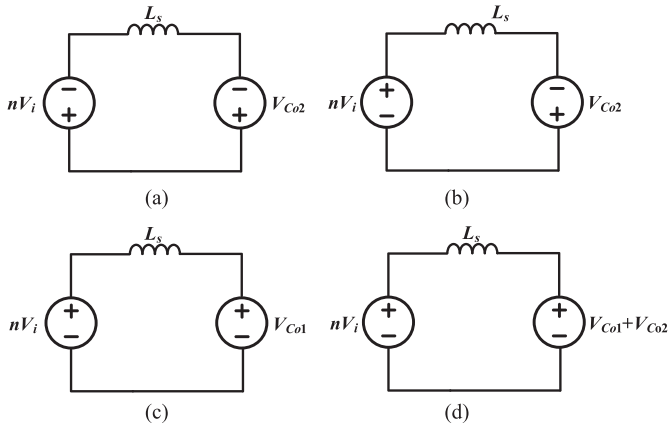

Fig. 4. Simplified equivalent circuits of several operation modes. (a) Mode I. (b) Mode III. (c) Mode IV. (d) Mode V.

Based on the charge balance of C_{o1} and C_{o2}, the net charge delivered to C_{o1} and C_{o2} over one switching period should be equal to zero. Besides, in modes V and VI, the currents passing through C_{o1} and C_{o2} are equal. Hence, the total charge delivered to C_{o1}, C_{o2} over modes I, III, and IV should also be equal, which can be expressed with i_s and output current (i_o). By eliminating duplicate items associated with i_o on both sides, the following can be derived:

$$\frac{1}{2}\left(\frac{T_s}{2} + t_{\text{III}}\right)\frac{T_s}{2}\left(\frac{nV_i - V_{C_{o2}}}{L_s}\right) = \frac{1}{2}\left[(D - 0.5)T_s - t_{\text{III}}\right]^2 \times \left(\frac{nV_i - V_{C_{o1}}}{L_s}\right). \tag{8}$$

As shown in Fig. 3, according to Kirchhoff's circuit laws (KCL), i_{D1} is the sum of the current flowing through C_{o1} (i_{Co1}) and i_o. The integral of i_{Co1} over one switching period is zero; hence, the integrals of i_{D1} and i_o over one switching period should be equal

$$\frac{\left(V_{C_{o2}} + V_{C_{o1}}\right)T_s}{R_L} = \frac{\left[(D-0.5)T_s - t_{\text{III}} + t_V\right]\left[(D-0.5)T_s - t_{\text{III}}\right]}{2}\left(\frac{nV_i - V_{C_{o1}}}{L_s}\right). \tag{9}$$

As mentioned above, it is preferred to operate the proposed converter in DCM/BCM. The boundary condition established based on the time interval of Mode VI is zero, when $t_V = (1 - D)T_s$. Combining (6)–(9), the boundary curve is defined by the following equation and represented by the black dotted line in Fig. 5

$$G = \frac{\sqrt{-16D^3 + 24D^2 - 8D + 1} + 4D - 4D^2 - 1}{4D(1 - D)}. \tag{10}$$

In DCM, according to (6)–(9), the four unknown quantities (t_{III}, t_{V}, V_{co1}, and V_{co2}) can be solved. However, these equations are transcendental, and only numerical solutions can be obtained with mathematical tools. Here, an approximation has been made to reduce the complexity. It is observed that when *D* changes, the variation of V_{co2} is quite small and V_{co2} is close to nV_i. By linear fitting, the expression of V_{co2} can be de-

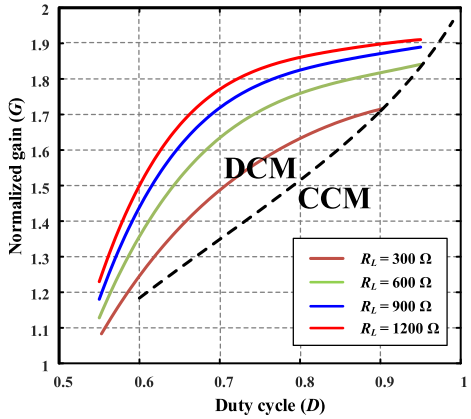

Fig. 5. Normalized voltage gain (G) versus D with different R_L.

rived. Two intermediate variables (k and m) are used to simplify the equations

$$k = \frac{256L_s^2}{R_L^2 T_s^2} \tag{11}$$

$$m = (D - 0.5)\left(1 - \sqrt{1 + k} + \sqrt{k}\right). \tag{12}$$

Accordingly, output voltages and normalized gain V_{co1}, V_{co2}, and G can be expressed as

$$V_{C_{o2}} = nV_i\,(1 - 2m) \tag{13}$$

$$V_{C_{o1}} = nV_i\left[1 + \frac{2m^2 - 2m}{(1 - 2D + 2Dm)^2}\right] \tag{14}$$

$$G = \frac{V_o}{nV_i} = 2 + \frac{2m^2 - 2m}{(1 - 2D + 2Dm)^2} - 2m. \tag{15}$$

In order to more clearly describe the voltage regulation capability of the FB-SC converter, G versus D and R_L in the simulation are plotted in Fig. 5. The duty cycle of S_5 should be larger than 0.5 because it loses regulating ability when D is smaller than 0.5. Fig. 5 illustrates the voltage gain of the designed prototype, which always operates in DCM/BCM.

III. Features and Characteristics

A. Enhanced ZVS Performance for MOSFETs

As shown in Fig. 1, the secondary side of the proposed structure can be semiactive, active rectifier or bidirectional rectifier. In DCM/BCM, S_{5-8} are turned ON under ZVS with adequate deadtime, while the current passes through their body diodes. In CCM, S_5 loses ZVS performance.

To analyze the ZVS conditions for S_{1-4}, the volt-second balance of large but not infinite L_m should be considered first.

1) Volt-Second Balance of L_m: The volt-second balance of L_m brings two important benefits in the proposed FB-SC converter. The first benefit is the suppression of nonidealities of S_{1-4} and their drivers. Usually, there may be small mismatches of MOSFET on-resistances or conduction times. This voltage mismatch across L_m accumulates and may lead to transformer saturation. However, the volt-second balance of L_m can suppress these mismatches.

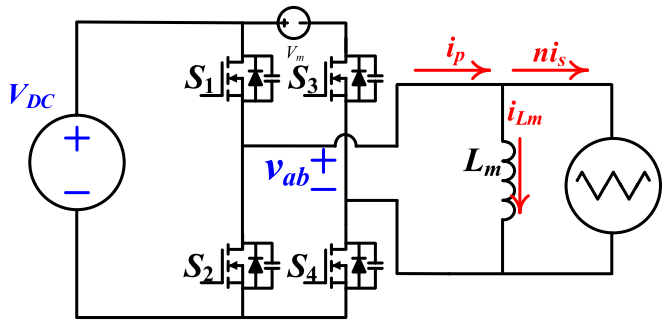

Fig. 6. Equivalent circuits with the primary-side mismatch (V_m).

The core of the suppression mechanism is that a negative feedback is established in case of nonidealities. Take Fig. 6 as an example, where the drivers are ideal and the voltage drop across $S_{1,2,4}$ is zero. The only mismatch is the extra voltage drop across S_3 denoted as V_m. Besides, the output capacitors (C_{oss}) of S_{1-4} are identical. The secondary side of the converter is simply represented by a symmetrical triangular-wave current source, ni_s.

Fig. 7 shows the driving signals of S_{1-4}, v_{ab}, and i_p. Primary-side switches S_{1-4} operate in complementary with certain deadtime (t_{dead}). The ON time of $S_{1,4}$ and $S_{2,3}$ ($t_{1,4}$ and $t_{2,3}$) is equal. Assuming S_{1-4} can all achieve ZVS and t_{dead} is set to larger than t_{down}, t_{up}, when C_{oss} of $S_{2,3}$ or $S_{1,4}$ are discharged to zero. In Fig. 7(a), $V_m = 0$, t_{down}, t_{up} corresponds to when v_{ab} changes from V_{DC} to $-V_{\text{DC}}$ and reversely from $-V_{\text{DC}}$ to V_{DC}. In Fig. 7(b), $V_m > 0$, t_{down}, t_{up} corresponds to when v_{ab} changes from V_{DC} to $-(V_{\text{DC}} - V_m)$ and reversely from $-(V_{\text{DC}} - V_m)$ to V_{DC}.

Magnetizing inductance L_m is very large. In Fig. 7(a), v_{ab} across L_m causes negligible symmetrical ac current passing through L_m. Primary-side current i_p can be seen as equal to ni_s. Hence, $I_{\text{down}} = I_{\text{up}}$, which are respectively the currents discharging C_{oss} of $S_{2,3}$ and $S_{1,4}$ to be zero. Accordingly, $t_{\text{down}} = t_{\text{up}}$, the volt-second of L_m over one switching period can be expressed as

$$\int_0^{T_s} v_{ab}\,(t)dt = [t_{1,4} + (t_{\text{dead}} - t_{\text{up}})]\,V_{\text{DC}} - [t_{2,3} + (t_{\text{dead}} - t_{\text{down}})]\,V_{\text{DC}} = 0. \tag{16}$$

In Fig. 7(b), $V_m > 0$, the negative feedback compensates this mismatch as follows. First, $V_m > 0$ causes the volt-second of L_m to be larger than zero. Then, a positive dc current offset (i_{Lm}) is induced by L_m for the positive volt-second of L_m. Therefore, the currents discharging C_{oss} of $S_{2,3}$ and $S_{1,4}$ become $I_{\text{down}} + i_{Lm}$ and $I_{\text{up}} - i_{Lm}$. This, in turn, causes $t_{\text{down}} < t_{\text{up}}$ and the integral of v_{ab} decreases. Finally, volt-second of L_m returns to zero which is the state of equilibrium, and primary-side mismatches are compensated.

2) Enhanced ZVS Performance With L_m Volt-Second Balance: In most cases of the proposed converter except $D = 1$, i_s is asymmetrical. Usually, i_s operates in DCM, which is shown

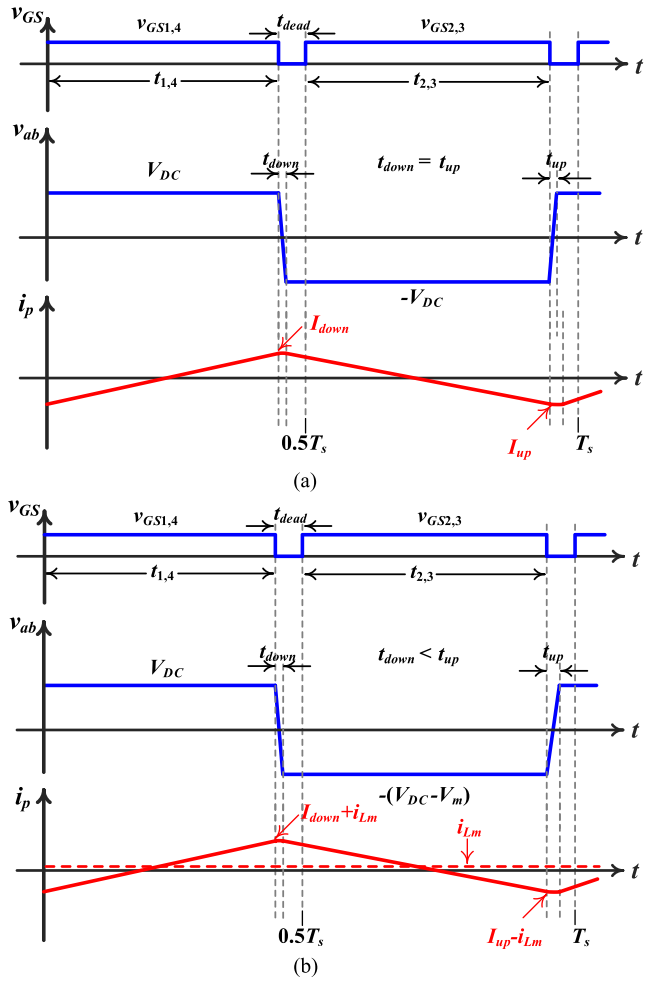

Fig. 7. Waveforms of v_{GS}, v_{ab}, and i_p over one switching cycle. (a) $V_m = 0$. (b) $V_m > 0$.

in Fig. 2. In the transient process, i_s reflected to the primary side causes the left-hand side of (16) to be larger than zero. Then, a small positive current offset is introduced through L_m to balance the previous I_{down} and I_{up}. This dc offset current can be seen in Fig. 2. Finally, equilibrium condition that the integral of $v_{ab}(t)$ over one switching period is zero has been established. Hence, the turning-ON currents for S_{1-4} are all large enough to achieve ZVS.

This self-balance always works no matter how large L_m is. Hence, to reduce the circulating currents, in the proposed converter, the transformer core has no airgap and L_m is set as large as possible. Also, it should be noted, this small positive current offset causes a negligible difference in losses for S_{1-4}, because the conduction losses increase for $S_{1,4}$, while decrease for $S_{2,3}$.

Note that, for the converters with phase shift control, the negative feedback cannot be established. In such condition, the operations of the same leg switches are identical. A singular direction offset of i_{Lm} is not enough to achieve ZVS for all switches. For example, if $S_{3,4}$ are the lagging-leg switches in the PSFB converter at light load conditions, to achieve ZVS, the offset current of i_{Lm} should be positive and negative for S_3 and S_4, respectively. Hence, to ensure all switches' ZVS, one possible strategy is to decrease L_m to make i_{Lm} to have bidirectional current flow. However, this leads to increased conduction losses because the circulating currents flowing through S_{1-4} all increase.

3) Utilizing the Magnetizing Energy by the Secondary Control: The energy stored in the magnetizing inductance becomes available for the primary-bridge switches to achieve ZVS only when the secondary side is open-circuited. Under normal condition, when converters operate with primary phase-shift control, the secondary side is open-circuited only at very light load conditions. However, as demonstrated in [17] and [18], one advantage of these secondary-side controls is that the energy stored in L_m can be directly used to discharge the C_{oss} of MOSFETs. The proposed topology also contains this inherent advantage.

In the proposed converter, i_s in the FB-SC converter is designed to operate in DCM. For $S_{1,4}$, only the energy stored in L_s can be used. Hence, (17) has to be satisfied for ZVS condition

$$\frac{1}{2n^2}L_s|i_p(t_1)|^2 \geq \frac{1}{2}\left(\frac{8}{3}C_{\text{oss}}\right)V_i^2. \tag{17}$$

While for $S_{2,3}$, Mode VI exists. Hence, the energy stored in L_m can be used. Therefore, the following inequality should be satisfied to achieve ZVS:

$$\frac{1}{2}L_m i_{L_m}^2 \geq \frac{1}{2}\left(\frac{8}{3}C_{\text{oss}}\right)V_i^2. \tag{18}$$

4) Extended ZVS Range: In the mode analysis, L_m is assumed as sufficiently large but finite. Hence, there is negligible ac current swing passing through L_m for the volt-second of v_{ab}, and i_{Lm} only contains a positive dc current induced by the volt-second balance of L_m. This is not the actual fact because the maximum L_m is limited by the coil number and the magnetizing core; hence, practically i_{Lm} contains an ac part. First, assuming in ideal condition, where i_{Lm} has only a dc value, the relation between i_{Lm} and $|i_p(t_1)|$ can be expressed as

$$|i_p(t_1)| = \frac{(-nV_i + V_{C_{o2}})nT_s}{2L_s} - i_{L_m}. \tag{19}$$

It should be noted that L_m is much larger than L_s. Hence, $|i_p(t_1)|$ decreases faster than i_{Lm} when discharging C_{oss} during the deadtime. In other words, according to the volt-second balance equilibrium condition, $|i_p(t_1)|$ should be larger than i_{Lm}. However, to simplify the analysis, the following assumption is made:

$$I_{L_m} = |i_p(t_1)| = \frac{(-nV_i + V_{C_{o2}})nT_s}{4L_s}. \tag{20}$$

Since L_m is a very large value, (17) is easy to satisfy. The required L_s is constrained by

$$L_s \leq \frac{3n^2m^2T_s}{32C_{\text{oss}}}. \tag{21}$$

To limit the root-mean-square (rms) value of i_p and i_s, secondary-side inductance, L_s cannot be too small. Furthermore, m decreases with the increase of R_L. Hence, $S_{1,4}$, can lose ZVS at light load conditions.

In practical conditions like the prototype built for verification, secondary-side equivalent L_m is around 1 mH. Therefore,

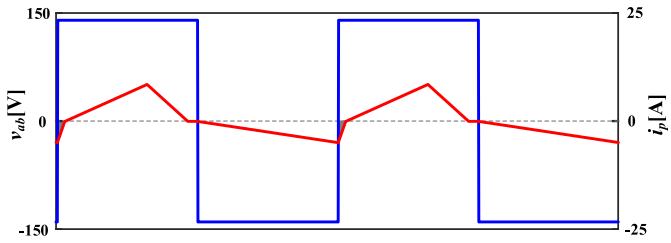

Fig. 8. Waveforms of v_{ab} and i_p in the FB-SC converter with $V_i = 140$ V and $P_o = 500$ W.

i_{Lm} consists of a dc offset and an ac current part. The ac part provides extra energy for ZVS of $S_{1,4}$. Consequently, proposed topology offers almost full-range ZVS with a minimum amount of circulating energy.

B. Small Circulating Current Without Phase Shift

Another advantage of the FB-SC converter is that there is no primary freewheeling interval. Hence, the circulating current is very small. Fig. 8 depicts v_{ab} and i_p of the proposed converter with $V_i = 140$ V and $P_o = 500$ W. The dc offset i_{Lm} will be considered later. In Fig. 8, the shaded zones represent the negligible circulating currents.

When taking i_{Lm} into considerations, this small positive current offset causes a negligible difference in circulating current passing through S_{1-4}, because the circulating current increases for $S_{1,4,}$, while they decrease for $S_{2,3}$.

C. Design Considerations

Since the proposed topology operates in DCM, the circuit parameters should be well chosen for a given power level. The design considerations are given as follows.

1) Power and Voltage Rating: In the proposed topology, the active/semiactive rectifier is derived from the voltage doubler structure. This structure brings two advantages: 1) output voltage is multiplied and 2) the reverse voltages of the secondary-side switches are clamped by the capacitor filter. Hence, there is no secondary-side ringing problem which always happens with an *L–C* output filter. The tradeoff is that without the large filter inductor, the currents in converters with capacitive filters like in [6] and [7] change more steeply than those with *LC* filter in [1]. In other words, to transfer the same power, RMS and peak values of currents with capacitive filters are usually higher than those with *LC* filters. Hence, the capacitive filters are preferred to work in medium or low power applications. The proposed topology adopts capacitive filter and i_s is designed to operate in DCM. Considering the pros and cons of the capacitive filter and the DCM operation, this topology is suitable for high voltage gain or high output dc-link voltage low-power applications.

2) G_{max}, L_s and Turns Ratio: The input voltage range $(V_{i\min} - V_{i\max})$, the output voltage (V_o), and the lowest equivalent load resistance $(R_{L\min})$ are defined by the application needs. The switching frequency (f_s) is chosen based on the power density and efficiency requirement. Essentially, the gain curve at maximum load should be above the boundary curve for DCM operation as shown in Fig. 5. Hence, the intersection point of the gain curve with $R_{L\min}$ and the boundary curve defines the maximum normalized voltage gain $(G_{\max})$. In the boundary curve, G only depends on D. Accordingly, with defined $G_{\max}$ and known $R_{L\min}$ and f_s, the required L_s can be derived. Based on (11), with fixed R_L, a higher $G_{\max}$ corresponds to reduced L_s. The selections of $G_{\max}$ or L_s should take these two factors into consideration: 1) decreasing $G_{\max}$ brings higher L_s, which means higher inductive reactance, smoother currents, and lower conduction losses and 2) $D_{\max}$ defined by $G_{\max}$ should be close to 1 to alleviate circuit asymmetry. In the prototype, $G_{\max}$ and $D_{\max}$ are selected to be 1.71 and 0.9, respectively. With the designed $G_{\max}$ and the input, output voltage range, the turns ratio of the transformer can be defined accordingly.

3) L_m and t_{dead}: The discussion of ZVS and L_m has been provided in Section III-A. The induced dc offset i_{Lm} is useful for ZVS achievement. However, at very light conditions, $i_p(t_1)$ and i_{Lm} are both very small. Therefore, the energy stored in L_s and L_m may not be sufficient to fully discharge C_{oss} of $S_{2,3}$. Hence, they may be turned ON under partial ZVS. If the design goal is to achieve a full range ZVS performance, L_m should be smaller than an upper boundary (L_{mx}) for enough extra ac magnetizing currents.

With L_m in the upper boundary, the current ripple of i_{Lm} can be expressed as

$$\Delta i_{L_m} = \frac{V_i}{2L_{\text{mx}}} T_s. \tag{22}$$

At very light load, the induced dc offset i_{Lm} is small, which is assumed as zero to simplify the analysis. With this assumption, the turn-ON currents for S_{1-4} are equal to half of Δi_{Lm}. According to the mode analysis, in Mode II, before turning ON $S_{1,4}$, C_{oss} of S_{1-4} resonate with L_s, and v_{ab} can be expressed as

$$v_{ab}(t) = -\frac{V_{C_{o2}}}{n} + A\sin(\omega_s t + \alpha) \tag{23}$$

$$\omega_s = \frac{n}{\sqrt{L_s C_{\text{oss}}}} \tag{24}$$

$$A = \sqrt{\left(-V_i + \frac{V_{C_{o2}}}{n}\right)^2 + \left(\frac{\Delta i_{L_m}}{2\omega_s C_{\text{oss}}}\right)^2} \tag{25}$$

$$\alpha = \arcsin\left(\frac{-nV_i + V_{C_{o2}}}{nA}\right). \tag{26}$$

In Mode VII, when is deadtime for $S_{2,3}$ to achieve ZVS, the transformer secondary side is open-circuited. Hence, v_{ab} can be derived as follows:

$$v_{\text{ab}}(t) = V_i - \frac{\Delta i_{L_m} t}{2C_{\text{oss}}}. \tag{27}$$

To ensure the ZVS turning ON of S_{1-4}, the energy stored in L_s and L_m should be large enough and the time interval for C_{oss} of S_{1-4} to be discharged to be zero should be smaller than t_{dead}.

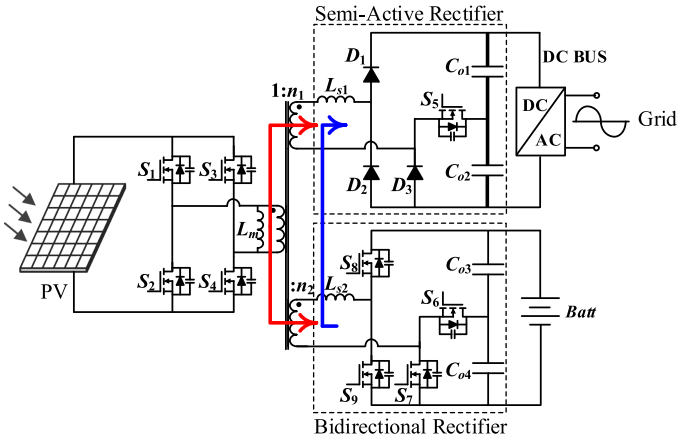

Fig. 9. Structure extension for a PV-based generator application.

Accordingly

$$A - \frac{V_{Co2}}{n} > V_i \tag{28}$$

$$t_{\text{dead}} > \frac{\arcsin\left(\frac{nV_i + V_{Co2}}{nA}\right) - \alpha}{\omega_s} \tag{29}$$

$$t_{\text{dead}} > \frac{4V_i C_{\text{oss}}}{\Delta i_{L_m}}. \tag{30}$$

Combing (13), (22), and (24)–(30), the upper boundary of L_m and the required t_{dead} can be derived with the assistance of the mathematical tools.

D. Extension for Multiple Outputs in PV-Based Microgrid Applications

The primary side of the FB-SC converter can be seen as a square-wave generator. In the proposed converter, considering the input voltage range, it is chosen as a full-bridge switching network. However, it can also be a half-bridge network. The proposed structure can be extended to achieve multiple outputs with independent voltage regulation capability. For unidirectional power flow, the semiactive or active rectifiers are used. For bidirectional power flow, rectifying diodes are replaced with switches so that the power can be drawn from energy stored elements like batteries or supercapacitors.

Fig. 9 shows a structure extension example for grid-connected PV application. It serves as the interface between a PV panel, dc bus, and battery. The dc bus, which can also supply power to other loads, is connected to the grid through an inverter. When power flows from PV panel to dc bus and battery simultaneously, the primary switching network and the transformer core are shared and voltages across different secondary-side windings are both square waveforms. The charging strategy of the battery can be achieved by PWM control of S_6, while maximum power point tracking algorithm of the PV panel and energy balance functions are implemented by the PWM control of S_5.

When the battery is discharged to dc bus, the bidirectional rectifier is controlled by turning ON S_6 and turning OFF S_7. Secondary-side switches and capacitors $S_{8,9}$, C_{o3}, and C_{o4} generate square-wave input for the semiactive rectifier. Note that if turns ratio $(1 : n_1 : n_2)$ is designed on the condition that power flows from the PV panel to battery and dc bus, this ratio fits the voltage ratio when power flows from the battery to dc bus.

TABLE I
DESIGN PARAMETERS OF THE PROTOTYPE

Components	FB-SC
Switching frequency (f_s)	100 kHz
Leakage inductor (L_s)	20 μH
Turns ratio $(n_p : n_s)$	1:1.75
Filter capacitors (C_{o1}, C_{o2})	120 μF
Primary MOSFETs (S_{1-4})	C3M0120090D
Secondary diodes (D_{1-3})	C3D10060A
Secondary MOSFET (S_5)	IPA60R060C7

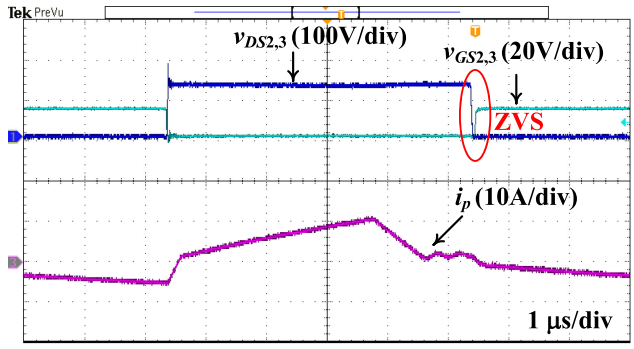

Fig. 10. Waveforms of $v_{DS2,3}$, $v_{GS2,3}$, i_p with $V_i = 130$ V, $V_o = 390$ V, $P_o = 500$ V.

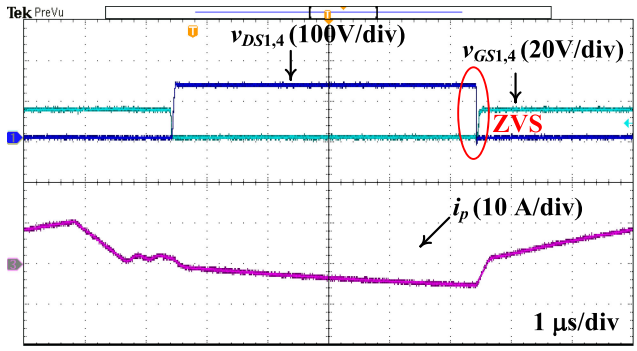

Fig. 11. Waveforms of $v_{DS1,4}$, $v_{GS1,4}$, i_p with $V_i = 130$ V, $V_o = 390$ V, $P_o = 500$ V.

IV. EXPERIMENTAL RESULTS

In order to verify the effectiveness of the converter, a prototype with two 500 W, 390 V, and 330–400 V outputs from 130–180 V dc link, is built. The components of the prototype are listed in Table I.

Figs. 10–12 show the experimental steady-state waveforms of v_{DS}, v_{GS}, i_p, and i_s. These waveforms coincide with the theoretical mode analysis. Observing i_p and i_s in Mode VI, it can be seen that i_p is shown as a small dc value plus resonance. The dc value represents the induced i_{Lm} and the resonance occurs for the DCM operation. Due to the volt-second balance

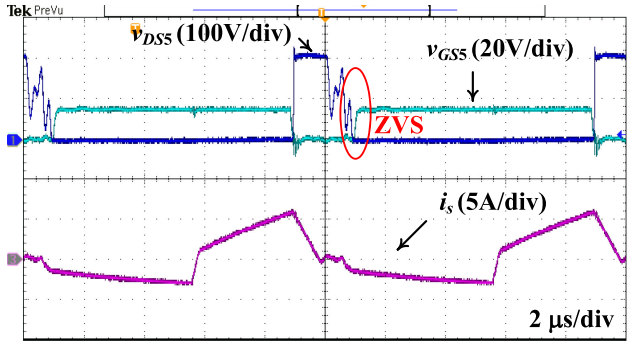

Fig. 12. Waveforms of v_{DS5}, v_{GS5}, i_s with $V_i = 130$ V, $V_o = 390$ V, $P_o = 500$ V.

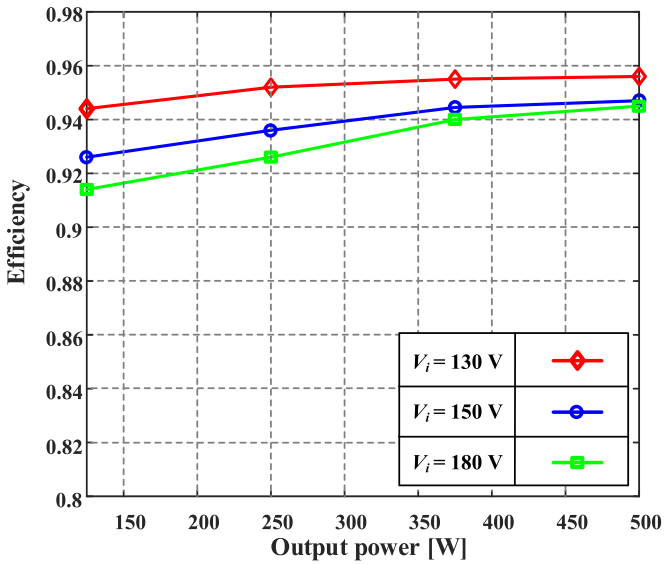

Fig. 13. Measured efficiency versus the output power with different input voltages.

of L_m, S_{1-4} all turn ON with zero voltage. Down to 25% load condition, ZVS for S_{1-4} still remains.

There is no steep change of i_s in Fig. 12 and the current passing through D_{1-3} are part of i_s. Hence, it can be concluded, the turn OFF *di/dt* of D_{1-3} is limited by L_s. Due to the voltage doubler structure, the secondary parasitic ringing problem is avoided. The voltage stresses of $D_{1,2}$ are determined by V_o, while those of D_3–S_5 are both clamped by V_{co2}.

In Fig. 12, the resonance of v_{DS5} can be observed in Mode VI. During this interval, D_3–S_5 are all turned OFF and their output capacitance and the parasitic capacitance of windings resonate with L_s. Then, the body diodes of $S_{2,3}$ conduct and i_s discharges C_{oss} of S_5. Therefore, S_5 is also turned ON with zero voltage as shown in Fig. 12.

The measured system efficiency graph with a single output is plotted in Fig. 13. As shown, the converter demonstrates good system efficiency and the peak value reaches 95.6% at full load condition. Lower input voltage corresponds to higher D, smoother i_s, lower conduction losses, and higher efficiency.

Fig. 14 illustrates the dynamic response of the prototype with a digital PID controller. The load resistance is constant and

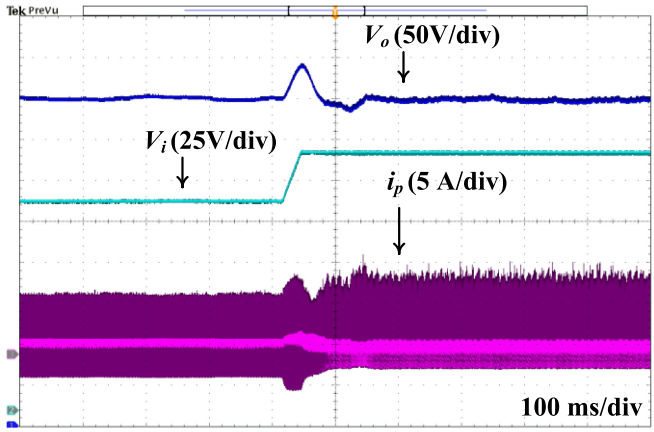

Fig. 14. Closed-loop dynamic response with $R_L = 600\ \Omega$, $V_o = 400$ V, and V_i changes from 130 to 160 V.

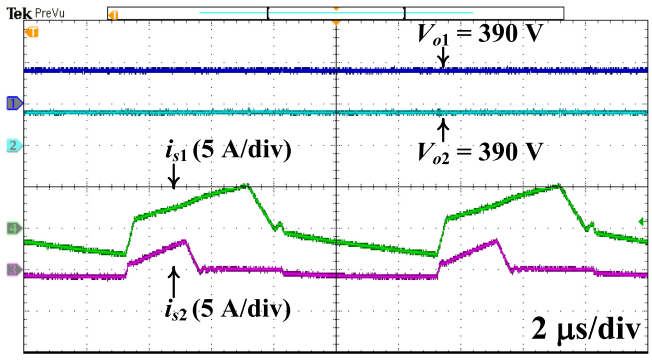

Fig. 15. Dual outputs ($V_{o1} = V_{o2} = 390$ V) with $R_{L1} = 300\,\Omega$ and $R_{L2} = 900\,\Omega$.

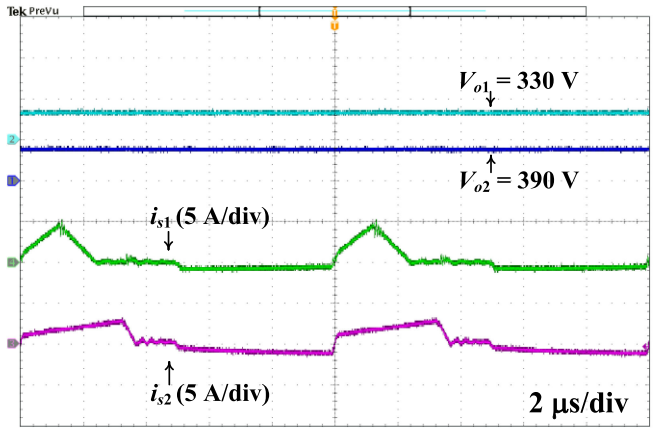

Fig. 16. Dual outputs ($V_{o1} = 330$ V, $V_{o2} = 390$ V) with $R_{L1} = R_{L2} = 600\,\Omega$.

the input changes from 130 to 160 V, as shown, the converter responds fast for the input perturbation with a stabilized 400 V output voltage.

The secondary-side control characteristic of the proposed structure makes it convenient to provide independently controlled outputs. In Fig. 15, the prototype has two outputs with

different load resistances ($R_{L1} = 300\ \Omega$, $R_{L2} = 900\,\Omega$, and $V_{o1} = V_{o2} = 390$ V). By controlling D of the respective two semiactive rectifiers, the outputs of them are both regulated to be 390 V. In Fig. 16, the prototype has two different outputs with same load resistance ($R_{L1} = 600\ \Omega$, $R_{L2} = 600\ \Omega$, $V_{o1} = 330$ V, and $V_{o2} = 390$ V).

V. Conclusion

In this paper, a novel soft switching dc–dc converter with secondary-side control is proposed. This topology is suitable for high voltage gain or high output dc-link voltage, low-power, and multioutput applications. The proposed topology adopts a voltage doubler rectifier with a duty-cycle-controlled diode-MOSFET bridge. The soft-switching extension relies on the volt-second balance of magnetizing inductance, which also helps to compensate the mismatches of primary-side switches and their drivers. Hence, large blocking capacitor is unnecessary.

Comparing with its primary-side counterpart, utilizing the secondary-side control brings a number of advantages: 1) extending the useful load range for ZVS operation by enabling the transformer magnetizing inductance to join the resonance between leakage inductance and MOSFET output capacitance; 2) small circulating current without phase shift; and 3) naturally suitable for multioutput applications.

To verify the circuit performance, a prototype with two 500 W, 390 V, and 330–400 V outputs from 130–180 V dc link is designed and tested. The prototype demonstrates an enhanced ZVS range down to 25% load conditions. At the designed power rating, the peak system efficiency reaches 95.6%. Furthermore, a closed-loop control is designed, which is easy to realize with fixed primary-side driving signals and PWM control of the auxiliary switch. Finally, from the dual output experiments, the proposed structure shows the great potential for multioutput applications.

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