Design Considerations for a Level-2 On-Board PEV Charger Based on Interleaved Boost PFC and LLC Resonant Converters

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***Abstract*—In this paper, a two-stage on board battery charger is proposed for plug-in electric vehicles (PEVs). An interleaved boost topology is employed in the first stage for power factor correction (PFC) and to reduce total harmonic distortion (THD). In the second stage, a half bridge LLC multi-resonant converter is adopted for galvanic isolation and dc-dc conversion. Design considerations are discussed focusing on the reducing the charger volume, and increasing conversion efficiency over the wide battery pack voltage ranges. Detailed design procedure is provided for a 7.6 kW prototype, charging the battery with an output voltage range of 320 V to 420 V from 240 V, 60 Hz single phase grid. Results of the analyses show that the first stage PFC converter achieves THD less than 4% and power factor higher than 0.99, and the second stage LLC converter operates with high efficiency over the full output voltage range under ZVT.**

***Index Terms*— interleaved boost converter, LLC resonant converter, plug-in electric vehicle, on-board charger.**

I. Introduction

High power density, high conversion efficiency, high power factor, and low total harmonic distortion are the major features and capabilities desired from level-2 on-board plug-in electric vehicle (PEV) battery chargers [1–3]. Level-2 charger is located inside the vehicle and requires an electric vehicle supplement equipment (EVSE) mounted on the wall, which provides 240 V output [4], [5]. It is recognized as the primary intermediate charging power level rated up to 19.2kW, for both private and public facilities [6], [7].

Fig. 1 shows the general power electronic architecture of an on-board battery charger. The system consists of a front-end ac/dc converter used for rectification at unity power factor, and a second stage dc/dc converter responsible for battery current regulation and providing galvanic isolation [8], [9]. Selection of the optimal topology and optimization of the power loss in the semiconductors are important steps in the design and development of PEV battery chargers [10].

Boost converter is the common front-end PFC interface due to its simple structure, good total harmonic distortion (THD) reduction performance, and unity power factor operation capability [11]. However, with the increase of charging power, the volume of the converter tends to increase. Moreover, high root mean square (rms) current in the dc link capacitors would generate high power loss and seriously reduce the capacitor's lifetime, leading to capacitor failures [12]. In addition, the required inductance value to reduce the ripples in the input current for better THD performance, considerably increases as charging power increases, which results in a large-volume inductor core and wire size. In comparison to single phase boost rectifier, the interleaved boost topology has the benefit of reduced overall volume and improved power density [13], [14].

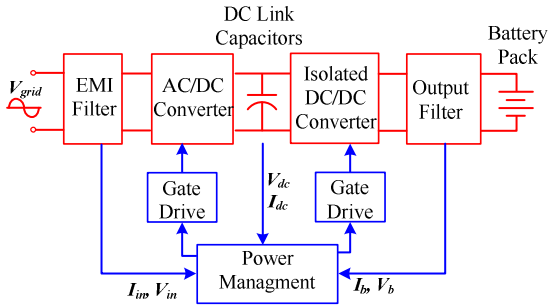

Fig. 1. General system architecture of a battery charger

In the dc/dc isolation stage, resonant converters are preferable at high voltage and high power. In particular, the LLC topology, which is based on multi-resonance and has advantages over other resonant topologies, such as: (a) high efficiency at high input voltage, (b) ability to operate with ZVT over wider load ranges, (c) no diode reverse recovery losses through soft commutation, (d) low voltage stress on the output rectifying diodes, and (e) having only a capacitor as the output filter as opposed to the conventional LC filters [15]. However, in PEV battery charging applications, the battery voltage varies in a wide range depending on the different states of charge (SOC) of the battery as well as different battery types [16]. Therefore, operating with maximum efficiency through reducing the conduction and switching losses over the full output voltage range is a challenging issue in LLC charger design.

In this paper, an on-board level-2 PEV charger topology composed of an interleaved boost PFC rectifier followed by an LLC multi-resonant is investigated and analyzed. The schematic of the proposed interleaved LLC charger is shown in Fig. 2. The design considerations for a highly efficient on-board charger rated at 7.6 kW, which corresponds to the maximum current of 32 A supplied from a single phase 240 V outlet, are discussed and detailed.

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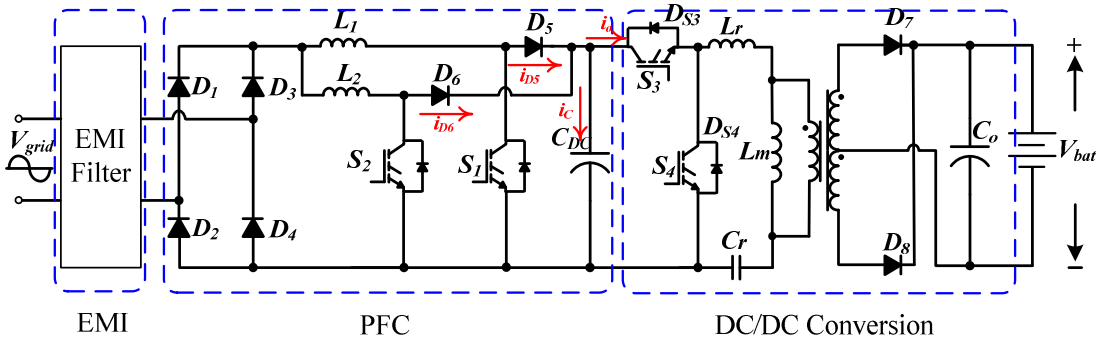

Fig. 2. Schematic of proposed interleaved level 2 isolated on board charger.

This paper is organized as follows; Section II introduces the proposed structure and explains the operation principles of both converters. Section III details the design considerations of LLC converter for a PEV battery charger. The results are presented and evaluated in Section IV. Finally, Section V summarizes the study and features the benefits based on the achieved results.

II. Proposed Interleaved LLC Charger

The schematic of the proposed interleaved LLC charger is shown in Fig. 2.

A. Interleaved Boost PFC Converter

An interleaved converter is simply a multi-leg converter, each leg operating $360^0/n$ out of phase, where n denotes the number of phases. In this structure, a two-leg interleaved boost converter, whose interleaving legs are operated with 180^0 phase difference, is utilized. Fig. 3 illustrates the waveforms of a two-leg interleaved boost converter. As seen from Fig. 3, the control of the interleaved converter is based on shifting the phase of S_1 with respect to S_2 such that the ripples cancel out each other. Eq. (1) shows the normalized input current ripple, $K(d)$, as a function of switching duty cycle, d.

$$K(d)=\frac{\Delta i_{in}}{\Delta i_L}=\begin{cases}\dfrac{1-2d}{1-d}, d\le 0.5\\ \dfrac{2d-1}{1-d}, d>0.5\end{cases} \quad (1)$$

As seen from Fig. 4, in comparison to single stage boost topology, the ripple current of the interleaved boost converter is improved over the full duty cycle range. Particularly at 50% duty cycle, a ripple-free current can be maintained.

Another advantage of an interleaved topology is that the input current is evenly shared between the interleaved inductors. For a two-leg interleaved topology, the energy stored in the inductor is defined as:

$$E=\frac{1}{2}L\left(\frac{i_{in,rms}}{2}\right)^2+\frac{1}{2}L\left(\frac{i_{in,rms}}{2}\right)^2=\frac{1}{4}Li_{in,rms}{}^2 \quad (2)$$

According to the Eq. (2), the energy stored in the inductor is half in comparison to single stage boost topology. This reduction could effectively reduce the inductor volume for the same performance criteria as of the conventional boost converter. In [17], a 500 W two-leg interleaved boost converter

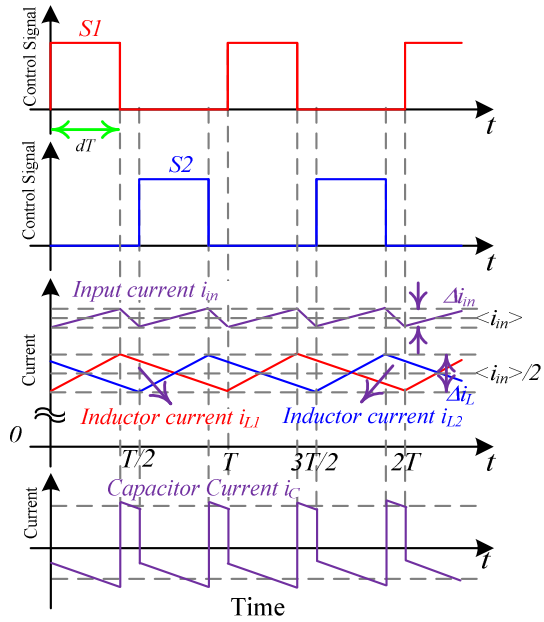

Fig. 3. Waveforms of two-leg interleaved boost converter ($d < 0.5$).

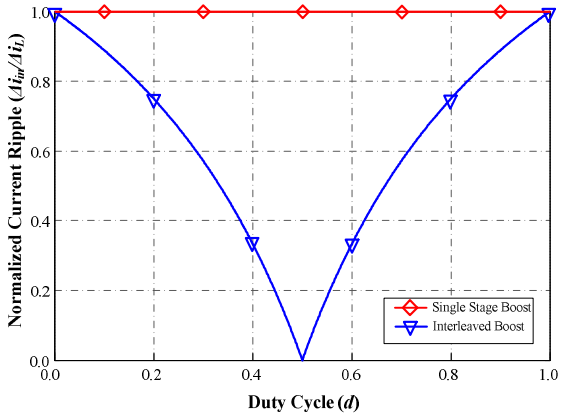

Fig. 4. Effective input current ripple cancellation in two-leg interleaved converter.

with 385 V output has been analyzed, and a volume reduction of 32% with an E-core inductor is reported.

High values of the output capacitor rms current causes more losses depending on the capacitor equivalent series resistance (ESR) and results in higher temperatures, which seriously shortens the capacitor life time [12].

The output capacitor current can be expressed as,

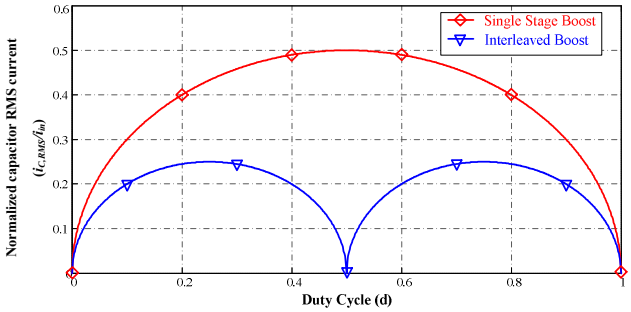

Fig. 5. Effective output capacitor rms current reduction in two-leg interleaved converter.

$$i_C = i_{D5} + i_{D6} - i_o \tag{3}$$

The normalized capacitor rms current ($i_{C,RMS}/i_{in}$) is a function of duty cycle, and could be derived as,

$$i_{C,RMS} / i_{in} = \begin{cases} \sqrt{-d^2+0.5d} & d \le 0.5 \\ \sqrt{-d^2+1.5d-0.5} & d > 0.5 \end{cases} \tag{4}$$

Fig. 5 shows the normalized capacitor rms current ($i_{C,RMS}/i_{in}$) in a single stage boost and in a two leg interleaved boost converters. The peak capacitor rms current is reduced to half in the interleaved structure. The improvement in capacitor rms current reduces the power loss dissipation in the ESR of the capacitor, reduces the electrical and thermal stress on the capacitor, and improves the system reliability.

B. Series LLC Half-Bridge Converter

In Fig. 6, half-bridge LLC multi-resonant converter is shown in three stages. In the first stage, the dc voltage source and two phase shifted complimentary switches operate as a square wave generator. The second stage is a series LLC resonant network. The third stage consists of the n:1 center tapped transformer, rectifier and a resistive load. The load resistance is equal to the load voltage divided by load current.

The resistive load in the secondary side of the transformer can be expressed as an effective resistor in the primary side [see Fig. 7 (a)]. To simplify the analysis, the leakage flux and parasitic effect in the secondary side of the transformer are ignored. For simplicity in the analysis, first harmonic approximation (FHA) method, in which only the first harmonic is allowed to pass the resonant network, is utilized [18]. The LLC converter could be modeled as shown in Fig. 7(b). The resistance of the equivalent ac resistor can be derived as,

$$R_{ac} = \frac{8}{\pi^2} n^2 R_L \tag{5}$$

According to the circuit model in Fig. 7(b), the voltage gain G, transconductance g, and input impedance Z_{in}, can be respectively expressed as,

$$G = \left|\frac{v_s}{v_{in}}\right| = \left|\frac{j\omega L_m \| R_{ac}}{j\omega L_m \| R_{ac} + j\omega L_r + 1/j\omega C_r}\right| \tag{6}$$

$$g = \left|\frac{i_s}{v_{in}}\right| = \frac{1}{R_{ac}}\left|\frac{v_s}{v_{in}}\right| = \frac{1}{R_{ac}}\left|\frac{j\omega L_m \| R_{ac}}{j\omega L_m \| R_{ac} + j\omega L_r + 1/j\omega C_r}\right| \tag{7}$$

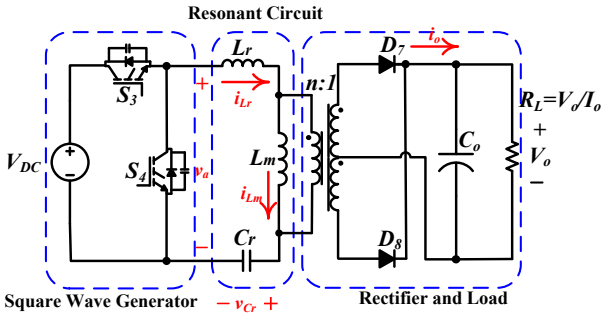

Fig. 6. Schematic of an LLC resonant half-bridge converter.

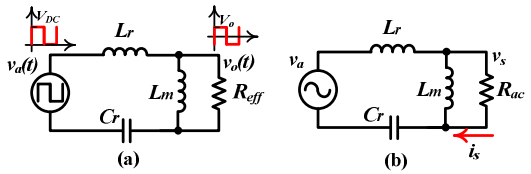

Fig. 7. (a) Simplified LLC half-bridge converter circuit. (b) Circuit model under first harmonic approximation (FHA).

$$Z_{in} = j\omega L_m \| R_{ac} + j\omega L_r + 1/j\omega C_r \tag{8}$$

The frequency responses of voltage gain and transconductance are plotted in Fig. 8. The resonance frequencies f_o and f_1 are defined in Eqs. (9) and (10),

$$f_o = \frac{1}{2\pi\sqrt{L_r C_r}} \tag{9}$$

$$f_1 = \frac{1}{2\pi\sqrt{(L_r + L_m) C_r}} \tag{10}$$

To illustrate different load conditions, quality factor Q is introduced. Q is defined to be the ratio between characteristic impedance ($\sqrt{L_r/C_r}$) and the load resistance.

$$Q = \frac{\sqrt{L_r / C_r}}{R_{ac}} \tag{11}$$

Large Q corresponds to small load resistance and heavy load condition. On the contrary, small Q corresponds to large load resistance and light load condition.

As seen from Fig. 8 (a), the peak voltage occurs somewhere between f_o and f_1. From no load condition (Q = 0) to short circuit condition (Q = ∞), the frequency corresponding to the peak voltage shifts from f_1 to f_o. At f_o, the converter behaves like a constant voltage source. From Fig. 8 (b), the peak current occurs somewhere between f_o and f_1. From short circuit condition (Q = ∞) to no load condition (Q = 0), the frequency corresponding to the peak current shifts from f_o to f_1. At f_1, the converter behaves like a constant current source.

The input impedance, Z_{in}, can be capacitive or inductive. If Z_{in} is capacitive, the current leads the voltage, which makes both freewheeling diodes D_{S3} and D_{S4} turned off at a finite current and a finite voltage. In this case, the freewheeling diodes must have good reverse-recovery characteristics to avoid large reverse spikes flowing through the switches, and to minimize the diode turn-off losses. On the other hand, If Z_{in} is inductive, the current lags the voltage, which makes both freewheeling diodes D_{S3} and D_{S4} turned off at zero current and zero voltage. Thus, the freewheeling diodes do not need to have very fast reverse-recovery characteristics. In our application,

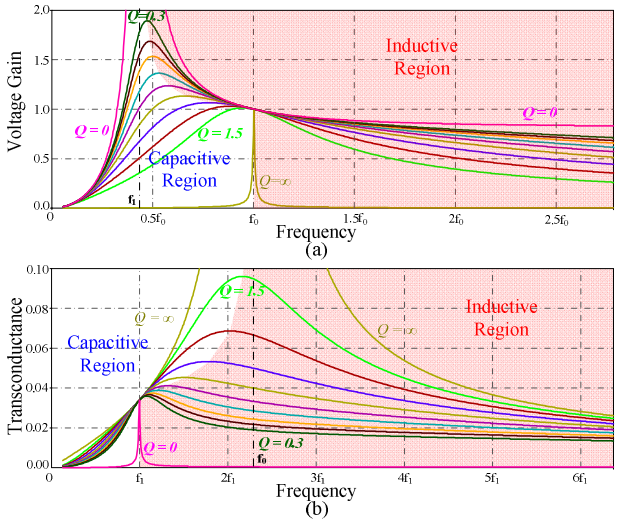

Fig. 8. Dc characteristic of LLC resonant converter: (a) voltage characteristic (b) current characteristic.

since the MOSFETs are utilized as the primary switches in high frequency, inductive region is preferable.

When the switching frequency is higher than f_o, the resonant network is inductive. When the switching frequency is lower than f_1, the resonant network is capacitive. In between f_1 and f_o, inductive or capacitive is determined by the load. The capacitive and inductive regions are marked in Fig. 8.

On the other hand, as the switching frequency is closer to f_o, the impedance of the resonant tank becomes smaller. This can reduce the circulating energy in the resonant tank, which results in reduction in the conduction losses of the LLC converter. Generally, the LLC converter is desired to operate in the inductive region and close to f_o for minimizing switching and conduction losses, i.e. maximizing efficiency.

For design considerations, f_o is preset by the optimum operating frequency of the MOSFETs, considering the tradeoff between high frequency operation and switching power loss. Thus, the product of L_r and C_r can be determined as the initial design step. Short circuit performance ($Q = \infty$) and peak voltage gain at maximum output power ($Q = Q_{turn}$) are two important considerations in designing L_r and C_r. When the short circuit happens, the power management module shifts the switching frequency to a higher value ($2 \sim 3f_o$) to increase the impedance of the resonant tank, hence, the short circuit current could be effectively reduced and limited to a predetermined value. If L_r is large, the resonant tank impedance becomes large as well, while the short circuit current becomes smaller. However, for a constant f_o, a larger L_r would result in a smaller C_r, which increases the voltage stress of the resonant capacitor as well as the quality factor. This would cause the peak voltage gain at heavy load condition become smaller and potential failure to fulfill the specification of desired application. The values of L_r and C_r are determined based on this tradeoff.

The design of L_m is based on the tradeoff between conduction losses and switching losses. Smaller L_m corresponds to smaller operation frequency range, which provides lower conduction losses. However, if L_m decreases, the switch turning off current increases, which in turn would result in higher switching losses. The values of L_m is determined from this tradeoff.

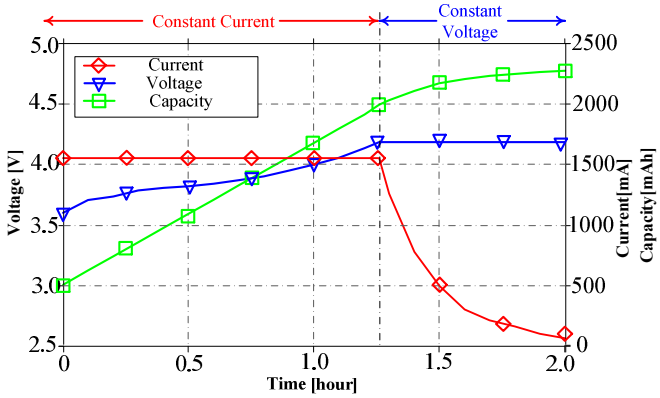

Fig. 9. Charging characteristics of a Li-Ion battery cell.

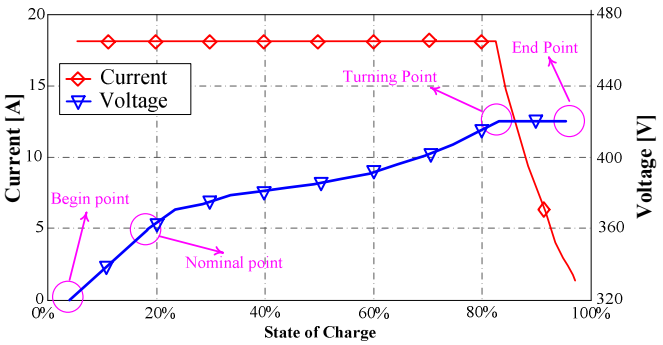

Fig. 10. Charging profile of the Li-Ion battery pack.

III. Designing a 7.6 kW PEV Charger Prototype

In this section, an interleaved LLC PEV charger is designed based on the design considerations discussed in Section II. The design considerations are provided for a level-2 charger rated at 7.6 kW. It is aimed to charge a Li-ion battery with 360 V nominal voltage from depleted to fully charged conditions. The charging process is divided into constant current (CC) and constant voltage charging (CV) stages.

A. Charging profile of the Li-ion battery

Fig. 9 provides the charging characteristics of a single Li-ion battery cell. The nominal voltage of the battery is 3.6 V. Based on the charging data of a single battery cell, the charging profile of a Li-ion battery pack could be obtained, as plotted in Fig. 10.

According to Fig. 10, there are four key points in the charging process.

1) *Begin point:* Begin point corresponds to the lowest stage of charge. At this point, the battery pack has the minimum voltage (320 V). The charging current equals to 18.1 A. The equivalent load resistance which corresponds to the battery charging power of 5.8 kW is calculated as 17.7 Ω.

2) *Nominal point:* The voltage is equal to the nominal voltage (360 V) while the charging current still equals to 18.1 A. The corresponding load resistance at 6.5 kW is 19.9 Ω.

3) *Turning point:* Turning point is the intersection between CC charging and CV charging modes. The voltage is 420 V, and maximum power (7.6 kW) is achieved at this point. The charging current is still 18.1 A. The equivalent load resistance is 23.2 Ω.

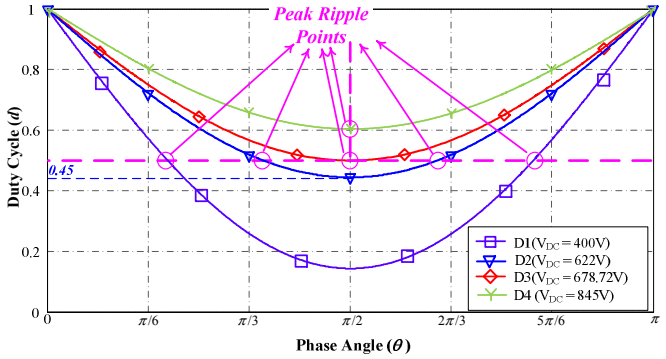

Fig. 11. Duty cycles corresponding to different DC link voltages in conventional PFC boost rectifier.

4) *End point:* End point marks the end of the constant voltage charging and also the end of the whole charging process. The load resistance corresponds to 420 Ω.

The corresponding quality factors at different operating points could be calculated from Eq. (12).

$$Q = \frac{\sqrt{L_r / C_r}}{8n^2/\pi^2 \times R_L} \tag{12}$$

In the following section, the charger is designed based on these four operation points.

B. Interleaved Boost PFC Converter Design

For boost converter in PFC application, the instantaneous duty cycle d varies with the input voltage as,

$$d(\theta) = 1 - \frac{|V_{in}|}{V_{DC}} = 1 - \frac{339.36 \times |\sin\theta|}{V_{DC}} \tag{13}$$

where 339.36 V is the peak input voltage, and θ is the phase angle between the input voltage and current. The input current ripple can be expressed as,

$$\Delta I_{in} = \frac{|V_{in}|}{L} d(\theta) T_s = \frac{339.36 T_s}{L}\left(|\sin\theta| - \frac{339.36}{V_{DC}}(\sin\theta)^2\right) \tag{14}$$

Assume $x = |\sin\theta|$, then $0 \le x \le 1$. The derivative of ΔI_{in} is calculated as Eq. (15)

$$\frac{\delta \Delta I_{in}}{\delta x} = \frac{339.36 T_s}{L}\left(1 - \frac{678.72}{V_{DC}} x\right) \tag{15}$$

According to Eq. (15), if $V_{DC} \le 678.72$ V, the peak ripple happens when $x = V_{DC}/678.72$. Substituting x into Eq. (12), d is calculated to be 0.5. If $V_{DC} > 678.72$ V, the peak ripple happens when $x = 1$ and $\theta = \pi/2$. Based on the previous analysis in Section II-A, duty cycle close to 50% provides the best inductor current ripple cancellation.

According to the Eq. (13), duty cycles corresponding to different dc link voltages in conventional PFC boost converter (400 V, 622 V, 678.72 V, and 845 V) are plotted in Fig. 11. As seen from the figure, the curve corresponding to 622 V dc link voltage outperforms the others, since its duty cycle is closer to 0.5.

The circuit is designed to operate at 100 kHz switching frequency taking the tradeoff between the sizes of the inductors and dc link filter capacitor and switching losses into account. The inductance should be large enough to suppress the THD. The capacitance of dc link capacitor determines the output voltage ripple. In this design, the inductances and capacitance are selected as 280 μH and 1.8 mF, respectively.

C. Series LLC Half-Bridge Converter Design

The parameters in the dc/dc stage can be designed based on the dc voltage and current characteristics of LLC resonant converter.

1) *Selection of the turns ratio of transformer*

For the battery charger applications, the target is to optimize the performance at high battery voltage, where the highest conduction loss and thereby lowest efficiency is expected. From previous analysis, the optimal operation point is when switching frequency equals to f_o. At this point, the converter behaves like a constant voltage source. In this case, the voltage corresponding to f_o is determined to be equal to the nominal voltage of the battery pack. The transformer turns ratio can be calculated as,

$$n = \frac{V_{DC}}{2(V_{nom} + V_d)} = 1 \tag{16}$$

where, V_d is the voltage drop across the diode.

2) *Selection of L_r and C_r*

The optimal operation frequency was determined as f_o = 200 kHz. According to Eq. (9), the product of L_r and C_r can be found as,

$$\sqrt{L_r C_r} = 1/(2\pi f_o) = 7.96 \times 10^{-7} \tag{17}$$

As mentioned earlier in Section II-B, there is a tradeoff between the peak voltage gain at heavy load and the short circuit current. In this case, the peak voltage gain at the turning point is the heaviest load condition in CV charging mode. The voltage gain must be larger than 420/360 = 1.17. The short circuit current should be smaller than the maximum current of the charger (19.1 A). Based on this tradeoff, the quality factor at the turning point Q_{turn} is selected to be 0.5, which satisfies the peak gain voltage and short circuit current requirements. Thus, the ratio between L_r and C_r could be determined by Eq. (18).

$$\sqrt{L_r / C_r} = Q_{turn} \times \frac{8n^2}{\pi^2} \times 23.2\Omega = 9.4 \tag{18}$$

From Eqs. (17) and (18), L_r and C_r could be calculated as 7.48 μH, and 84.6 nF, respectively.

3) *Selection of the inductance ratio L_m/L_r*

As discussed in Section II-B, the design of L_m is based on the tradeoff between conduction losses and switching losses. Decreasing the inductance ratio would increase the turning off current and the switching losses. While increase of the inductance ratio would make the converter operate in frequencies far from f_o and increase the conduction losses. Different ratios between L_m and L_r are investigated. The optimal inductance ratio is found to be equal to 4. Thus, the magnetizing inductance is 26.92 μH.

Voltage and current curves using the determined L_m and L_r parameters, which correspond to begin point, nominal point, turning point, end point, and short circuit condition, are plotted in Fig. 12.

According to Fig. 12 (a), in CV charging mode, the output voltage is constrained at 420 V which is the fully charged battery pack voltage. From the turning point to the end point, the switching frequency increases from 161.9 kHz to 166.4

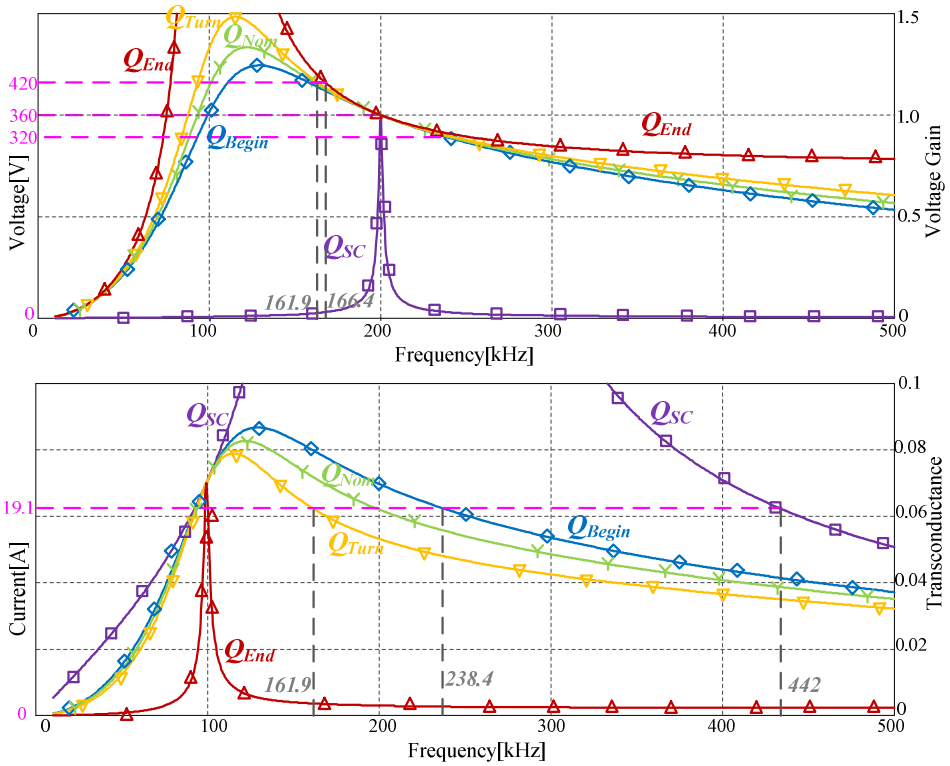

Fig. 12. Dc characteristics of the designed 7.6kW LLC converter: a) voltage characteristic b) current characteristic.

kHz. According to Fig. 12 (b), in CC charging mode, the charging current is constrained at 19.1 A. From the begin point to the turning point, the switching frequency decrease from 238.4 kHz to 161.9 kHz. Under short circuit condition, the switching frequency needs to be boosted to be higher than 442 kHz, so that the short circuit current could be lower than the nominal current.

IV. Simulation Results and Discussion

A. Simulation results

Simulations are carried out for both stages of the proposed EV battery charger prototype with the parameters shown in Table I.

The waveforms achieved in the first stage interleaved boost converter are presented in Fig. 13. According to Fig. 13, the input current is in phase with the input voltage. The converter demonstrates power factor equal to 0.999. The voltage ripple in the dc link capacitor is 18 V. In comparison to the inductor current ripple, the input current ripple is improved. As seen from Fig. 13 (e), THD is 3.61%. The harmonic component at switching frequency (200 kHz) is well suppressed.

The simulation results of the second stage LLC converter are presented in Figs. (14-16). Fig. 14 demonstrates the operation at the begin point. Switching frequency is regulated at 195 kHz. Fig. 15 shows the waveforms of the operation at the nominal point. Switching frequency is regulated at 171 kHz. Likewise, Fig. 16 presents the operation at the turning point. The 7.6 kW peak power is achieved at this point. Switching frequency is regulated at 151 kHz.

TABLE I
Design of a Level-2 Interleaved LLC On-Board Charger

Symbol	Quantity	Parameter
L_1, L_2	Boost inductor	270 µH
C_{dc}	DC link capacitor	1.8 mF
V_{in}	Input voltage	240 V/60 Hz
V_{DC}	DC link voltage	622 Vdc
V_b	Battery voltage range	320 V to 420 V
P_{max}	Rated maximum power	7.6 kW
f_o	Primary resonant frequency	200 kHz
f_l	Secondary resonant frequency	100 kHz
n	Transformer turn ratio	1
L_m	Magnetizing inductor	22.92 µH
L_r	Resonant inductor	7.48 µH
C_r	Resonant capacitor	84.6 nF
C_f	Output filter capacitor	10 µF
L_m/L_r	Inductance ratio	4

The simulation result of the LLC resonant converter is summarized in Table II. The switching frequency varies from 151 kHz to 195 kHz. This range is close to the primary resonant frequency f_o (200 kHz), which make the impedance of the resonant tank small. Thus, the circulating energy in the resonant tank is small, which minimizes the conduction losses.

B. Discussion

With respect to the analysis in Section III-C, switching frequency used in the simulation at the turning point (151 kHz) is slightly lower than the theoretical analysis (161.9 kHz). Likewise, the switching frequency used in the simulation at the begin point (195 kHz) is smaller than the theoretical analysis (238.4 kHz). This difference is because of the error of first

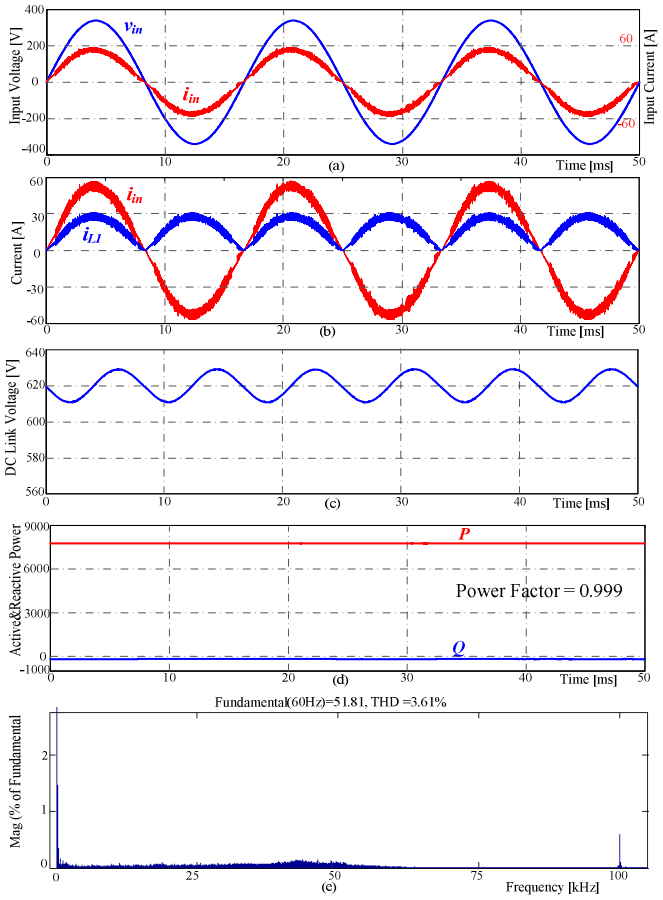

Fig. 13. Simulation results for the interleaved boost PFC converter.

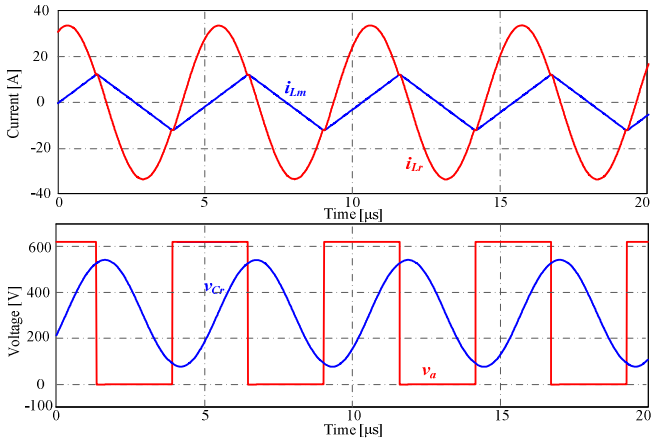

Fig. 14. LLC results at the begin point (V_o = 320 V, I_o = 19.1 A, f = 195 kHz).

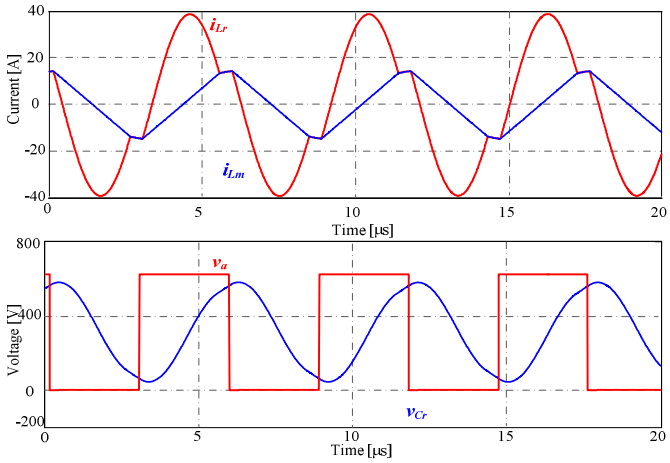

Fig. 15. LLC results at the nominal point (V_o = 360 V, I_o = 19.1 A, f = 171 kHz).

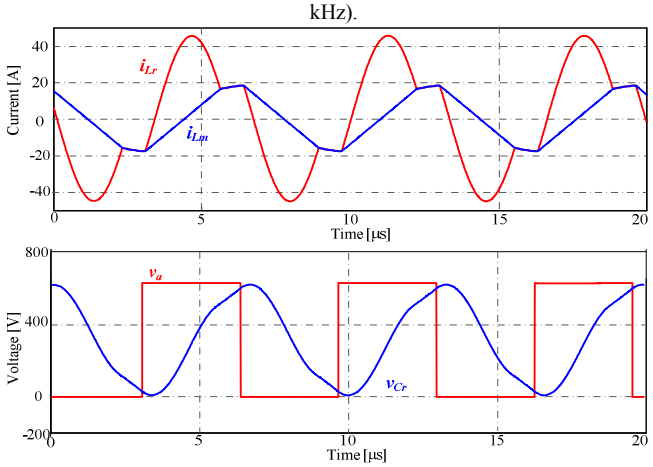

Fig. 16. LLC results at the turning point (V_o = 420 V, I_o = 19.1 A, f = 151 kHz).

TABLE II
SUMMARY OF THE LLC CONVERTER SIMULATION RESULTS

Quantity	Parameter
Q range	0.66 to 0.02
Frequency range	151 kHz to 195 kHz
Short circuit frequency	450 kHz
Max switch turn-off current	19 A
Output voltage range	320 V to 420 V
C_r voltage rating	650 V
L_r current rating	45 A

harmonic approximation. In practice, at the primary resonant frequency, the voltage gain varies slightly with the change of the load. As the load gets heavier, the voltage gain becomes smaller. In order to follow the battery voltage, the frequency should be reduced to boost the voltage gain. Since the slope of the gain curve in the heavy load is small, the frequency needs to be reduced more to meet the gain requirement.

V. CONCLUSIONS

In this paper, a level-2 on board PEV battery charger is proposed. Interleaved boost topology is used in the first stage for PFC and THD reduction as well as reducing volume of the magnetic components. In the second stage, a half bridge LLC resonant converter is employed to achieve high conversion efficiency over the full voltage range of the battery pack.

The suitability and advantages of the proposed converter are discussed and design guidelines are provided through theoretical analyses for both converter topologies. As a case study, design considerations for a 7.6 kW level-2 charger, which converts 240 V, 60 Hz AC to battery voltage range of 320 V to 420 V are provided, considering the characteristics of the converter. Moreover, the charging profile of a 360 V battery pack is detailed to provide guideline to the charger design.

Finally, the simulation results are presented for validation. The first stage interleaved boost converter demonstrates unity

power factor operation at the rated power and achieves THD less than 4%. In the second stage LLC converter, the switching losses and conduction losses are optimized through operating the converter close to resonance frequency of the resonant tank. Experimental verification of the proposed design approach lays out the future research direction.

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