A Phase Shift Full Bridge Based Reconfigurable PEV Onboard Charger With Extended ZVS Range and Zero Duty Cycle Loss

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***Abstract*—In this paper, an integrated onboard charger architecture is proposed for plug-in electric vehicle (PEV). In this architecture, the phase shift full bridge (PSFB) converter serves as the main high voltage battery charging topology, and the half bridge LLC resonant converter serves as the low voltage battery charging topology. Under light charging mode, the half-bridge LLC is reconfigured to be paralleled with the PSFB topology, to guarantee zero voltage switching (ZVS) of the lagging-leg MOSFETs. Practical design considerations are presented for both the PSFB and the half bridge LLC converters. Switching frequency and the shifted phase angle provide two degrees of freedom to regulate the output voltage/current of both converters. The proposed architecture maintains low cost and high efficiency in this specific application. A 390V input, 420V/2.4A, 14V/21A outputs converter prototype is designed, simulated, and analyzed to verify the proof of concept.**

Keywords—integrated charger; LLC; onboard charging; PEV; PSFB; ZVS;

I. INTRODUCTION

Both the environmental problems and the energy crisis have been pushing the transition from conventional internal combustion engine vehicles towards more electrified plug-in electric vehicles (PEV) [1], [2]. In order to achieve a longer electric mileage, a high voltage Li-ion battery pack is installed onboard. Thus, an onboard battery charger is mandatary to charge this high voltage battery pack [3], [4]. Plus, a low voltage lead-acid battery (12V/14V) is installed onboard to provide power to the auxiliary loads, such as the air conditioner, head lights, stereo systems [5].

The typical configuration of the power management system in PEV is plotted in Fig. 1. There are three major power modules: a) onboard charger for the high voltage battery, b) propulsion motor drive, and c) low voltage battery charger. It should be noted that both the high voltage charger and the low voltage charger require an isolated DC/DC conversion stage.

The PSFB dc/dc topology as shown in Fig. 2. (a), enjoys the benefits of a) simple circuit structure with reduced components count, b) zero voltage switching of MOSFETs,

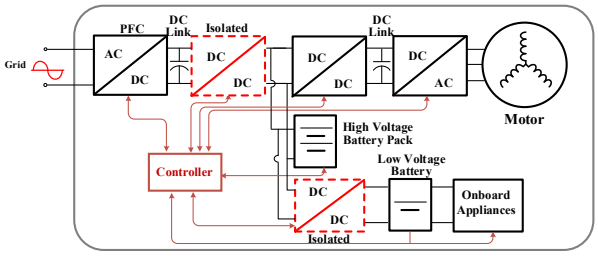

Fig. 1. Power management architecture of a full electric vehicle.

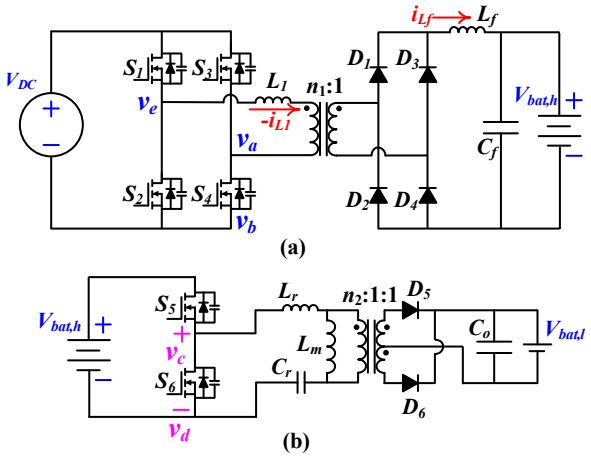

Fig. 2. Conventional onboard charger topologies: a) PSFB based high voltage battery charger, and b) Half bridge LLC based low voltage battery charger.

and c) easy to control with pulse width modulation. Therefore, it has been widely used in the PEV onboard battery chargers [6]–[8]. Regarding to the low voltage battery charger, half bridge LLC topology as shown in Fig. 2. (b), is considered as a good candidate due to its wide voltage gain range and ZVS features.

However, the traditional ZVS PSFB dc–dc converter has two fundamental limitations: a) the lagging leg MOSFETs lose ZVS feature under light load conditions, and b) the duty cycle loss problem. Many research efforts have been made to solve those problems [9]–[13]. Ideas on utilizing the ZVS half bridge

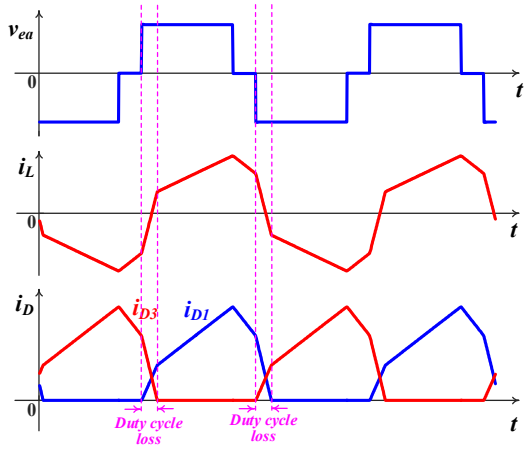

Fig. 3. Duty cycle loss of PSFB converter at heavy load condition.

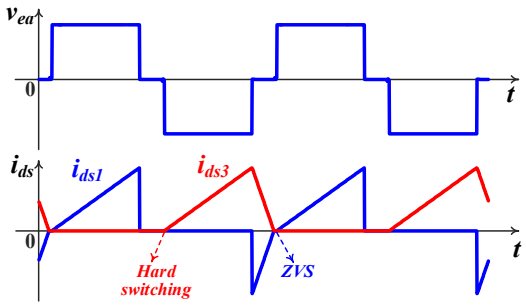

Fig. 4. PSFB MOSFET drain-source I-V waveforms under light load condition.

LLC topology to mitigate the hard switching problems on the PSFB lagging leg have attracted special attention [14]–[17]. In [14], a dual output dc/dc converter combining PSFB and half bridge LLC topologies is proposed to achieve the ZVS of the lagging leg. However, the proposed converter still suffers from duty cycle loss problems and design considerations are not optimized for the PEV specific applications. In [15], a PSFB and LLC integrated topology is proposed with the dual outputs in series; in [16], a PSFB and LLC integrated topology is proposed with the LLC output in series with the PSFB auxiliary capacitor; while in [17], PSFB and LLC outputs are simply in parallel. However, all those converters significantly increases the components count, and the secondary side always suffers from doubled diode conduction losses. Moreover, the parallel topology proposed in [17] suffers from increased control complexity.

In this paper, a self-reconfigurable PEV onboard charger is proposed. In the proposed architecture, an auxiliary circuit is added to the secondary side of the PSFB topology. This modification eliminates the duty cycle loss problem and mitigates the turning off d*i*/d*t* on the secondary diodes. Moreover, under light load charging mode, the half bridge LLC based low voltage battery charger can be switched to the DC link (AC/DC stage output) of the PSFB converter. Therefore, the proposed architecture can achieve those benefits simultaneously: a) full ZVS range of the lagging leg; b) zero duty cycle loss and reduced circulating currents; c) relative low

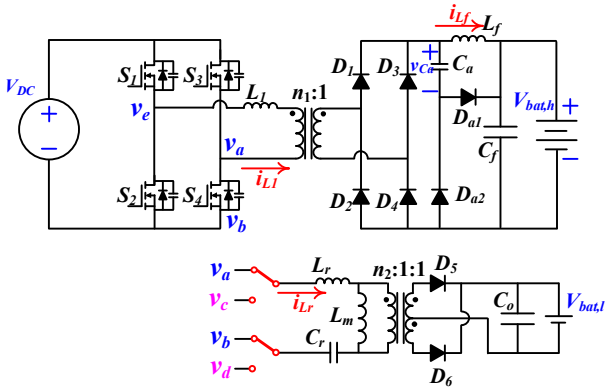

Fig. 5. Proposed self-reconfigured onboard charger topology combination.

circuit components count due to the topology reuse; and d) reduced secondary side diode turning off losses.

II. Issues with Conventional PSFB Topology

PSFB converter is a classic ZVS isolated dc/dc topology and has been well studied. By actively controlling the phase shift amount between the leading phase leg and the phase lagging leg, the root mean square voltage exposed to the transformer primary side can be actively controlled. Therefore, the voltage/current regulation can be achieved by phase shift control. Its main issues are summarized as below.

A. Duty cycle loss at heavy load condition

At heave load condition, PSFB topology suffers from duty cycle loss. Duty cycle loss occurs when the current entering into the transformer primary side ($-i_{L1}$ as defined in Fig. 1) intersect with the secondary side output current (i_{Lf} as defined in Fig. 1). From this moment on, all the diodes (D_1-D_4) on the secondary side are off. This phenomenon is marked in Fig. 3.

During the duty cycle loss mode, the transformer secondary side sees a short circuit. Thus, no power is delivered to the load side, and the current will be circulating on the primary side tank. This squeezes the effective power supply duty cycle and increases the conduction losses. Moreover, in order to deliver the required amount of power to the load, the circuit components need to stand higher current stresses due to the low power supply utilization rate.

B. ZVS feature loss in the lagging leg at light load condition

The ZVS mechanism of power MOSFET is detailed as: before the current conduction through the MOSFET channel, there is a current from the source terminal to the drain terminal of the MOSFET. This current goes through the MOSFET body diode and creates a zero voltage condition for the MOSFET channel. Thus, ZVS is achieved when the current intersects with zero and the conduction is switched from the body diode to the channel. This ZVS feature can be observed among all the power MOSFETs.

However, with the decrease of load power, this source to drain current on the lagging leg MOSFETs decays. When the integral of this current during the dead band cannot fully

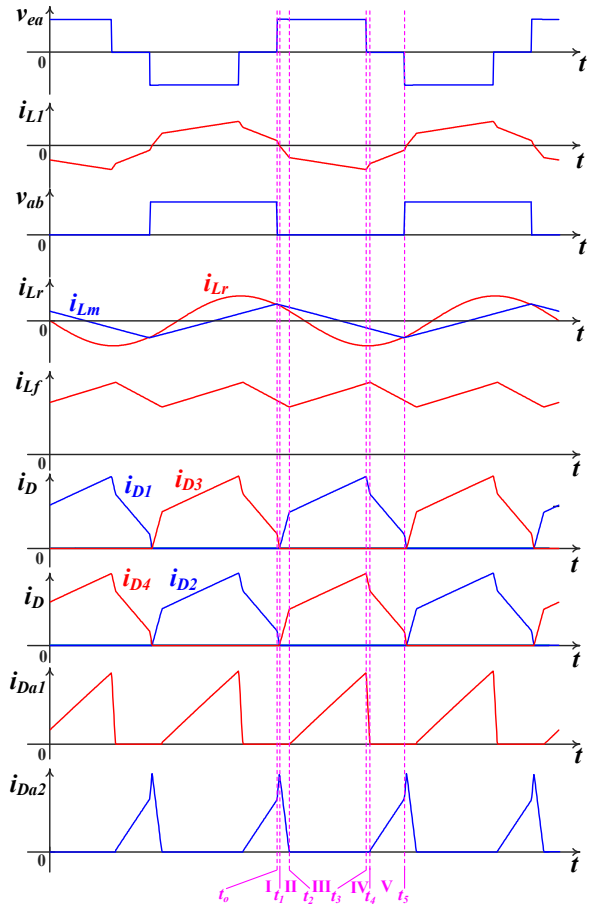

Fig. 6. Key waveforms of the circuit.

charger and discharge the lagging leg MOSFET output capacitances, the ZVS feature is lost. This can be clearly observed from Fig. 4. As shown on the waveform of i_{ds3} in Fig. 4, before i_{ds3} crosses with zero, there is not a negative current to pre-charge or pre-discharge C_{oss}.

This ZVS loss problem brings severe ringing and EMI problems to the circuit. To reduce the ringing and EMI, typically a lossy snubber and an additional bulky passive filtering tank is required. Thus, both the conversion efficiency and the power density decays.

III. Proposed Reconfigurable PEV Onboard Charger

A. Topology Description

The proposed reconfigurable PEV onboard charger is plotted in Fig. 5. As shown, by adopting two single-pole-double-throw relays, the half bridge LLC topology in the low voltage battery charger can be re-connected to the lagging leg of the PSFB converter. Moreover, a capacitor diode network is added on the secondary side of the PSFB topology. This network can eliminate the duty cycle loss problem of PSFB converter.

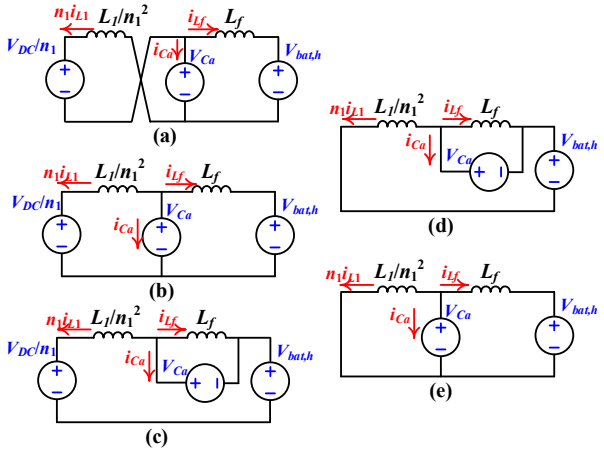

Fig. 7. PSFB equivalent circuits of different operation modes during one half switching cycle. a) Mode I: $t_0 \le t < t_1$; b) Mode II, $t_1 \le t < t_2$; c) Mode III, $t_2 \le t < t_3$; d) Mode IV, $t_3 \le t < t_4$; e) Mode V, $t_4 \le t < t_5$.

B. Operation Principle

Key waveforms of the proposed circuit is plotted in Fig. 6. As shown, in each half switching cycle, there are five different operating modes. The next half switching cycle is symmetrical to the first switching cycle. To facilitate the analysis, one specific half switching period, [t_0, t_5) is extracted from Fig. 6. The five operating modes of PSFB stage during this half switching cycle corresponds to five equivalent circuits as shown in Fig. 7. It should be noted that the primary side voltage source and impedance are both equivalent to the secondary side.

The following analysis is based on the assumption: C_a, C_f, and C_o are sufficiently large such that one can ignore their voltage ripples. Thus, those capacitor voltages are considered as dc voltages, V_{Ca}, $V_{bat,h}$, and $V_{bat,l}$, respectively.

Mode I: [t_0, t_1). Mode I starts when S_3 is turned off and S_4 is turned on. The full bridge generates a positive voltage V_{DC}. D_2, D_3 conduct on the secondary side. Therefore, V_{DC} is coupled to be $-V_{DC}/n_1$ on the secondary side. D_{a2} conducts. Thus, negative terminal of C_a is connected to the isolated ground, as demonstrated in Fig. 7(a). Mode I ends when i_{L1} reaches zero. i_{L1} decreases linearly as,

$$\frac{di_{L1}}{dt} = \frac{-V_{DC} - n_1 V_{Ca}}{L_1} \tag{1}$$

i_{Lf} decreases linearly as,

$$\frac{di_{Lf}}{dt} = \frac{-V_{bat,h} + V_{Ca}}{L_f} \tag{2}$$

It should be noted that $i_{Ca} = n_1 i_{L1} - i_{Lf}$ in mode I.

Mode II: [t_1, t_2). D_2, D_3 are off while D_1, D_4 are on. Therefore, V_{DC} is coupled to be V_{DC}/n_1 on the secondary side. D_{a2} keeps conducting. Thus, negative terminal of C_a is connected to the isolated ground, as demonstrated in Fig. 7(b). Mode II ends when i_{Da2} reaches zero and D_{a2} is turned off. In this mode, i_{L1} decreases linearly as,

$$\frac{di_{L1}}{dt}=\frac{-V_{DC}+n_1V_{Ca}}{L_1} \tag{3}$$

In Mode II, i_{Lf} still decreases linearly following Eq. (2). While $i_{Ca}=-n_1i_{L1}-i_{Lf}$ in modes II-V. The initial value of $i_{L1}(t_1)=0$, which can facilitate solving the time-domain expression for $i_{L1}(t)$.

Mode III: [t_2, t_3). D_1, D_4 are still on and V_{DC} is coupled to be V_{DC}/n_1 on the secondary side. D_{a1} is on. Thus, C_a is paralleled with the filtering inductor L_f, as demonstrated in Fig. 7(c). Mode III ends when S_1 is turned off and S_2 is turned on. In this mode, i_{L1} decreases linearly as,

$$\frac{di_{L1}}{dt}=\frac{n_1V_{Ca}-V_{DC}+n_1V_{bat,h}}{L_1} \tag{4}$$

i_{Lf} increases linearly as,

$$\frac{di_{Lf}}{dt}=\frac{V_{Ca}}{L_f} \tag{5}$$

Mode IV: [t_3, t_4). S_2 and S_4 are both on. Thus, the output of the full bridge is zero. D_1, D_4 are still on and zero is coupled to the secondary side. D_{a1} is still on. Thus, C_a is still paralleled with the filtering inductor L_f, as demonstrated in Fig. 7(d). Mode IV ends when i_{Da1} reaches zero and D_{a1} is turned off. In this mode, i_{L1} increases linearly as,

$$\frac{di_{L1}}{dt}=\frac{n_1V_{Ca}+n_1V_{bat,h}}{L_1} \tag{6}$$

In Mode III, i_{Lf} still increases linearly following Eq. (5).

Mode V: [t_4, t_5). S_2 and S_4 are both on. Thus, the output of the full bridge is zero. D_1, D_4 are still on and zero is coupled to the secondary side. D_{a2} conducts. Thus, negative terminal of C_a is connected to the isolated ground, as demonstrated in Fig. 7(e). Mode V ends when S_3 is turned on and S_4 is turned off and the circuit operation enters into the second half cycle. In this mode, i_{L1} increases linearly as,

$$\frac{di_{L1}}{dt}=\frac{n_1V_{Ca}}{L_1} \tag{7}$$

i_{Lf} decreases linearly following Eq. (2). Itt should be noted that,

$$t_3-t_0=\frac{T_s}{2\pi}(\pi-\varphi) \tag{8}$$

where, φ is the shifted phase angel between the leading and lagging legs. φ is an actively controlled variable.

Assuming that all the circuit components are ideal, all the input power is delivered to the high voltage battery pack. According to the law of energy conservation,

$$P_{in}=\frac{\int_{t_0}^{t_0+\frac{T_s}{2\pi}(\pi-\varphi)}V_{DC}i_L(\mathrm{t})dt}{T_s/2}=V_{bat,h}I_{charge} \tag{9}$$

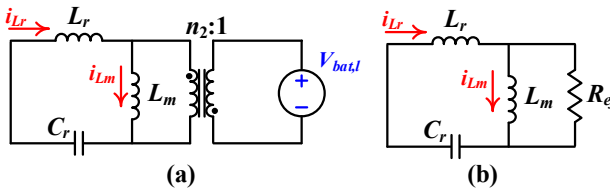

Fig. 8. a) LLC equivalent circuit during one half switching cycle, [t_0-t_5); b) circuit model using FHA.

According to the charge balance of the auxiliary capacitor, C_a,

$$\int_{t_0}^{t_0+\frac{T_s}{2}}i_C(\mathrm{t})dt=0 \tag{10}$$

Therefore, if circuit parameters (L_1, L_f, n_1, V_{DC}, I_{charge}, φ) are considered as known variables, the two unknown voltages, V_{Ca}, and $V_{bat,h}$ could be represented by those known variables based on the two equations (9-10). This means that the dc operating point of this converter can be solved numerically.

Regarding to the half bridge LLC converter, during this half switching cycle defined by [t_0-t_5), S_4 is always on. Thus, the input to the LLC resonant tank is always grounded, as shown in Fig. 8(a). D_6 is always on. Thus, the low voltage battery ($-V_{bat,1}$) is connected to the secondary side of the transformer. The magnetizing inductor voltage is clamped to be $-n_2V_{bat,1}$. Thus, i_{Lm} decrease linearly. i_{Lr} and v_{Cr} resonates sinusoidally. This could be observed from Fig. 6.

The LLC circuit can be modeled based on the first harmonic approximation (FHA) [18]. The secondary side of the transformer is equivalent to an effective resistance,

$$R_{eff}=\frac{8n^2}{\pi^2}\frac{V_{bat,l}}{I_{bat,l}} \tag{11}$$

The LLC circuit model using FHA is plotted in Fig. 8(b). Utilizing this circuit model, the voltage gain can be predicated. It should be noted that this predication demonstrates good accuracy when the switching frequency is close to the resonant frequency between L_r and C_r [19].

IV. Design Considerations

A. *ZVS condition of the lagging leg MOSFETs*

The ZVS of the lagging leg MOSFETs is achieved by the joint force of i_{L1} and i_{Lr}. The corresponding critical waveforms are plotted in Fig. 9, where Fig. 9(b) illustrates the more detailed waveforms during the dead band (t_{tead}).

Fig. 10 shows the equivalent circuit during the dead band. Both S_3 and S_5 have their channels off. $i_{L1}+i_{Lr}$ jointly charges C_{oss3} from 0V to V_{DC}, and discharges C_{oss4} from V_{DC} to 0V. Therefore, the ZVS condition is defined as,

$$\int_{t_0}^{t_0+t_{dead}}\left[i_{L1}(\mathrm{t})+i_{Lr}(\mathrm{t})\right]dt\geq 2C_{oss}V_{DC} \tag{12}$$

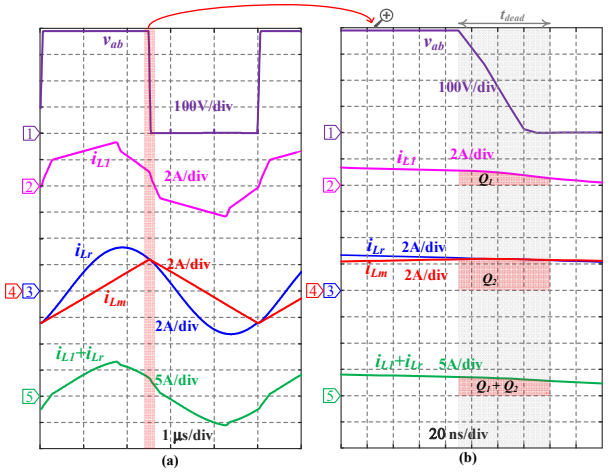

Fig. 9. ZVS waveforms of the lagging leg.

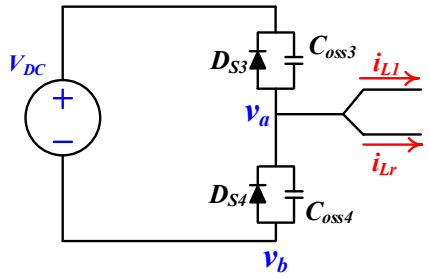

Fig. 10. Charging/discharging MOSFETs output capacitors during the dead band of the lagging leg.

As can be observed from Fig. 9(a), $i_{L1}(t)$ can be considered as a constant current source during this narrow dead band. $i_{L1}(t)$ can be calculated as,

$$i_{Lr}(t)\big|_{t\in[t_0,t_0+t_{dead})} = i_{Lr}(t_o) = \frac{T_s n_2 V_{bat,1}}{4L_m} \tag{13}$$

It should be noted that $i_{L1}(t)$ can be derived based on the circuit analysis in Section III. Thus, the ZVS condition of lagging leg MOSFETs can be achieved once Eq. (12) is satisfied.

B. LLC tank parameters selection

Regarding to the LLC part, the resonant tank L_r, C_r, L_m are the most important design parameters. To guarantee the optimized operation of the LLC converter, the switching frequency should be equal to the resonant frequency,

$$f_s = \frac{1}{2\pi\sqrt{L_r C_r}} \tag{14}$$

The voltage gain is also determined by the quality factor, Q, which is defined as the ratio between the characteristic impedance and effective load resistance,

$$Q = \frac{\sqrt{L_r / C_r}}{R_{eff}} \tag{15}$$

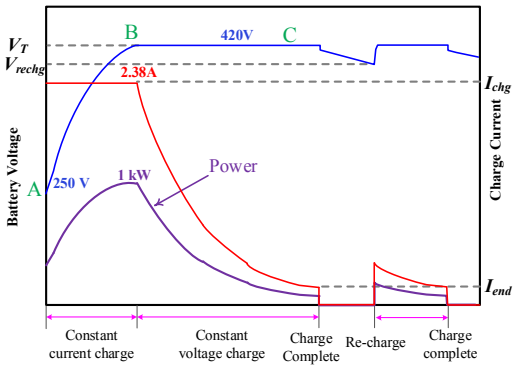

Fig. 11. 1kW charging profile of a 250V-420V battery pack.

Detailed selection of Q can be found in [18]. The basic idea is to make sure that the voltage gain curve at f_r has a sharp slope, such that the f_s has a narrow range and close to the resonant frequency. The gain fluctuation range corresponds to the fluctuation on the DC link input voltage. This fluctuation origins from the grid and the PFC rectification stage. After selecting Q and f_s, the L_r and C_r could be calculated.

Generally, large L_m means reduced circulating current and conduction losses. However, large L_m could results in ZVS loss in the MOSFETs. L_m can be selected by its largest possible value which still guarantees ZVS of the lagging leg MOSFETs.

C. Semiconductor devices selection

MOSFETs S_1-S_4 must have their voltage stress equal to V_{DC}. Typically, a 20% margin should be reserved. Thus, the voltage rating of MOSFETs can be calculated. The current stress of the MOSFETs can be calculated based on the expression of i_{L1} at the rated power of PSFB. It should be noted that at the PSFB rated power, the LLC topology is not activated.

Regarding to power diodes, D_1-D_4 have their voltage stress equal to $V_{bat,h} + V_{Ca}$, D_{a1} and D_{a2} have their voltage stress equal to $V_{bat,h}$, while D_5 and D_6 have their voltage stress equal to $2V_{bat,l}$. Typically, a 20% margin should be reserved. The current stress of the diodes can be calculated based on the expression of secondary side currents at the rated power, which can be derived based on the circuit analysis in Section III.

V. RESULTS

The specifications and design parameters of the proposed integrated charger are summarized in Table I.

Fig. 11 shows the 1kW charging profile of a PEV onboard battery pack. The charging is classified into constant current charging and constant voltage charging. While in the transition between those two charging modes, the charging power reaches its maximum value. Three important operating points (A, B, C) are marked in Fig 11.

Based on the circuit parameters shown in Table I. The normalized voltage gain of LLC converter versus f_s under different load conditions is plotted in Fig. 12. As shown, within the specified dc link voltage range (390V ± 10V), f_s can always be constrained in a narrow range close to f_r.

TABLE I

SPECIFICATIONS AND DESIGNED PARAMETERS OF THE PROPOSED CHARGER

Symbol	Parameter	Symbol	Parameter
V_{DC}	390V±10V	L_r	35 µH
$V_{bat,h}$	250V-420V	C_r	18 nF
$P_{PSFB,max}$	1 kW	L_m	100 µH
$V_{bat,l}$	14 V	n_2:1:1	40:3:3
f_s	200 kHz	n_1:1	12:20
$P_{LLC,max}$	300 W	L_1	40 µH
Co	100 µF	L_f	560 µH
C_f	20 µF	C_a	1 µF

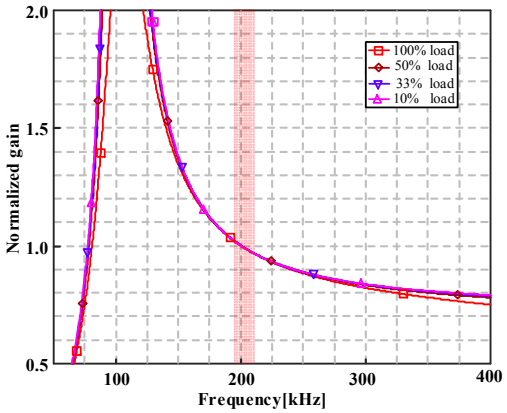

Fig. 12. Normalized gain versus the frequency for the selected design parameters.

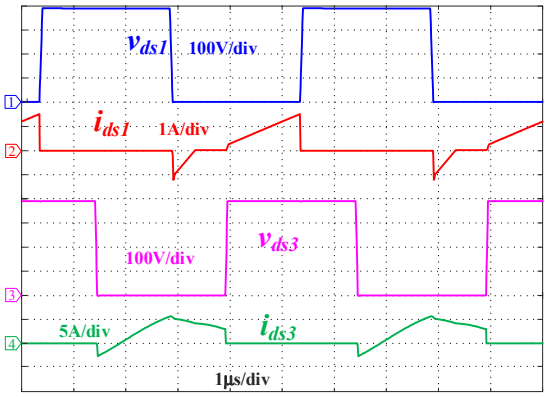

Fig. 13. PSFB circuit waveforms at V_{bat} = 420V, I_{bat} = 0.48A, LLC

Simulation is conducted based on the parameters provided in Table I. MOSFET C_{oss} is set to be 150 pF. Simulation data is presented in figures 13-15. Fig. 13 demonstrates the circuit operation at PSFB light load condition, where the charging power for the high voltage battery is 200W (point C in Fig. 11). At this operating point, the LLC converter is reconfigured and activated. As shown, V_{ds3} drops to zero before the conduction of MOSFET. Therefore, ZVS is achieved on the lagging leg.

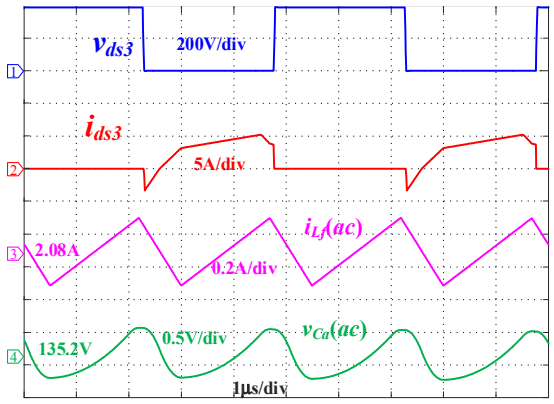

Fig. 14. PSFB circuit waveforms at V_{bat} = 420 V, I_{bat} = 2.38A, LLC not activated.

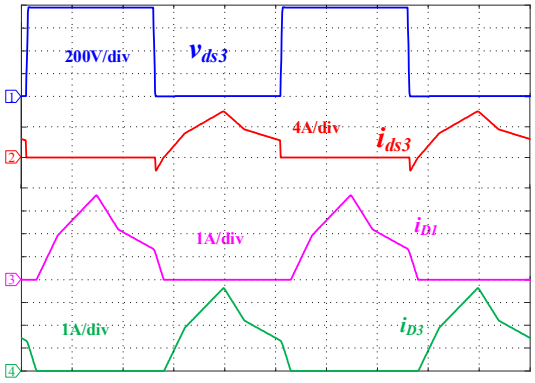

Fig. 15. PSFB circuit waveforms at V_{bat} = 250 V, I_{bat} = 2.38A, LLC not activated.

Fig. 14 shows the circuit operation at the PSFB full load condition, where the charging power for the high voltage battery is 1 kW (point B in Fig. 11). At this operating point, the LLC converter is in idle mode. As can be observed on the curve of i_{ds3} and v_{ds3} The PSFB can achieve ZVS on the lagging leg by itself. Ac coupled filter inductor current (i_{Lf}) and ac coupled auxiliary capacitor voltage (v_{Ca}) waveforms are also captured. i_{Lf} ripple is 0.42A with its dc offset as 2.08A. v_{Ca} ripple is 0.8V with its dc offset as 135.2 V. The ripple voltage is much smaller than its dc offset.

Fig. 15 shows the circuit operation at the beginning of constant current charging mode, where the battery voltage is 250V and the charging power is 595W (point A in Fig. 11). At this operating point, the LLC converter is also in idle mode. The PSFB achieve ZVS on the lagging leg without the assistance of LLC converter. i_{D1} and i_{D3} are captured. The waveforms shows that duty cycle loss is successfully eliminated.

VI. CONCLUSIONS

In this paper, a self-reconfigured PEV onboard charging architecture is proposed. The proposed architecture adopts an auxiliary circuit on the secondary side of the PSFB converter, which help to eliminate the duty cycle loss problem. Moreover, at light charging mode, a half bridge LLC topology is reconfigured to be connected to the DC link. This help the

PSFB converter to realize ZVS on the lagging leg. The proposed converter demonstrates the benefits of a) optimized LLC switching frequency; a) full ZVS range of the lagging leg; b) zero duty cycle loss and reduced circulating currents; c) relative low circuit components count due to the topology reuse; and d) reduced secondary side diode turning off losses. Circuit analysis and design considerations are both conducted in detail. A 1 kW charging prototype is designed and simulated to verify the proof of concept. Future work will be focused on the hardware implementation of this designed charger.

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