An Integrated Three-port DC/DC Converter for High-Voltage Bus Based Photovoltaic Systems

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***Abstract*—In high-voltage bus based photovoltaic systems, a power electronic interface is required to manage the power flow in between the PV panel, battery, and the high-voltage dc bus. In this paper, a novel three-port dc/dc topology is proposed for this application. Pulse width and phase shift offer two degrees of freedom to effectively regulate the power flows. On the primary side, the input current ripple is reduced due to the interleaved structure. This avoids the usage of the bulky electrolytic capacitor on the PV terminal. On the secondary side, a voltage sixfolder rectifier is employed to boost the step-up ratio. This reduces the turns number on the secondary-side of the transformer. Moreover, the voltage stresses of secondary-side MOSFETs and diodes are reduced to one-third of the output voltage. Zero-voltage switching and zero-current switching are realized among all power MOSFETs and diodes respectively and in an extended range. A 500 W converter prototype, linking a 40 V-60 V battery pack, a 20 V- 30 V PV panel, and a 760 V dc bus, is designed and tested to verify the proof-of-concept. Both the circuit functionality and theoretical analysis are validated by the experimental results.**

***Index Terms*—high-voltage bus, phase-shift modulation (PSM), pulse-width modulation (PWM), three-port converter, zero-voltage switching (ZVS).**

I. Introduction

In photovoltaic (PV) based microgrid systems, high-voltage (760 V) dc bus with half-bridge micro-inverter is considered as an attractive solution [1]. This is because the half-bridge structure is featured with reduced components count, enhanced power density, and improved reliability [2]. Besides, due to the power mismatch between the PV generator and the load, a battery pack is required to serve as the energy buffer. Therefore, in the front stage, a three-port converter (TPC) is necessary to manage the power flow in between the PV panel, battery pack, and the high-voltage bus. The diagram of such a microgrid system is illustrated in Fig. 1.

To realize the TPC, the conventional method is to use multiple discrete converters [3], [4]. This jeopardizes the power density and conversion efficiency. Moreover, different control strategies such as maximum power point tracking (MPPT), battery charging/discharging and load regulation need to be addressed separately.

To improve, the concept of integrated TPC has been proposed. Integrated solution is featured with: 1) reused circuit components, 2) reduced power conversion stages, and 3) centralized control strategy. Due to those advantages, integrated TPC topologies and the corresponding control strategies have attracted wide research attention in recent years.

Integrated TPC topologies can be classified into three

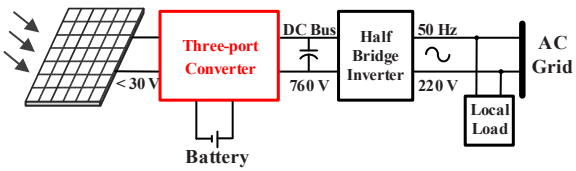


Fig. 1. The structure of three-port 760V dc bus based PV microgrid.

categories: non-isolated TPCs, three-port isolated TPCs, and two-port isolated TPCs. By integrating coupled inductors into Boost or Buck-Boost topologies, multiple non-isolated TPCs are derived in [5]–[8]. The high voltage gain with moderate duty cycle can be achieved. However, non-isolated TPC is usually not considered due to the galvanic isolation requirement in high-voltage bus applications.

Alternatively, some three-port isolated TPCs are proposed in [9]–[12]. Those converters are usually based on half-bridge, boost-half-bridge or full-bridge structures. A three-winding transformer is employed to realize multi-directional power flow. The transformer turns ratio can be easily customized to accommodate different voltage levels. However, the switch count is large, which leads to increased manufacturing cost and conduction loss. Furthermore, the design of the magnetic component is complicated.

Compared with three-port isolated solution, two-port isolated TPC is more attractive. It offers galvanic isolation between the high and low voltage sides, and can easily accommodate different voltage levels. Furthermore, it is featured with reduced switch count and simpler transformer design. By integrating the boost converter into the phase-shift-full-bridge (PSFB) converter, a group of ZVS TPCs is proposed in [13]–[15]. However, there are some intrinsic disadvantages inherited from PSFB topology [16]: 1) high conduction loss in the freewheeling stage, 2) constrained ZVS range on the primary side MOSFETs, 3) duty cycle loss due to the existance of output filter inductor, and 4) voltage spike and reverse recovery issues on the rectification diodes due to the clamping effect of the output capacitor. Furthermore, the current ripple on the PV panel is large. Large current ripple is harmful for the PV panel lifetime. In [17], interleaving technique is introduced to the primary side and helps to reduce the current ripple. However, in discontinuous conduction mode (DCM), the current stress and conduction loss are large, and a Boost integrated with ZVS LLC topology is proposed in [18]. It adopts pulse-width and pulse-frequency hybrid regulation scheme and this control scheme is difficult to implement.

It is worthy mentioning that most of the state-of-the-art two-

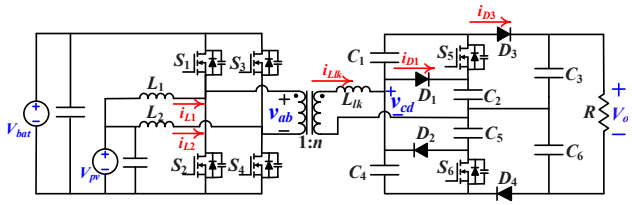


Fig. 2. Schematic of the proposed three-port topology.

port isolated TPCs adopt half/full bridge rectification stage on the output side. Therefore, to realize a high step-up ratio, a transformer with large secondary-side turns number is required. This degrades the system power density. In addition, the voltage stresses of the secondary-side switches equal the output voltage or twice of the output voltage. This brings challenges to the optimal selection of semiconductors in high-voltage applications.

In [19], [20], the voltage quardrupler rectifier is adopted in high-voltage bus based PV systems. This rectifier owns the benefits of moderate secondary-side turns number and low voltage stresses on the high-voltage side. However, the current ripples of the PV panel are large. In addition, the voltage regulation is based on singular pulse-frequency or phase-shift modulation. Thus, it is infeasible to deploy those topologies into the three-port applications.

In this paper, a novel two-port isolated integrated TPC is proposed. The proposed topology is derived from interleaved Boost topology and active voltage sixfolder rectifier. The phase shift on the active rectifier brings another modulation scheme, which accommodates the control of three-port power flows. This makes it a good candidate for high-voltage bus based PV systems. In comparison with the prior arts, it demonstrates following advantages:1) PV panel current ripple is reduced remarkably; 2) ZVS and ZCS ranges are effectively extended; 3) a high step-up ratio is realized with a moderate transformer secondary-side turns number; 4) the voltage stresses on the secondary-side semiconductors are reduced.

II. Operation Principles

A. Topology Description

Fig. 2 shows the schematic of the proposed TPC. The primary-side circuit is the parallel of two synchronized rectified boost units, including two inductors (L_1 and L_2) and four power MOSFETs S_1-S_4. The driving signals for S_1 and S_2 (S_3 and S_4) are complementary with certain deadband. The two parallel phase legs are driven in an interleaved manner with 180° phase shift. The duty cycle of S_1's gate signal is defined as D. The power flow between the PV panel and the battery can be regulated by D. The transformer turns ratios is defined as 1:n. On the secondary side, S_5 and S_6 are driven complementarily with fixed 0.5 duty cycle. Certain phase shift (β) between the switch patterns of S_1 and S_6 is enforced to regulate the power delivered to the load. The phase shift ratio is defined as $D_{ph} = \beta/\pi$.

Based on the range of D and β, the steady-state operation can be classified into four states. The operation state with $D < 0.5$ and $\beta > 0$ is adopted in this work. This main sate is discussed and analyzed in detail.

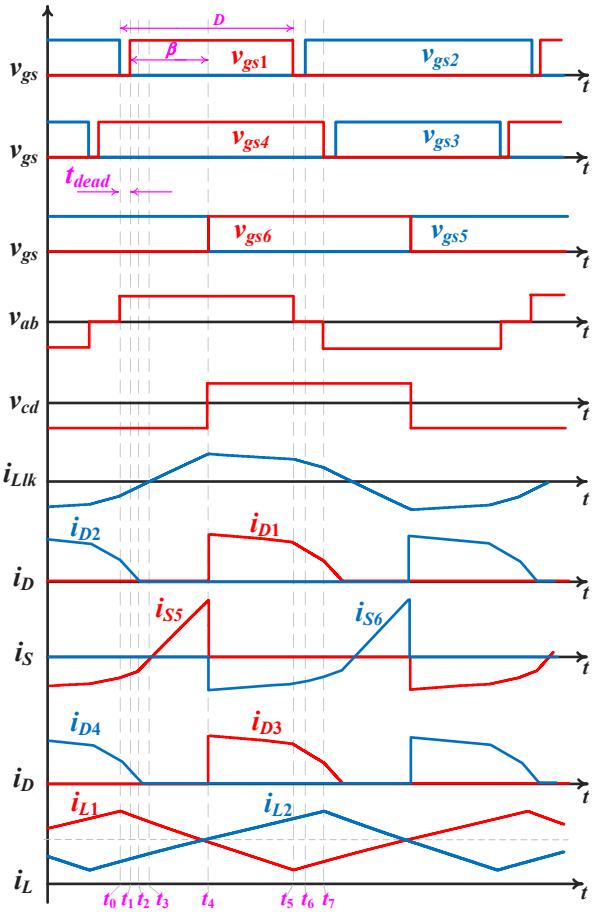


Fig. 3. Converter steady state waveforms.

In this state, there are 14 operation modes in one switching period. Considering the circuit symmetry, only 7 operation modes in a half switching period are presented.

L_1 and L_2 are sufficiently large to keep the i_{L1} and i_{L2} is continuous. The secondary-side capacitances are sufficiently large with ignorable voltage ripple. According to the principles of the secondary-side rectifiers, the relationship between the amplitudes of V_{cd} and V_o can be expressed as,

$$V_{cd} = V_o/6 \tag{1}$$

The key waveforms are plotted in Fig. 3 and the corresponding equivalent circuits are presented in Fig. 4.

Mode I: [t_0, t_1). Before t_0, $S_{2,4,5}$ are ON and the secondary-side diodes $D_{2,4}$ conduct. The inductor current $i_{Llk} < 0$. L_1 and L_2 are energized by the PV panel. At t_0, S_2 is turned off. i_{Llk} flows from the source to drain of S_1. L_1 release power to the battery and while L_2 continues to be energized. During the deadband, the negative current discharges the output capacitor (C_{oss}) of $S_{1,2}$.

Mode II: [t_1, t_2). At t_1, S_1 is turned on with ZVS naturally. At the end of this mode, D_2 and D_4 are turned off naturally without reverse-recovery losses. i_{Llk} begins to only flow through S_5 and continues to decrease.

Mode III: [t_2, t_3). During this mode, C_1 is charged while C_2

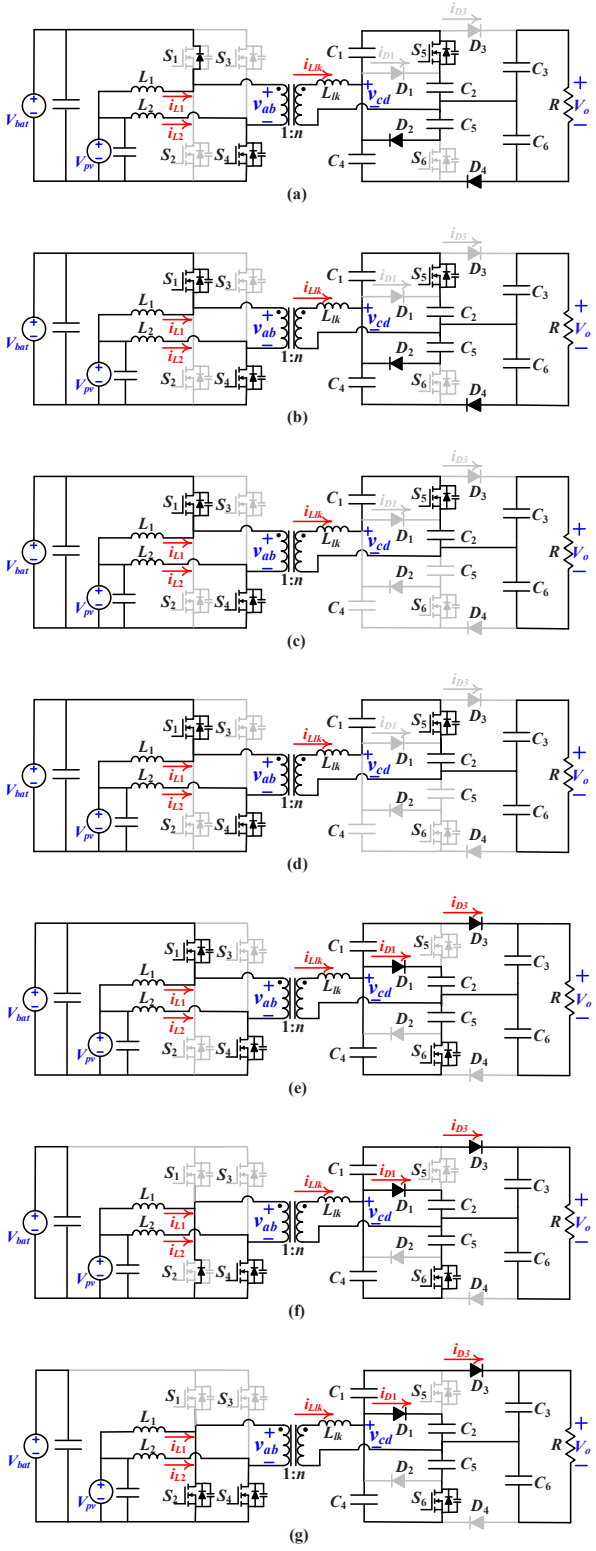


Fig. 4. Converter equivalent circuits. (a) Mode I, $t_0 \leqslant t < t_1$. (b) Mode II, $t_1 \leqslant t < t_2$. (c) Mode III, $t_2 \leqslant t < t_3$. (d) Mode IV, $t_3 \leqslant t < t_4$. (e) Mode V, $t_4 \leqslant t < t_5$. (f) Mode VI, $t_5 \leqslant t < t_6$. (g) Mode VII, $t_6 \leqslant t < t_7$.

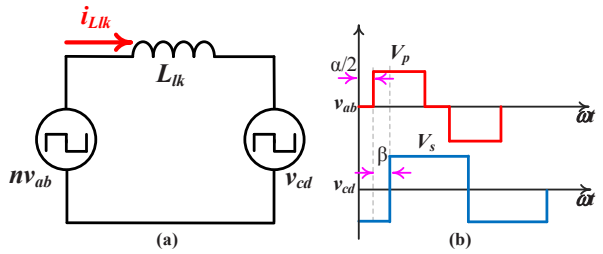


Fig. 5. The model of the proposed converter. (a) the equivalent circuit, (b) voltage waveforms.

is discharged. L_{lk} continues to release power. Mode III ends when i_{Llk} crosses zero.

Mode IV: [t_3, t_4). At t_3, i_{Llk} becomes positive and increases linearly. i_{S5} becomes positive. This means i_{S5} only flows S_5' channel. At t_4, S_5 is turned off; the body diode of S_6, D_2, and D_4 begin to conduct.

Mode V: [t_4, t_5). During this mode, i_{S6} is still negative. This means the ZVS for the secondary-side MOSFETs occurs naturally without any deadband. i_{Llk} decreases linearly. At the end of this mode, S_1 is turned off.

Mode VI: [t_5, t_6). This mode is similar to Mode I. During this short interval, C_{oss} of S_2 is discharged to zero. This creates a ZVS condition for S_2. At t_5, L_1 is energized by the PV panel.

Mode VII: [t_6, t_7). At t_6, S_2' channel conducts with zero voltage. At the end of this mode, S_4 is turned off and the body diode of S_3 conducts.

III. Circuit Modeling and Analysis

A. Circuit Modeling and Output Power Analysis

The proposed topology can be simplified into an equivalent circuit, as shown in Fig. 5 (a). The typical waveforms of v_{ab} and v_{cd} are demonstrated in Fig. 5 (b).

According to the Fourier analysis, v_{ab} and v_{cd} can be expressed as,

$$\begin{aligned} v_{ab} &= \sum_{i=1,3,5,\ldots} \frac{4V_{bat}}{i\pi}\cos\left(i\frac{\alpha}{2}\right)\sin(i\omega_0 t) \\ v_{cd} &= \sum_{i=1,3,5,\ldots} \frac{2V_o}{3i\pi}\sin\left[i(\omega_0 t-\beta-\alpha/2)\right] \end{aligned} \tag{2}$$

Where

$$\alpha = \begin{cases} 2(0.5-D)\pi, & (D<0.5) \\ 2(D-0.5)\pi, & (D>0.5) \end{cases} \tag{3}$$

The output power with $D < 0.5$ can be derived as,

$$P_o = \sum_{i=1,3,5,\ldots} P_{B,i}\cos\left[i(0.5-D)\pi\right]\sin\left\{i\left[\beta+(0.5-D)\pi\right]\right\} \tag{4}$$

where $\beta + (0.5 - D)\pi < \pi$, and $P_{B,i}$ is the normalized power.

$$P_{B,i} = \frac{4nV_O V_{bat}}{3i^3\pi^3 f_0 L_{lk}} \tag{5}$$

In order to simplify the analysis, only the fundamental component is considered. The corresponding result is plotted in

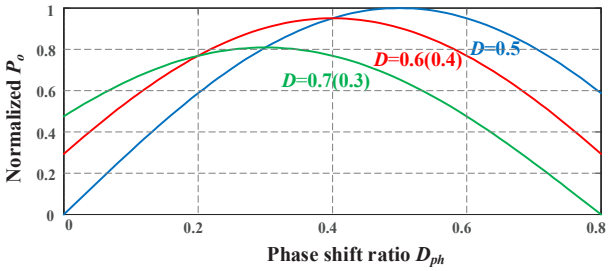


Fig. 6. Curves of output power varied versus phase shift ratio under different duty cycles.

Fig. 6. As indicated, the output power curve is symmetrical to $D = 0.5$; β and $2D\pi - \beta$ correspond to the same P_o. Thus, there are two symmetric phase-shift regulation ranges [0, $D\pi$) and [$D\pi$, $D\pi + 0.5\pi$). In [0, $D\pi$), P_o increases with the increase of phase shift angle. While in [$D\pi$, $D\pi + 0.5\pi$), P_o decreases with the increase of phase shift angle.

B. Voltage Gain

The primary side is essentially an interleaved boost converter. Thus, the relationship between V_{pv} and V_{bat} is derived as,

$$V_{bat} = \frac{V_{pv}}{D} \tag{6}$$

When the gate signals of the secondary-side MOSFETs are removed, the MOFSETs functions as diodes. The corresponding β equals zero and the secondary side becomes a voltage multiplier. Thus,

$$V_o = 6nV_{bat} \tag{7}$$

The corresponding voltage gain is,

$$G' = V_o / V_{PV} = \frac{6n}{D} \tag{8}$$

The gain curves versus D'=1-D with different transformer turns ratios are plotted in Fig. 7. A high voltage gain is achieved in passive voltage multiplier converter, even when the transformer turns ratio and the duty cycle are moderate. Furthermore, when the gates signals of the secondary-side MOSFETs are enabled, the phase shift control works. Due to the addition of a control freedom, the voltage gain regulation range is changed from a single curve to two-dimensional region. Compared with passive voltage multiplier converter, the regulation flexibility of voltage gain is enhanced. Therefore, a high step-up ratio can be achieved in the proposed topologies.

C. Soft Switching

1) Secondary-side Switches

To ensure ZVS, C_{oss} of MOSFET should be fully discharged before the channel conducts. As shown in Fig. 3, a negative current exists before the gate signal is applied. This indicates a clear ZVS. Meanwhile, the secondary-side diodes' turn-off di/dt is constrained by L_{lk}. This indicates a robust ZCS turn-off of the diodes. Hence, the reverse recovery issues can be effectively mitigated.

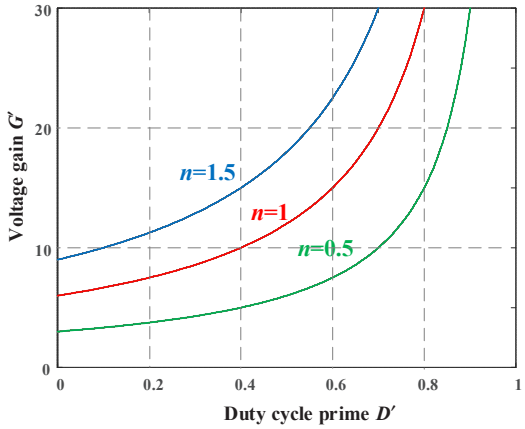


Fig. 7. Curves of voltage gain varied versus D' under different turns ratios.

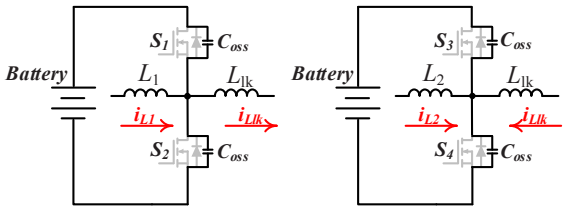


Fig. 8. ZVS conditions for primary-side switches.

2) Primary-side MOSFETs

As demonstrated in Fig. 8, the ZVS condition of the primary-side MOSFETs can be expressed as,

$$\begin{cases} S_1 : i_{L1}(t_{S1}) - ni_{Llk}(t_{S1}) > I_{\min} \\ S_2 : i_{L1}(t_{S2}) - ni_{Llk}(t_{S2}) < -I_{\min} \\ S_3 : i_{L2}(t_{S3}) + ni_{Llk}(t_{S3}) > I_{\min} \\ S_4 : i_{L2}(t_{S4}) + ni_{Llk}(t_{S4}) < -I_{\min} \end{cases} \tag{9}$$

where t_{s1}~ t_{s4} are the turn-on time of S_1~ S_4, respectively. In the energy storage perspective, the minimum current to charge and discharge C_{oss} of two complementary MOSFETs is defined as,

$$I_{\min} = \sqrt{\frac{2 \cdot C_{oss} \cdot V_{bat}^{\ 2}}{L_{lk}}} \tag{10}$$

According to the basic principles of boost converter, i_{L1} and i_{L2} are derived as,

$$\begin{cases} i_{L1}(t_{S1}) = i_{L2}(t_{S3}) = \dfrac{P_{pv}}{2V_{pv}} + \dfrac{V_{PV}}{2L}(1-D)T_S \geq 0 \\ i_{L1}(t_{S2}) = i_{L2}(t_{S4}) = \dfrac{P_{pv}}{2V_{pv}} - \dfrac{V_{PV}}{2L}(1-D)T_S \geq 0 \end{cases} \tag{11}$$

According to the steady-state analysis of the primary-side circuit, i_{Lk} is expressed as

$$\begin{cases} i_{Llk}(t_{S1}) = -i_{Llk}(t_{S3}) = i_{Llk}(t_0) < 0 \\ i_{Llk}(t_{S2}) = -i_{Llk}(t_{S4}) = i_{Llk}(t_6) > 0 \end{cases} \tag{12}$$

It should be noted that the ZVS conditions for S_1 and S_3 (S_2 and S_4) are the same. According to Eq. (9-12) and Fig. 8, the

TABLE I
COMPARISON OF COMPONENT VOLTAGE STRESSES

Secondary-side Rectifier	MOSFETS & diodes	Capacitors
Half-wave rectifier	$2V_o$	V_o
Full-wave rectifier	$2V_o$	V_o
Full-bridge rectifier	V_o	V_o
Voltage quadrupler rectifier	$V_o/2$	$V_o/2$, $V_o/4$
This work	$V_o/3$	$V_o/2$,$V_o/4$,$V_o/6$

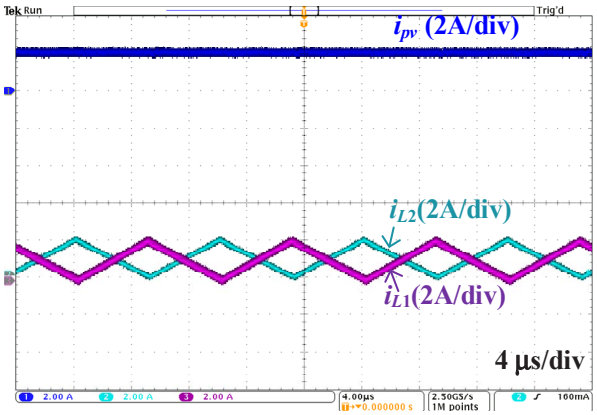


Fig. 9. The steady state current waveforms of the primary side.

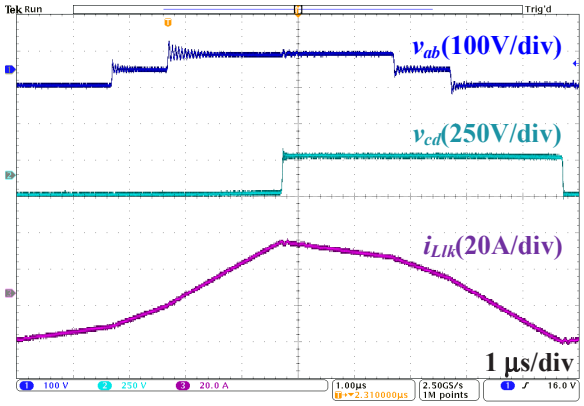
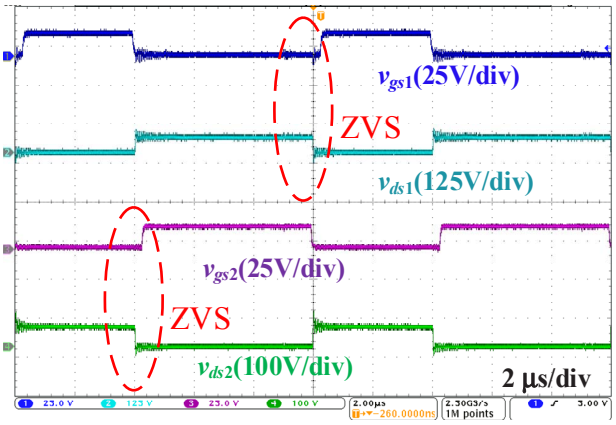


Fig. 10. The steady-state key waveforms.

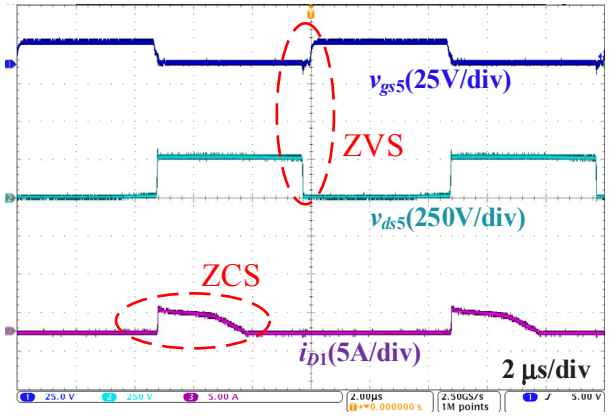
ZVS condition for the proposed converter is rather different from the traditional PSFB converter. This is mainly due to the existence of L_1 and L_2. L_1 and L_2 extend the ZVS range of the upper switches (S_1 and S_3), while narrows the ZVS range of the lower switches (S_2 and S_4). Therefore, ZVS of the lower switches is more important.

D. Voltage Stress

The voltage ratings of the secondary-side switches and capacitors need to be analyzed to facilitate the selection of components. In the proposed converter, their voltage stresses are summarized and compared with the conventional structures in Table I. As shown, the voltage stresses of the secondary-side switches and capacitors are much smaller than the conventional



(a)



(b)

Fig. 11. Soft-switching waveforms. (a) MOSFETs $S_{1,2}$. (b) MOSFET S_5 and Diode D_1.

structures. This makes the proposed converter more suitable for high-voltage applications.

IV. EXPERIMENTAL RESULTS

To verify the effectiveness of the proposed converter, a 500W converter prototype is designed. The key parameters are as follows. V_{pv} = 20 V-30 V, V_{bat} = 40 V-60 V, V_o = 760 V, transformer's turns ratio n = 2, L_{lk} = 30 µH, L_1= L_2 = 25 µH and the switching frequency f_s = 100 kHz. Fig. 9 shows the experimental steady-state waveforms of the inductor currents on the primary side. As demonstrated, the current ripple on the PV terminal is significantly reduced. The steady-state key waveforms are captured in Fig. 10. The experimental results agree with the analysis.

The switching waveforms of the proposed converter are captured in Fig. 11. As shown in Fig. 11(a), there is no overlap between the rising edge of v_{gs} and falling edge of v_{ds}. This validates the ZVS of the primary side MOSFETs $S_{1,2}$. Similarly, Fig. 11(b) proofs that ZVS is realized on the secondary-side MOSFETs S_5 and the diode D_1 is turned off with low di/dt without any reverse recovery. The soft-switching results agree with previous analysis.

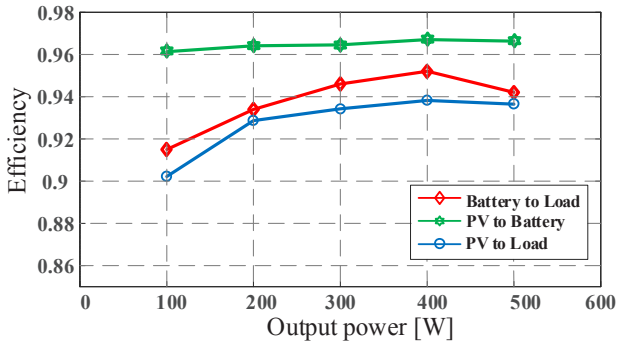


Fig. 12. Measured efficiency versus the output power.

The conversion efficiency is evaluated in three different power transfer paths (PV to battery, battery to load, and PV to load). The results are shown in Fig. 12. The efficiency data is calibrated with a high-precision power analyzer (PPA4530 from Newtons4th Ltd). As shown, in PV to battery path, the measured peak efficiency is 97%. In battery to load path, the measured peak efficiency is 95%. In PV to load, the measured peak efficiency is 94%.

V. Conclusion

This paper proposes a novel integrated high step-up three-port dc/dc converter for PV based microgrid systems. The proposed topology is regulated by primary-side pulse-width and secondary-side phase-shift. It is featured with high integration and high power density. Extended ZVS and ZCS can be achieved for all MOSFETs and diodes, respectively. This results in low switching loss and high efficiency. Due to the voltage sixfoler rectifier structure, the voltage stresses of the secondary-side components are remarkably reduced. In comparison with prior arts, the current ripple of the PV panel is reduced due to the interleaving structure. Those features make the proposed topology a good candidate for high-voltage bus based PV systems. Topology features, operational principles, and circuit characteristics are analyzed in detail in this paper. A 500 W converter prototype is designed and demonstrates good efficiency performance. The circuit analyses are validated in the experimental results. Robust dynamic performance validates the control scheme and regulating strategy.

Acknowledgment

This work was supported in part by the National Natural Science Foundation of China under Grant 51607113, and in part by the Shanghai Sailing Program under Grant 16YF1407600.

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