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A Hierarchical ZVS Battery Equalizer Based on Bipolar CCM Buck-Boost Units

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***Abstract*—Conventional battery equalizers rely on unipolar continuous-conduction mode of power electronic converters. This causes substantial energy losses during the switching transitions. To cope with this issue, this paper proposes a novel hierarchical battery equalizer based on bipolar continuous-conduction mode buck-boost units. In the proposed structure, the inductor current is controlled to enter into the negative region at the end of each switching period. Thus, the body diode of power MOSFET provides a freewheeling path for the inductor current during the dead band. This ensures zero-voltage switching of both power MOSFETs. Therefore, the switching losses are significantly reduced. Meanwhile, the integral of the inductor negative current is precisely controlled to minimize the circulating current. This guarantees both minimized conduction losses and suitable equalization speed. The operation principle and control strategy of the equalizer are analyzed. The comparison of equalization speed between different equalizer is presented. An experimental prototype to balance four series-connected Lithium-ion battery cells is implemented. Both simulation and experimental results validate the functionality and analysis of this battery equalizer.**

Keywords—battery equalizer, bipolar continuous-conduction mode (CCM), buck-boost converter, Lithium-ion battery, zero-voltage switching (ZVS).

I. INTRODUCTION

In high power applications such as electric vehicles, the Lithium-ion batteries must be connected in series to boost the power capability [1]-[3]. Due to the manufacturing and environmental variances, the internal impedance of each battery cell in the battery string may vary. This causes the mismatch of cell voltages when the battery string is charged or discharged [4]-[6]. Thus, certain cells may be overcharged or depleted, which leads to the decay of battery capacity and lifetime, and even incurs safety issues (e.g. fire or explosion) [7]-[10]. Therefore, battery equalizers are required to effectively mitigate cell mismatch issues, and to improve the system performance.

Different battery equalization techniques have been reported in the literature. Those techniques can be divided into passive methods and active methods. The passive methods usually have a resistor paralleled with each battery cell. The resistor consumes the excessive energy of the overcharged battery cells [1]. These methods are easy to implement and are featured with low cost and small size. However, the power dissipation is large which degrades the efficiency and causes thermal issues to the battery management system.

In comparison with the passive methods, the active methods are preferable due to their advantages of high efficiency and fast equalizing speed. In [4], the switched-capacitor based equalizer is proposed. This technique provides a direct equalization path between two arbitrary cells. However, the equalization speed decays when the battery cell voltage difference is trivial. The reference [6] uses a bidirectional Fly-back converter to transfer the energy of the overcharged battery cells to the battery string. While a complicated control algorithm is required to ensure robust system performance. Some transformer based equalizers are proposed in [7]-[9]. The technique proposed in [7] is based on a multi-secondary windings transformer. This method achieves relatively fast equalization speed, but it is impractical to design the transformer when the cell number scales up.

In order to improve the equalization speed, the hierarchical equalization architecture is proposed in [11]-[14]. In [12], a hierarchical equalization architecture based on buck-boost units is proposed. However, the equalization unit operates at unipolar CCM, substantial switching loss occurs during the switching transitions. This jeopardizes the system efficiency, especially in high-frequency scenarios. Moreover, all equalizer units operate simultaneously, while the

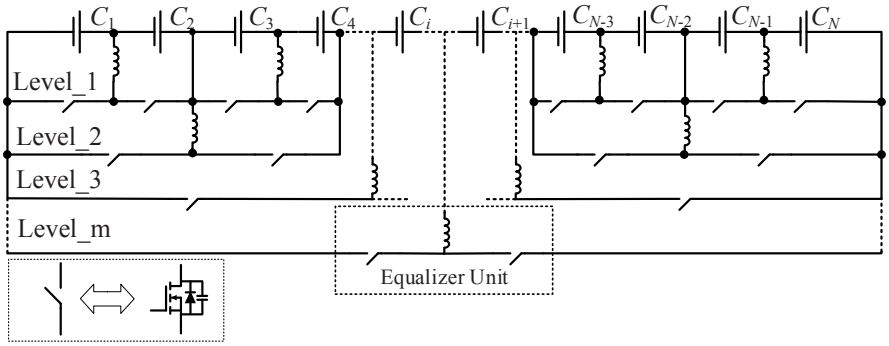

Fig. 1 The hierarchical equalizer schematic based on buck-boost converter.

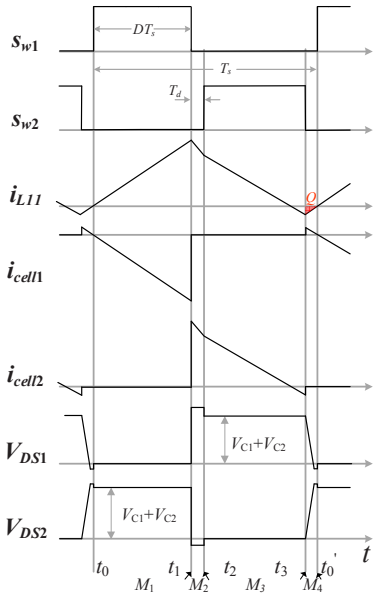

Fig. 2 The key waveforms of the basic equalization unit.

optimization between different levels is not addressed. This is not preferred as it may cause the overcharged cells even further charged at the beginning of the equalization process.

To boost the conversion efficiency and to optimize the equalization strategy, the paper presents a hierarchical battery voltage equalizer based on buck-boost units operating at bipolar CCM. The schematic of the proposed equalizer with N series-connected cells is plotted in Fig. 1. As shown, each unit is configured by a modified buck-boost circuit. Different units are placed at different levels to provide flexible balancing paths for corresponding cells or strings. The equalizer can realize bidirectional energy flow. Furthermore, all the power MOSFETs are turned on with zero voltage. This reduces the switching losses remarkably. An advanced control strategy is introduced to optimize both the conversion efficiency and the equalization speed.

II. Operation Principles

The proposed equalizer can transfer energy between two adjacent battery cells or strings via the basic units located at different levels. In order to simplify the analysis, we focus on one basic equalization unit to interpret the operation modes. The key waveforms of the basic equalization unit at steady state are shown in Fig. 2. Some assumptions are made as follows,

1. The voltage of $Cell_1$ is higher than $Cell_2$ ($V_{C1} > V_{C2}$);
2. The voltage of the cell can be seen as a constant during a specific switching period;
3. The forward voltage drops of body diodes of MOSFETs are considered, while the equivalent series resistance (ESR) is ignored;
4. All the equalization units (modified buck-boost converter) operate in bipolar CCM.

S_{w1} and S_{w2} turn on and off complementarily following the buck-boost switching pattern. The operation of the equalization unit can be divided into four modes.

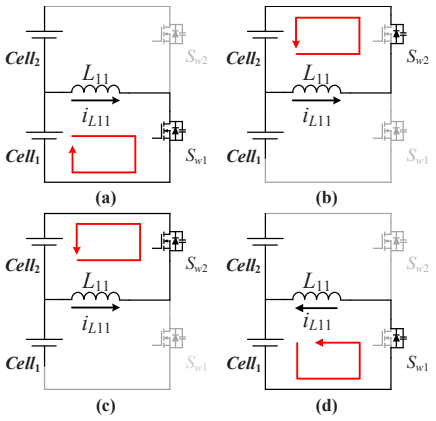

Fig. 3 The equivalent circuit of four modes. (a) Mode 1; (b) Mode 2; (c) Mode 3; (d) Mode 4.

Mode 1 [t_0-t_1): The equivalent circuit of mode 1 is shown in Fig. 3 (a). When S_{w1} turns on, Mode 1 starts. In Mode 1, the voltage of $Cell_1$ (V_{C1}) is applied to the inductor (L_{11}), and the inductor current (i_{L11}) builds up. i_{L11} is equal to the equalization current in this sub-interval. Since the cell voltage can be seen as a constant, the inductor current increases linearly. The discharge current of the $Cell_1$ also increases linearly. Thus, the excessive energy of the $Cell_1$ is transferred to L_{11}.

Mode 2[t_1-t_2): The equivalent circuit of mode 2 is shown in Fig. 3 (b). When S_{w1} turns off, Mode 2 starts. Since i_{L11} could not change abruptly, the body diode of S_{w2} provides a freewheeling path. Therefore, the body diode conducts before the conduction of MOSFET channel, which establishes the zero voltage turning-on condition for S_{w2}. In this mode, the inductor is paralleled with $Cell_2$ via S_{w2}. Thus, the polarity of the inductor voltage is inverted and i_{L11} decreases linearly.

Mode 3[t_2-t_3): The equivalent circuit of mode 3 is shown in Fig. 3 (c). When S_{w2} turns on, Mode 3 starts. i_{L11} continues to decrease linearly. Thus, the stored energy in the inductor is transferred to the target cell ($Cell_2$). The charge current of $Cell_2$ also decreases simultaneously. Consequently, the drain-source voltage of S_{w1} (v_{ds1}) is clamped to the sum of the cell voltages.

Mode 4[t_3-t_0'): The equivalent circuit of mode 4 is shown in Fig. 3 (d). When S_{w2} turns off , Mode 4 starts.

The voltage stresses of the switches are derived as,

$$v_{ds1} = V_{C1} + V_{C2} + V_D,\ v_{ds2} = V_{C1} + V_{C2} + V_D \qquad (1)$$

During Modes 2 and 3, the analytical expression of the inductor current is derived as,

$$i_{L11}(t) = \frac{V_{C1}}{L_{11}} DT_s - \frac{V_{C2} + V_D}{L_{11}}(T_d) - \frac{V_{C2}}{L_{11}}(t - t_2) \qquad (2)$$

III. Design Considerations

A. The Condition of Bipolar CCM

In order to achieve high conversion efficiency, the equalizer is designed to operate at the bipolar CCM and all the power MOSFETs are turned on at zero voltage. Therefore, during Mode 3, the inductor current must be slightly negative after S_{w2} turns off to ensure both the ZVS of S_{w1} and the bipolar

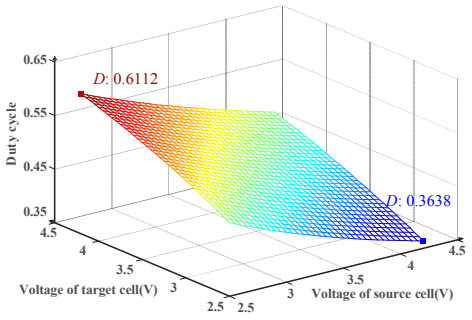

Fig. 4 The variation scope of duty cycle.

CCM operation. Moreover, the dead band of Mode 2 should be large enough to secure the ZVS of S_{w2}. Hence, based on Eq. (2), the condition of bipolar CCM can be derived as,

$$D \le \frac{(1-A_{T_d})V_{C2} + A_{T_d}V_D}{V_{C1}+V_{C2}}, \quad A_{T_d} = \frac{T_d}{T_s} \tag{3}$$

where A_{Td} is the ratio between the dead band and the switching period.

The boundary condition defined by Eq. (3) is plotted in Fig 4. Practically, the open-circuit terminal voltage of the Lithium-Ion battery cell varies between 2.5 V and 4.2 V. With this voltage range and according to Eq. (3), the maximum value of duty cycle varies between 0.36 and 0.61, as shown in Fig. 4.

In order to ensure both bipolar CCM and ZVS, the accurate design of duty cycle and the dead band should be considered. This requires minimized circulating current during the commutation in Mode 4. Moreover, i_{L11} discharges and charges the output capacitors of S_{w1} and S_{w2} in Mode 4, respectively. The corresponding voltages of the output capacitors of S_{w1} and S_{w2} are discharged and charged to V_D and $V_{C1}+V_{C2}+V_D$, respectively. Thus, the voltage variations (ΔV) of the two capacitors are equal to $V_{C1}+V_{C2}$. The charge transferred between the two capacitors during this period is expressed as,

$$Q = \Delta V C_{oss} = (V_{C1}+V_{C2})C_{oss} \tag{4}$$

where C_{oss} is the output capacitance of the power MOSFETs.

In Mode 4, the minimum charge transferred from i_{L11} to the output capacitors of the two MOSFETs can be derived as,

$$q_{\min} = \frac{1}{2}\cdot T_d \cdot i_{L\min} = \frac{1}{2}\cdot T_d^2 \cdot \frac{V_{c1}}{L_{11}} \tag{5}$$

From equations (4) and (5), the dead band should be designed as follows,

$$T_d \ge \sqrt{\frac{2(V_{C1}+V_{C2})L_{11}C_{oss}}{V_{C1}}} \tag{6}$$

B. Inductor Design

The inductor peak current (I_{peak}) can be derived from the specified average equalization current (I_{ave}),

$$I_{peak} = I_{ave}\frac{2}{D_{\max}} \tag{7}$$

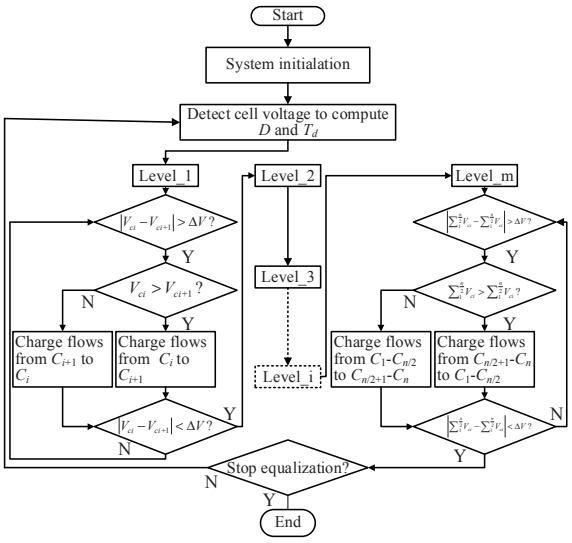

Fig. 5 The control flowchart of the equalizer.

The maximum inductance is determined by the switching frequency (f_s), the maximum battery cell voltage (V_{Cmax}), the maximum duty cycle, as well as I_{peak}. This relationship is defined as,

$$L_{\max} = \frac{V_{C\max}D_{\max}}{I_{peak}f_s} \tag{8}$$

C. Control Strategy

A control strategy is enforced to evaluate the performance of proposed battery equalizer. The corresponding control flowchart is plotted in Fig. 5. As shown, when the voltage mismatch is detected, the corresponding equalizers in the first layer is activated until the balance is achieved. When the equalization of the first level is fully achieved, the identical control strategy spreads up to higher levels. Therefore, the overall cell voltage equalization can be achieved after the equalization of the mth level. Moreover, the adopted control strategy enables a flexible equalization path. This helps to improve the equalization speed.

It should be noted that the proposed equalization method is based on the open circuit voltage of the cell. This is because in battery charging/discharging mode, the voltage drop across the internal resistance of cell affects the accuracy of equalization evaluation. Since we can only measure the terminal voltage of each cell during charging/discharging mode, the compensation of the internal resistance voltage drop should be addressed in the control algorithm. Especially, the detected terminal voltage of the discharging/charging cell is compensated with an estimated internal resistance voltage drop in real time. This guarantees the accuracy of the equalization judgement.

IV. Comparative Analysis of the Proposed Equalizer

A. Comparison of Equalization Speed

The equalization speed is the main criteria of the battery equalization performance. Generally, the higher the power rating of the equalizer is, the shorter the equalization time becomes. Thus, if the power rating of the equalizer circuit is

TABLE I

THE REQUIRED CYCLES FOR BIDIRECTIONAL CELL-TO-CELL METHOD

position of i^{th} cell	position of j^{th} cell						
	C_1	C_2	C_3	C_4	…	C_{N-1}	C_N
C_1	-	1	2	3	…	N-2	N-1
C_2	1	-	1	2	…	N-3	N-2
C_3	2	1	-	1	…	N-4	N-3
C_4	3	2	1	-	…	N-5	N-4
…	…	…	…	…	…	…	…
C_{N-1}	N-2	N-3	N-4	N-5	…	-	
C_N	N-1	N-2	N-3	N-4	…	1	-

fixed, the average number of equalization cycles can be chosen as the figure of merit to evaluate the equalization speed [9]. The proposed equalizer can be seen as one of the "adjacent cell-to-cell" methods. This is because different equalizers placed at different levels transfer charge between two adjacent cells or strings. In order to simplify the analysis, it assumes that there is only one mismatched battery cell in the battery string, while the other cells are balanced to the same voltage. A battery string with N series-connected battery cells is considered. The required average number of cycles to achieve final balance can be defined as,

$$Cycle_{ave}=\frac{\sum Cycle_{ij}}{Num_{\text{total}}} \tag{9}$$

where $Cycle_{ij}$ is the required number of charge transfer cycles from the ith cell to the jth cell. Num_{total} is the number of all possible imbalance cases. For the above-mentioned assumptions, $Num_{total}=N$.

For the bidirectional cell-to-cell (C2C) method, the equalizers are coupled in series. The required transfer cycles from the i^{th} cell to the j^{th} cell are listed in Table I. Based on Table I, the average number of required cycles of the bidirectional C2C method can be calculated as,

$$\begin{aligned}\sum Cycle_{ij}&=2\left(\sum_{k=1}^{N-1}k+\sum_{k=1}^{N-2}k+\sum_{k=1}^{N-3}k+\cdots+\sum_{k=1}^{2}k+\sum_{k=1}^{1}k\right)\\&=\frac{N(N^2-1)}{3}\end{aligned} \tag{10}$$

$$Cycle_{ave}=\frac{(N^2-1)}{3} \tag{11}$$

The direct cell-to-cell (C2C) method transfers charge between the two selected battery cells. Only two battery cells of the whole battery string can be equalized at one specific instant. Therefore, the minimum value of the sum of the required cycles and its average value can be derived as,

$$\sum Cycle_{ij}=N(N-1) \tag{12}$$

$$Cycle_{ave}=N-1 \tag{13}$$

For the proposed equalizer, when N is equal to a power of 2, the sum of required cycles is expressed as,

$$\sum Cycle_{ij}=N\log_2^N=Nm,\ \text{if } N=2^m \tag{14}$$

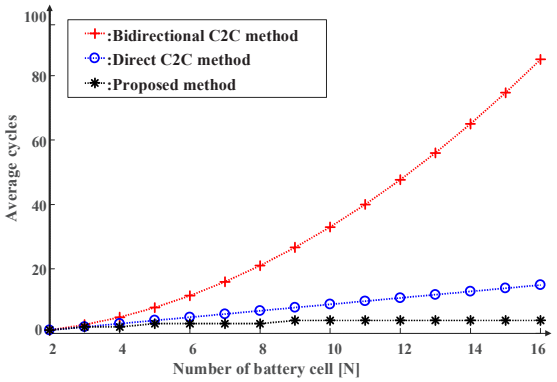

Fig. 6 The average cycles for charge transfer of each method.

$$\begin{aligned}\sum Cycle_{ij}=&\begin{cases}(N-1)\log_2^{2^m}+1\times1, & \text{if } N-2^{m-1}=1\\(N-2)\log_2^{2^m}+2\times2, & \text{if } N-2^{m-1}=2\\(N-3)\log_2^{2^m}+2\times2+1, & \text{if } N-2^{m-1}=3\\\quad\vdots\end{cases}\\&\sum Cycle_{ij}\le N\log_2^N=Nm\end{aligned} \tag{15}$$

where m is the number of levels in the equalizer. when $2^{m-1}<N<2^m$, the sum of required cycles is expressed as Eq. (15). As shown, it is difficult to obtain an accurate value for the sum of required cycles, especially when N is large. The worst case is that the required equalization cycles of each imbalanced cell are estimated to the maximum value m.

In this worst case, the maximum average value of the proposed method can be expressed as,

$$Cycle_{ave}=m \tag{16}$$

From equations (11), (13) and (16), the average cycles of each method can be depicted in Fig. 6. The proposed method in the worst case demonstrates the less number of average cycles than the bidirectional C2C method and the direct C2C method. Especially, for applications with a large number of series cells, the proposed method demonstrates better equalization speed.

B. *Efficiency Analysis*

The conversion efficiency is an important figure of merit to evaluate the performance of the battery equalizer. Since the proposed equalizer is configured by a modified buck-boost circuit, this paper focuses on the basic buck-boost unit to evaluate the efficiency. As shown in Eq. (17), the power loss includes the conduction loss and switching loss of the MOSFETs and conduction loss and core loss of the inductor.

$$P_{loss}=P_{S\_conduction}+P_{S\_switching}+P_{L\_conduction}+P_{L\_core} \tag{17}$$

Typically, the conduction loss of the MOSFETs can be evaluated as,

$$\begin{aligned}P_{Sw1\_conduction}&=i_{S\_RMS}^2R_{on}=\left(i_{peak}\sqrt{\frac{D}{3}}\right)^2R_{on}\\P_{Sw2\_conduction}&=i_{S\_RMS}^2R_{on}=\left(i_{peak}\sqrt{\frac{1-D}{3}}\right)^2R_{on}\end{aligned} \tag{18}$$

where R_{on} is the on-resistance of the MOSFETs. The switching loss generally consists of turn-on loss and the turn-

off loss. Since the proposed equalizer is controlled to operate at the bipolar CCM, the ZVS is achieved when the MOSFETs turns on. Thus, the switching loss of the modified buck-boost converter only contains the turn-off loss and can be derived as,

$$P_{switching} = P_{switching\_on} + P_{switching\_off} = \frac{1}{2} i_{peak} (V_{c1} + V_{c2}) t_{off} f_s \quad (19)$$

where t_{off} is the turn-off time of MOSFET, f_s is the switching frequency.

The conduction loss and core loss of the inductor can be expressed as,

$$P_{L\_conduction} = i_{L\_RMS}^2 R_L = \left(\frac{i_{peak}}{\sqrt{3}} \right)^2 \left(\rho \frac{l_e}{A_e} \right) \quad (20)$$

$$P_{L\_core} = \eta f_s^{\alpha} B_m^{\beta} V_{core} \quad (21)$$

where R_L is the resistance of the inductor wire. B_m is the AC flux swing, η, α and β are the coefficients of the core loss, determined by the magnetic material of inductor core. V_{core} is the effective volume of the inductor core.

Thus, the power efficiency of the basic buck-boost converter unit can be calculated as,

$$\eta_{equalizer\_unit} = \frac{p_{in} - p_{loss}}{p_{in}} \quad (22)$$

From equations (17)-(22), the theoretical efficiency of the basic buck-boost converter can be evaluated. If the required number of cycles to complete equalization increases, the overall efficiency decreases due to the required transfer cycles.

C. Comparison of Switching Loss

For the equalizer proposed in [11], the buck-boost converter operates at the unipolar continuous conduction mode (CCM). The corresponding switching loss can be expressed as,

$$P_{switching} = P_{switching\_on} + P_{switching\_off} = \frac{1}{2} i_{peak} (V_{c1} + V_{c2}) t_{on} f_s + \frac{1}{2} i_{peak} (V_{c1} + V_{c2}) t_{off} f_s \quad (23)$$

In comparison with Eq. (19), this equalization method suffers from higher switching loss. In high switching frequency applications, this deteriorates the conversion efficiency.

V. Simulation and Experimental Results

A. Simulation Results

In order to validate the analysis of the proposed equalizer and control strategy, an equalizer to balance four mismatched energy storage units is designed and simulated in PSIM. To accelerate the simulation speed, the battery cells are emulated by capacitors with extremely large capacitances. The simulation results are captured in Fig. 7. The initial capacitor voltages distribute randomly in the nominal operation region of Lithium-Ion batteries, (i.e. 3.6, 3.8, 3.85 and 3.9 V). As shown, the voltages of the four series-connected capacitors converge to be equal after the equalization progress.

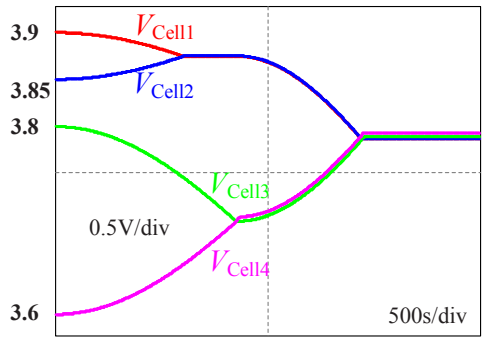

Fig. 7. Simulated balancing process of four series- connected capacitors.

TABLE II
DESIGN PARAMETERS OF THE EQUALIZER

Component Type	Parameters
Lithium-Ion battery	NCR18650PF (3.6 V/2.7 Ah)
Microcontroller	TMS320F28335
Monitor IC	BQ76PL536
MOSFET	AUIRF4104 (R_{on} = 4.3 mΩ, C_{oss} = 850 pF, t_{off} = 33 ns)
Inductor	15 μH 4 A (V_{core} = 0.28 cm^3, R_L = 65 mΩ)

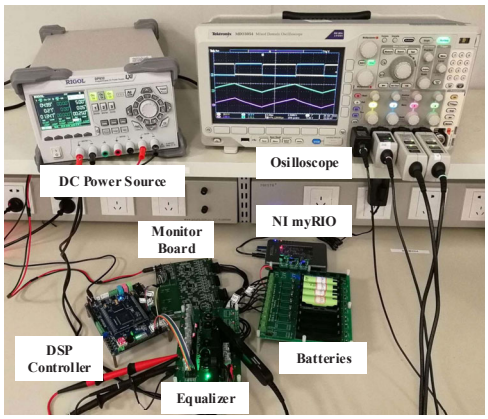

Fig. 8 The photo of experiment setup.

B. Experimental Results

An experimental prototype for four series-connected Lithium-ion battery cells is implemented to verify the theoretical and simulation results. The design parameters are listed in Table II. NCR18650PF Lithium-Ion battery cells, which are widely used in industrial applications, are employed in the prototype. The experimental setup is illustrated in Fig. 8. As shown, a monitor IC (BQ76PL536) is used to sense the cell voltages, leading to the convenience of voltage detection for series-connected battery strings. A digital signal processor (DSP) reads the voltage through the protocol of serial peripheral interface (SPI). A DC power source provides power to DSP, monitor IC and the isolated drivers of MOSFETs.

The key waveforms of the experimental are captured in figures 9 and 10. Fig. 9 presents the critical switching waveforms of S_{w2} and i_{L11}. Fig. 10 shows the key switching

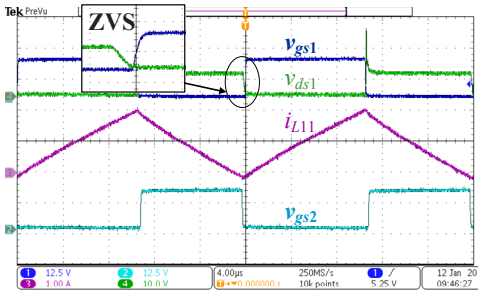

Fig. 9 v_{gs1}, v_{ds1} of S_{w1}, v_{gs2} of S_{w2} and the inductor current i_L.

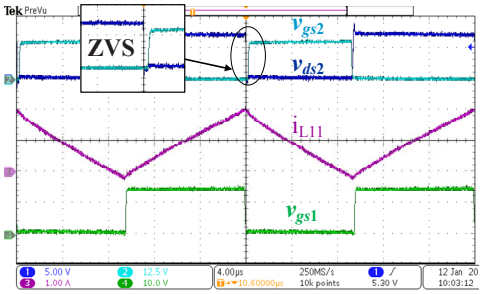

Fig. 10 v_{gs2}, v_{ds2} of S_{w2}, v_{gs1} of S_{w1} and the inductor current i_L.

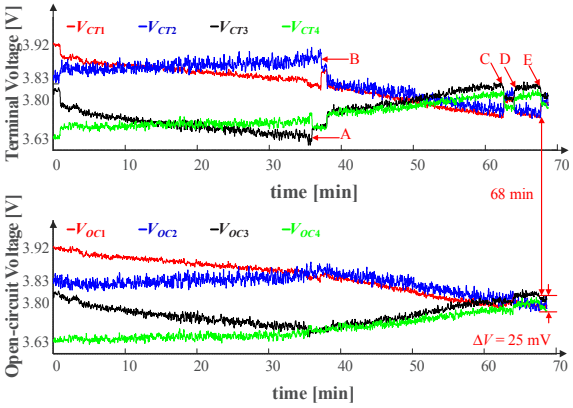

Fig. 11 The open circuit voltage (V_{OC}) and terminal voltage (V_{CT}) of the four cells

waveforms of S_{w1} and i_{L11}. As shown in figures 9 and 10, the MOSFET drain to source voltage drops to zero before the gate signal is applied. This indicates good ZVS performances for the MOSFETs. Figures 9 and 10 validate the bipolar CCM operation of the equalizer.

Fig. 11 shows the experimental open-circuit voltages and the terminal voltages of the four series-connected Lithium-Ion battery cells during the equalization process. The voltage data is sampled by the NI myRIO 1900 platform. As shown in Fig. 11, the initial voltages are 3.92, 3.84, 3.80 and 3.63 V, respectively. Specifically, the initial voltage difference between Cell3 and Cell4 is smaller than that of Cell1 and Cell2. Hence, this leads to an earlier equalization (at point A) between Cell3 and Cell4. When the equalization process of level_1 is completed, level_2 starts.

The voltages of the four cells converge to the predefined average value at point C. Thus, the equalizer is switched to idle mode. However, the battery cells self-recover in this idle mode. The certain open circuit voltage mismatch is again sensed. This mismatch is evaluated as higher the tolerated margin. Thus, the equalizer is enabled again at point D. At point E, it is judged that final equalization is achieved and the battery equalizer is switched to idle mode again. The initial voltage difference is 290 mV. The total equalization process takes 68 minutes, and the open-circuit voltage difference is reduced to 25 mV. This validates the control algorithm and the simulation results shown in figures 5 and 7, respectively.

VI. Conclusion

In this paper, a hierarchical battery voltage equalizer for series-connected battery string is presented. Its basic equalization unit is based on the modified buck-boost circuit. In the proposed equalizer, the basic converter operates at bipolar CCM with an accurate control of the circulating current. All the MOSFETs operate with ZVS to reduce the switching loss. Moreover, the hierarchical architecture provides flexible equalization paths for cell or strings. Thus, the equalization speed is improved. An advanced control strategy based on the open-circuit voltage is introduced to optimize both the conversion efficiency and the equalization speed. The comparison of equalization speed between different "cell-to-cell" architectures is conducted to verify the equalization performance. In addition, The functionality of the equalizer is validated by the simulation and experiment results.

Acknowledgement

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