A Seven-Level Boost Inverter for Medium Power PV Applications

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Abstract—Conventional multilevel inverters typically utilize high component count and cannot step up the input voltage. This paper presents an improved multilevel boost-type inverter with low component count. The proposed inverter is able to generate a seven-level ac output voltage \(0, 0.5V_{dc}, V_{dc}, 1.5V_{dc}, -0.5V_{dc}, -V_{dc}, -1.5V_{dc}\), while only eight switches and three capacitors are employed. The charge pump principle helps to boost the output voltage to 1.5 times of the input voltage. A level-shift pulse-width-modulation mechanism is introduced to drive the switches. The switch pattern is designed to balance the capacitors’ voltages and to control the charge/discharge of the filtering capacitor. In order to verify and validate the proper operation of the developed circuit configuration, the system is simulated in MATLAB/Simulink and are experimentally evaluated using a hardware set-up. Obtained results agree well with the theoretical analysis. A low total-harmonic-distortion is achieved with low filter requirement and the capacitor voltages are well balanced with the level-shift pulse-width-modulation pattern.

Keywords—Charge pump principle, level-shift pulse-width-modulation (LS-PWM), multilevel inverters, seven-level.

I. INTRODUCTION

Conventional two level inverters such as H-bridge inverter are flawed with low reliability, high voltage stress, and bulky filters [1]-[7]. Therefore, in medium and high power applications, they are being replaced by multilevel inverters [8]-[10]. Multilevel inverter generates output voltage in staircase shape with high power quality and high conversion efficiency. However, with the increase of voltage levels, the count of switches, drivers and capacitors increases dramatically. Moreover, special attention needs to be paid to the voltage balance of capacitors.

In general, multilevel inverters evolve towards solutions with reduced components count and balanced capacitor voltage [11]-[13].

Multilevel inverters can be divided into three categories: neutral point clamped (NPC) [14]-[17], cascaded H-bridge [18]-[19] and flying capacitors [20]-[22] inverters.

In grid connected photovoltaic (PV) systems, the terminal voltage of PV panel is low and varies with the environmental conditions. Therefore, an intermediate Boost converter is typically required. This Boost converter degrades the system power density and conversion efficiency. Alternatively, charge pump technique can also boost the voltage without the need for inductors [23]. The charge pump circuit steps up the voltage using switch capacitor principle. The capacitors are charged in parallel while discharged in series, or vice versa [24].

Different seven-level inverters have been presented in literature. In [25], a seven-level boost converter is presented to boost the output voltage to 1.5 times of input voltage. However, it utilizes 10-switches. Large number of switching devices may lead to increased system cost and degraded efficiency.

In [26] authors has presented unique single-phase seven-level multilevel inverter for PV applications. Although the topology can generate seven-level, but it doesn’t have boosting ability and big number of diodes are utilized.

In [27], a seven-level multilevel inverter is developed to generate the required level with reduced switching device count. Seven switches and two diodes are employed. However, the topology is not able to boost the input voltage.

In this paper, a new seven-level converter is proposed. The general schematic of the developed structure is plotted in Fig. 1. As shown, single phase version requires 8 switches and one flying capacitor to generate 7 level output voltage with amplitude higher than input voltage, while three-phase version requires 24 switches and three flying capacitors.

The proposed converter is able to boost the input voltage by a factor of 1.5 using charge-pump principle. For generating the required pulses for the switches, level-shift pulse-width-modulation technique is applied.
Fig. 2. Schematic of the proposed novel seven-level boost inverter.

II. TOPOLOGY DESCRIPTION AND OPERATION PRINCIPLES

The single-phase schematic of the proposed seven-level boost inverter is depicted in Fig. 2. \( V_{dc} \) is the input voltage, \( V_o \) is the output voltage, \( C_1 \) and \( C_2 \) are the input capacitors with \( n \) serving the neutral point, and \( C_o \) is the flying capacitor. \( C_1 \) is equal to \( C_2 \), which means they split the input voltage evenly. As shown, the developed topology has only 8 switches, 2 of them do not require anti parallel diode. This means they could be implemented with IGBT or with series connection of MOSFET and diode. Switching devices have different voltage stresses, as summarized in Table I. \( S_5 \) and \( S_8 \) have their voltage stresses compared to the other six switches, while \( S_7 \) and \( S_8 \) have to withstand twice of the input voltage. Eight valid switching states are used to generate the seven level profile. All valid switching states are mentioned in Table II. The maximum number of ON state switches is three. Indeed, in most of the cases, only two switches are ON. This helps to reduce the semiconductor conduction loss. The operation modes are depicted in Fig. 3. The circuit operation can be divided into 8 modes.

**Mode 1**, the inverter generates an output voltage equals \( V_{dc}/2 \) [see Fig. 3 (a)]. \( S_1, S_2 \) and \( S_3 \) are ON, and other switches are OFF. \( C_1 \) and \( C_2 \) are charged from the dc source with a matched voltage, \( V_{dc}/2 \). \( C_o \) is charged from the input voltage source and its steady-state voltage equals \( V_{dc} \). Output positive terminal (A) is connected to the positive terminal of \( C_1 \), and output negative terminal (B) is always connected to the neutral point of the switched capacitor.

**Mode 2**, the inverter generates an output voltage equals to 0 [see Fig. 3 (b)]. \( S_4 \) and \( S_5 \) are ON, and other switches are OFF. \( C_1 \) and \( C_2 \) are charged from the dc source and they have equal voltage value of \( V_{dc}/2 \). \( C_o \) is floating. This mode is a freewheeling stage. Output positive terminal (A) and (B) are connected to the neutral point of the switched capacitor.

**Mode 3**, the inverter generates an output voltage equals to \( V_{dc} \) [see Fig. 3 (c)]. \( S_1 \) and \( S_6 \) are ON, and other switches are OFF. \( C_1 \) and \( C_2 \) are charged from the dc source and they have equal voltage value of \( V_{dc}/2 \). \( C_o \) is discharging its stored energy to the load. Output positive terminal (A) is connected to the neutral point of the switched capacitor.

**Mode 4**, the inverter generates an output voltage equals to \( 1.5V_{dc} \) [see Fig. 3 (d)]. \( S_1 \) and \( S_7 \) are ON, and other switches are OFF. \( C_1 \) and \( C_2 \) are charged from the dc source and they have equal voltage value of \( V_{dc}/2 \). \( C_o \) is discharging its stored energy to the load. Output positive terminal (A) is connected to the positive terminal of capacitor \( C_o \).

| TABLE I. VOLTAGE STRESSES OF SWITCHING DEVICES |
|-----------------|------------------|
| Switching device | Voltage stress    |
| \( S_3, S_4, S_5 \) | \( V_{dc} \)     |
| \( S_3, S_5 \)      | \( 1.5V_{dc} \)  |
| \( S_5, S_7 \)      | \( V_{dc} \)     |
| \( S_5, S_8 \)      | \( 2V_{dc} \)    |

**Mode 5**, the inverter generates an output voltage \( -V_{dc}/2 \), \( V_{dc}/2 \) [see Fig. 3 (e)]. \( S_5, S_6 \) and \( S_7 \) are ON, and other switches are OFF. \( C_1 \) and \( C_2 \) are charged from the dc source and they have equal voltage value of \( V_{dc}/2 \). \( C_o \) is charged from the input voltage and it is steady state value equals \( V_{dc} \). Output positive terminal (A) is connected to the positive terminal of \( C_o \).

**Mode 6**, the inverter generates output voltage equals to 0 [see Fig. 3 (f)]. \( S_1, S_3 \) and \( S_8 \) are ON, and other switches are OFF. \( C_1 \) and \( C_2 \) are charged from the dc source and they have equal voltage value of \( V_{dc}/2 \). \( C_o \) is floating. This mode is a freewheeling stage. Output terminals (A) and (B) are connected to the neutral point of the switched capacitor.

**Mode 7**, the inverter generates an output voltage equals to \( -1.5V_{dc} \) [see Fig. 3 (g)]. \( S_1 \) and \( S_7 \) are ON, and other switches are OFF. \( C_1 \) and \( C_2 \) are charged from the dc source and they have equal voltage value of \( V_{dc}/2 \). \( C_o \) is discharging its stored energy to the load. Output positive terminal (A) is connected to the negative terminal of \( C_o \).

**Mode 8**, the inverter generates an output voltage equals to \( -0.5V_{dc} \) [see Fig. 3 (h)]. \( S_1 \) and \( S_8 \) are ON, and other switches are OFF. \( C_1 \) and \( C_2 \) are charged from the dc source and they have equal voltage value of \( V_{dc}/2 \). \( C_o \) is now in series with \( C_2 \). Output positive terminal (A) is connected to the negative terminal of \( C_o \).

III. LEVEL SHIFT PULSE WIDTH MODULATION

A level-shift pulse-width-modulation (LS-PWM) mechanism is introduced to modulate the proposed 7-level inverter. According to \([28]-[29]\), n-level inverter requires (n-1) carrier waveforms and a reference signal. As the proposed topology has seven levels, six carriers are employed, as depicted in Fig. 4. The switching pattern is determined by comparing the carrier signals with sinusoidal reference signal. The six carriers are symmetrical with identical amplitude, phase shift, and switching frequency. The modulation procedure represents six different sectors.

In Sector 1, the reference signal is compared with carrier signal \( e_1 \) and generates an output voltage from zero to \( -0.5V_{dc} \).

In Sector 2, reference signal is compared with carrier signal \( e_2 \) and generates an output voltage from \( -0.5V_{dc} \) to \( V_{dc} \).

In Sector 3, reference signal is compared with carrier signal \( e_3 \) and generates an output voltage from \( -V_{dc} \) to \( -1.5V_{dc} \). Due to the symmetrical operation, the positive half cycle is illustrated with the same procedure.
Fig. 3. Operation modes of the proposed converter (a) Mode 1, (b) Mode 2, (c) Mode 3, (d) Mode 4, (e) Mode 5, (f) Mode 6, (g) Mode 7, and (h) Mode 8.
IV. RESULTS AND DISCUSSIONS

In order to validate the proposed concept, a simulation model is built in MATLAB/Simulink and then a hardware prototype is implemented inside the laboratory. Parameters used in simulation and real time implementations are summarized in Table III.

In Fig. 5, the system is simulated with resistive load, no output filter is added. Output voltage and output current are staircase with seven level \(0, 0.5V_{dc}, V_{dc}, 1.5V_{dc}, -0.5V_{dc}, -V_{dc}, -1.5V_{dc}\). As shown, \(C_1\) and \(C_2\) have their voltages matched to \(0.5V_{dc}\), while \(C_0\) has its voltage equals to \(V_{dc}\).

The THD of the output current in this case of study is illustrated in Fig. 6 and it is found to be 47%.

Fig. 7 shows the simulation results with \(R\ L\) load. Load current becomes smoother due to inductive load. The total harmonic distortion is reduced to 22% as shown in Fig. 8.

Experimental prototype has been built in laboratory to validate the operation of the proposed seven-level multilevel-inverter. Camera-shot for the hardware set-up is shown in Fig. 9. Parameter used to build the hardware set-up is summarized in Table IV. Level-shift PWM is implemented using DSPACE 1202. Pulses applied to the power switches are captured in Figs 10 and 11.

S\_1 and S\_4 are operating at fundamental frequency, while other switches are working at high switching frequency. The measured output voltage and voltages of \(C_1\) and \(C_2\) are captured in Fig. 12.

V. CONCLUSIONS AND FUTURE WORK

A novel seven-level inverter with boosting ability is developed in this paper. The proposed inverter is able to generate a seven-level output voltage with boosting ratio of 1.5. It is constructed from eight-switches, two of them (S\_1 and S\_3) operate at fundamental frequency. Two switches (S\_2 and S\_4) does not require anti-parallel diode, where they could be implemented using IGBT or series connection of MOSFET and diode.

In order to generate switching signals for the inverter switches, level-shift PWM technique is employed, where six-carriers are used to generate the required number of voltage levels.

Level-shift PWM is designed to keep capacitor voltage balanced and control the voltage of the neutral point. The system was simulated with MATLAB/Simulink and hardware set-up has been built in the laboratory. Obtained results agreed well with the theory analysis.
References


