Abstract—This article proposes an ultrawide output range LLC resonant converter based on adjustable turns ratio transformer and reconfigurable bridge. Due to the reconfiguration of the transformer by two four—quadrant switches, the transformer exhibits three different effective turns ratios, which correspond to three output ranges. Moreover, in case of lower output voltage, the primary side is reconfigured as a half-bridge to further extend the output voltage range. The design of resonant tank parameters is less constrained by the voltage gain requirement. The switching frequency range in each mode can be squeezed close to the resonant frequency, which contributes to an improved soft switch performance. The operational principles, design considerations, and mode transition are analyzed. A 4 A rated prototype that converts 390 V input to a 60–450 V output is designed and tested to validate the concept. A smooth mode transition is achieved without transient issues. The design prototype demonstrates 97.50% peak efficiency and good overall efficiency performance over this ultrawide output range.

Index Terms—LLC resonant converter, reconfigurable bridge, reconfigurable transformer, ultrawide output range.

I. INTRODUCTION

In applications such as plug-in electric vehicle (PEV) battery charging, the dc/dc converter needs to be adapted to a wide output range. In certain extreme conditions such as battery deeply deletion, an ultrawide output range is required [1]. LLC topology is a prevalent candidate due to its characteristics of the soft-switching performance, low electromagnetic interference, and simple topology with low components count [2]–[4].

The operation of the LLC converter is deemed as optimal when its switching frequency is matched with the resonant frequency [5]. Either high conduction loss or lost of soft switching on the secondary side occurs when the switching frequency deviates from the resonant frequency. In order to realize an ultrawide output range, an ultrawide frequency range is necessary. Additionally, small magnetizing inductance is usually required. This leads to high circulation current and high conduction loss.

To achieve a good compromise between conversion efficiency and output range, many techniques have been studied to optimize the design parameters and to squeeze the frequency range of the LLC converter. In [6]–[9], different design methodologies are investigated to make full use of the voltage regulation with high efficiency. However, the converter structure constrains the voltage regulation capacity and makes it unsuitable for ultrawide voltage applications.

Topological reconfiguration can also extend the output range. Many reconfigurable structures have been proposed. In [10], the secondary side is reconfigured with two effective transformer turns ratios. The efficiency over the wide output range can be enhanced significantly. However, it is insufficient to achieve an ultrawide output range, and the transformer copper utilization is low. In [1] and [11], the secondary side rectifier is reconfigured to voltage-doubler mode or voltage-quadrupler mode to extend the output range. However, the current stress increases substantially on the secondary side. This leads to high conduction loss. In [12]–[15], the full-bridge and half-bridge structures are reconstructed to achieve a wide output range. However, the transfer current of half-bridge structure is doubled in comparison with the full-bridge, and the power source utilization is low. This means half-bridge is more suitable for light load conditions. In [16], an interleaved LLC converter with a cascaded voltage-doubler rectifier is introduced. The cascaded structure can achieve a doubled output range. However, the frequency range is still very wide in ultrawide output range applications. This leads to degraded performance. In [17], an interleaved LLC resonant converter with a hybrid rectifier and variable-frequency plus phase-shift control is proposed. The phase shift control in responsible for the voltage regulation with switching frequency higher than the resonant frequency. Consequently, the switching frequency can be narrowed down, and a high output range can be achieved.

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be achieved. However, the hybrid method increases the control complexity and implementation difficulty because there are two control variables. Moreover, it should be noted that the majority of the proposed converters require multiple transformers, resonant tanks and extra switches, which increase the system volume and cost.

Another way to achieve wide output range is pulsewidth modulation (PWM). In [18], a secondary-side PWM modulation scheme is introduced to regulate the output voltage. In [19] and [20], a bidirectional switch is added to reconfigure the primary side between the full-bridge and half-bridge. In [20], the secondary side can be reconfigured as a full-wave rectifier and voltage-doubler rectifier. The output range can be effectively extended. In [21] and [22], hybrid bridge and dual-transformer are introduced into the dual-active-bridge converter to extend its output range. However, output range is still constrained by the structure and an ultrawide output range cannot be achieved.

In this article, a unique ultrawide output range LLC converter is proposed. The proposed converter is based on adjustable turns ratio transformer and reconfigurable bridge. The output range can be extended remarkably via three effective transformer turns ratios and a half-bridge mode. The half-bridge is only enabled in very low voltage. This avoids additional loss incurred by the increased current stress. Soft switching can be ensured in all four modes. Singular frequency modulation is employed with low control complexity. Each mode is assigned a specific unit gain. Thus, it operates with the switching frequency close to the resonant frequency. The mode transition can be achieved instantaneously without transient issues. Its optimal parameters design is in analogy to that of the conventional LLC converter.

II. TOPOLOGY AND OPERATION PRINCIPLES

A. Topology Description

Fig. 1 shows the schematic of the proposed LLC converter. The primary side is a full-bridge inverter with four MOSFETs. The resonant tank consists of the resonant capacitor (C_r), the resonant inductor (L_r), and the magnetizing inductor of the transformer (L_m). The transformer is center-tapped on the secondary side. The turns numbers of three windings are n_1, n_2, and n_3, respectively. The secondary side is a rectifier bridge with six diodes. Two four-quadrant switches are used to facilitate the mode transition. Each switch consists of two back-to-back MOSFETs. By controlling the ON/OFF states of the four-quadrant switches, the transformer secondary side turns can be configured as n_2, n_3, n_2 + n_3, respectively. This helps to effectively extend the output range of the converter.

B. Operation Principles

Fig. 2 demonstrates the equivalent circuits of four modes. When S_5 is turned on and S_6 is turned off, the effective transformer turns ratio is n_2 : n_1. Mode I is activated when the primary side is configured as a half-bridge, as shown in Fig. 2(a). Mode II is activated when the primary side is configured as a full-bridge as shown in Fig. 2(b). When S_6 is turned on and S_5 is turned off, the effective transformer turns ratio is n_3 : n_1 and Mode III is activated. Mode IV is activated when both S_5 and S_6 are turned on. In Mode IV, the effective transformer turns ratio is (n_2 + n_3) : n_1. With the abovementioned four modes, the output voltage can be divided into four segments: [V_L, V_{th1}], (V_{th1}, V_{th2}), (V_{th2}, V_{th3}), and (V_{th3}, V_H). V_L, V_H are the lower and upper bounds of the output voltage. V_{th1}, V_{th2}, and V_{th3} are the upper bound output voltages of Modes I–III, correspondingly. Meanwhile, they are the lower bound output voltages of Modes II–IV, correspondingly. Therefore, V_{th1}, V_{th2}, and V_{th3} are the threshold voltages, which trigger the mode transitions.

The steady-state waveforms at the threshold voltage V_{th1} in Modes I and II are plotted in Fig. 3. Fig. 3(a) shows the waveforms when V_o = V_{th1} in Mode I, the switching frequency (f_s) is lower than the resonant frequency between L_r and C_r (f_r). It corresponds to the lower bound voltage in Mode I. With further increase of output voltage, the mode transition from Modes I to II is triggered. Fig. 3(b) shows the waveforms when V_o = V_{th2} in Mode II, f_s is higher than f_r. It corresponds to the lower bound output voltage in Mode II. The conditions in threshold voltages V_{th2} and V_{th3} are similar to that in threshold voltage V_{th1}.

Within each mode, f_s is the only control variable. The voltage gain decreases as f_s increases. When f_s equals f_r, the voltage gain is equal to the transformer turns ratio. When f_s is lower than f_r, the resonant current intersects with the magnetizing current before the primary gate signal turns ON/OFF, as shown in Fig. 3(a) at t_0. As a result, the secondary-side diodes operate in discontinuous mode that leads to naturally zero-current-switching (ZCS) turning-OFF. However, on the primary side, the
circulating current as shown in the shadow area of Fig. 3(a) increase with the decrease of $f_s$. Then, the root-mean-square (rms) value of the resonant current $i_{Lr}$ increase significantly. Additionally, it should be noted that if $f_s$ is substantially lower than $f_r$, the primary-side MOSFETs may lose ZVS. Therefore, the lower bound of $f_s$, which corresponds to the upper bound output voltage should be designed to be close to $f_r$. When $f_s$ is higher than $f_r$, the resonant current intersects with the magnetizing current after the primary gate signal turns OFF as shown in Fig. 3(b) at $t_2$. As a result, the secondary side loses ZCS. Additionally, the circulating current decreases with the increase of $f_s$. Therefore, there is a tradeoff between the secondary side turning-OFF loss and primary side conduction loss. With substantial increase of $f_s$, the small circulating current hardly affects the primary side current. However, the MOSFETs turning-OFF current and diodes turning-OFF $di/dt$ both increase. Both lead to an increased switching loss. Thus, the upper bound $f_s$, which corresponds to the lower bound output voltage gain should be designed close to $f_r$ as well.

C. Mode Transition

Mode transition is important as a harsh transition typically come with large voltage and current transients, which may incur system failures. When the output voltage reaches $V_{th1}$, the mode transition is triggered to switch the circuit operation from Modes I–II. When the output voltage reaches $V_{th2}$, the mode transition is triggered to switch the circuit operation from Modes II to III. A similar process happens if the output voltage reaches $V_{th3}$, the circuit is triggered to switch from Modes III to IV.

Fig. 4(a) exhibits the transition from Modes I to II. On the primary side, $S_3$ is driven from constantly OFF to be identical to the gate signal of $S_2$. $S_4$ is driven from constantly ON to be identical to the gate signal of $S_1$. $f_s$ steps from the lower bound frequency in Mode I ($f_{min1}$) to the upper bound frequency in Mode II ($f_{max2}$). The drive signals of $S_2$ and $S_6$ on the secondary side are unchanged. It is worth noting that the transformer clamping voltage remains unchanged during the transition. However, the sudden jump of $f_s$ leads to a short transit time. Correspondingly, the magnetizing inductor releases its energy as shown in Fig. 4(b). Moreover, it should be noted that there is a $V_{DC}/2$ bias on the resonant capacitor in half-bridge structure. The dc bias decreases to zero in full-bridge structure. Then, the energy stored in the resonant capacitor is transferred to the resonant inductor, which leads to an increase of the inductor current. Meanwhile, the inductor transfers the energy to the secondary side. Consequently, a minor dynamic occurs in $i_{Lr}$ during the mode transition. Define the spike of $i_{Lr}$ during mode transition as $I_{P1}$, and the steady state magnitude of $i_{Lr}$ as $I_{P2}$. Since the energy stored in the resonant capacitor is fixed, $(I_{P1}^2 - I_{P2}^2)$ remains constant. This means $(I_{P1} - I_{P2})$ decreases with the increase of $I_o$. The steady-state output voltages before and after the mode transition are unchanged as well. Therefore, a smooth transition from Modes I to II can be achieved.

Fig. 4(b) exhibits the transition from Modes II to III. On the primary side, $f_s$ steps from the lower bound frequency in Mode II ($f_{min2}$) to the upper bound frequency in Mode III ($f_{max3}$). On the secondary side, $S_5$ is turned OFF and $S_6$ is turned ON. The switching actions occur in a synchronous manner, right at the end of an switching period. Hence, the mode transition is realized instantaneously. It is also worth noting that the transformer clamping voltage remains unchanged during the transition. However, the effective transformer turns ratio $n$ is increased. Then, the $di/dt$ of $i_{Lm}$ decreases. In addition, the sudden jump of $f_s$ leads to a short transit time. Correspondingly, the magnetizing inductor releases its energy as shown in Fig. 4(b). The steady-state output
voltages before and after the mode transition are unchanged. In addition, there is no net change in the dc bias of the resonant capacitor voltage. Therefore, a smooth transition from Modes II to III can be achieved.

The mode transition from Modes III to IV is similar to that from Modes II to III and it not discussed separately.

### III. Design Considerations

#### A. Voltage Gain

Fig. 5 shows the equivalent circuit model of the proposed converter, where

- In Mode I: \( m = 1/2, n = n_2/n_1 \)
- In Mode II: \( m = 1, n = n_2/n_1 \)
- In Mode III: \( m = 1, n = n_3/n_1 \)
- In Mode IV: \( m = 1, n = (n_2 + n_3)/n_1 \).

The entire output range is divided into four segments. Thus, the frequency range of each segment can be squeezed and designed to be close to \( f_r \). The first harmonics approximation method can be employed to analyze the circuit model. Thus, the voltage gain of the proposed converter is

\[
M_g = \frac{mn}{\sqrt{1 + 1/L_n - 1/(L_nf_n^2)}} + Q_c^2(f_n - 1/f_n)^2
\]

where

\[
L_n = \frac{L_m}{L_r}, Q_c = \sqrt{L_r/C_r}, f_n = \frac{f_s}{f_r} = \frac{\omega}{\omega_0}
\]

\[
R_{ac} = \frac{8V_o^2}{n^2\pi^2P_o}, \omega_0 = \frac{1}{2\pi\sqrt{L_rC_r}}.
\]

\[n\] is the effective transformer turns ratio, \( Q_c \) is the quality factor, and \( P_o \) is the output power.

#### B. Design Consideration

1) \( L_n \) and Transformer Turns Ratio: The voltage gain is a function of \( L_n \) and \( n \). Fig. 6 showcases the voltage gain with different \( L_n \) when the transformer turns ratio \( n = 1 \) and \( Q_c = 0.7 \). In order to obtain a better gain curve, \( L_n = 3.5 \) is selected. The turns ratio of the transformer is the key parameter that determines the output range. In order to make the voltage gain continuous between adjacent modes and \( f_s \) squeezed close to \( f_r \), the upper bound voltage in Mode X should be equal to the lower bound voltage of the Mode X + 1 (X \( = I-III \)), respectively. Actually, there should be a voltage margin to avoid repeated mode switching at switching point, which can be achieved by slightly extending the frequency range. Moreover, the lower bound voltage of Mode I should be equal to the minimum output voltage (\( V_{IL} \)). The upper bound voltage of Mode IV should be equal to the maximum output voltage (\( V_{IH} \)). The boundaries of \( f_s \) in Modes I–IV are assumed as \((x_1, x_2), (x_3, x_4), (x_5, x_6), (x_7, x_8)\), respectively, as shown in Fig. 7. Then, the following minimization problem should be solved

\[
\text{min}_{x \in R^{11}} \sum_{i=1}^{8} (x_i - 1)^2
\]

s.t.

\[
M_{gt}(x_1) = V_L/V_{DC}
\]

\[
M_{gt}(x_2) = M_{gt}(x_3)
\]

\[
M_{gt}(x_4) = M_{gt}(x_5)
\]

\[
M_{gt}(x_6) = M_{gt}(x_7)
\]

\[
M_{gt}(x_8) = V_H/V_{DC}
\]

\[n_2/n_1 + n_3/n_1 - n_4/n_1 = 0
\]
be designed to be close to $f_r$. In order to make $f_s$ evenly distributed on both sides of $f_r$, a coefficient $\alpha$ is added to region of objective with $f_s < f_r$. Meanwhile, the difference between Modes I and II lies on the structure of the primary side inverter.

The optimization function tends to narrow down the frequency range of Mode II, which makes Mode II not maximize its voltage regulating function. A coefficient $\beta$ should be added to the point of Mode II in the objective function to solve this problem. The upper bound $f_s$ of Modes I and II is assumed to be equal ($x_1 = x_3$). Then, the minimization problem can be rewritten as

$$\min_{x \in R^{11}} \sum_{i=1,5,7} (x_i - 1)^2 + \sum_{j=2,6,8} (x_j - 1)^2 + \alpha \beta (x_3 - 1)^2 + \beta (x_4 - 1)^2$$

s.t. $G_1(x) = M_{gi}(x_1) - V_L/V_{DC} = 0$

$G_2(x) = M_{gi}(x_2) - M_{ii}(x_3) = 0$

$G_3(x) = M_{gi}(x_4) - M_{ii}(x_5) = 0$

$G_4(x) = M_{gi}(x_6) - M_{ii}(x_7) = 0$

$G_5(x) = M_{gi}(x_8) - V_L/V_{DC} = 0$

$G_6(x) = n_2/n_1 + n_3/n_1 - n_4/n_1 = 0$

$G_7(x) = x_1 - x_3 = 0$. (5)

The Taylor expansion of the objective function is derived. Only the first two terms are considered, the variables and equality constraints can be expressed as

$$\min_{\Delta x \in R^{11}} f(x) = \frac{1}{2} \Delta x^T M(x) \Delta x + B(x)^T \Delta x$$

s.t. $G(x_k) + A_{x_k} \Delta x = 0$ (6)

where

$$x = \left[ x_1 \ x_2 \ x_3 \ x_4 \ x_5 \ x_6 \ x_7 \ x_8 \ \frac{n_2}{n_1} \ \frac{n_3}{n_1} \ \frac{n_4}{n_1} \right]^T$$

$$G(x) = \left[ G_1 \ G_2 \ G_3 \ G_4 \ G_5 \ G_6 \ G_7 \right]^T$$

$$\Delta x = x - x_k$$

$$B(x_k) = \nabla F(x_k)$$

$$M(x_k) = \nabla^2 F(x_k)$$

A. (7)

The Lagrange multiplier method is employed to construct the following function:

$$L(\Delta x, \lambda) = \frac{1}{2} \Delta x^T M(x_k) \Delta x + B(x_k)^T \Delta x + \lambda^T G(x)$$

where $\lambda$ is the coefficient. The following results can be obtained from the extreme condition of a function with several variables

$$M(x_k) \Delta x + B(x_k) + A(x_k)^T \lambda = 0$$

$$A(x_k) \Delta x + G(x_k) = 0$$. (9)

If (9) is written as a matrix, the following result can be obtained

$$\begin{bmatrix} M(x_k) & A(x_k)^T \\ A(x_k) & 0 \end{bmatrix} \Delta x = \begin{bmatrix} -B(x_k) \\ -G(x_k) \end{bmatrix}$. (10)

Assume that

$$H = \begin{bmatrix} M(x_k) & A(x_k)^T \\ A(x_k) & 0 \end{bmatrix}$$

$$\Delta X = \begin{bmatrix} \Delta x_k \\ \lambda \end{bmatrix}, \ b = \begin{bmatrix} -B(x_k) \\ -G(x_k) \end{bmatrix}$. (11)

Then, the solution can be derived from the iteration

$$X_{k+1} = X_k + H^{-1}b$$. (12)

The turns ratios of the transformer are calculated as $n_2/n_1 = 0.36$, $n_3/n_1 = 0.68$ after 100 iterations, and the turns ratio in Mode IV is $n_4/n_1 = 1.04$.

Fig. 7 shows the voltage gain versus normalized $f_s$. The red line marks the operation region. The threshold voltages and frequency bounds are marked as well.

2) Dead Time $t_d$ and $L_{m}$: As mentioned above, the $f_s$ range of each mode is designed to be close to $f_r$. Only $f_s = f_r$ is taken into consideration. In order to reduce the volume of magnetic component without causing particularly high switching loss, $f_r$ is selected to be 140 kHz. Since the difference between $i_{Lr}$ and $i_{lm}$ is the current that flows through the secondary side, the following relationship stands

$$\begin{cases} \frac{2}{T_s} \int_0^{T_s} \sqrt{2I_{rms,p}} \sin(\omega t + \phi) + \frac{V_o}{n_{ms}} \left( \frac{T_0}{4} - t \right) dt = n I_o \\ \frac{2}{T_r} \int_0^{T_r} \left[ i_{Lr}(t) - i_{lm}(t) \right]^2 dt \\ n \end{cases}$$

(13)

where $T_0$ and $T_s$ are the resonant period and switching period, respectively. $\phi$ is the initial phase of $i_{Lr}$. For a given output current ($I_o$), the rms current of the primary side ($I_{rms,p}$) and secondary side ($I_{rms,s}$) can be calculated as

$$\begin{cases} I_{rms,p} = \frac{I_o}{4\sqrt{2n}} \sqrt{R^2 T_0^2 + 4 n^4 \pi^2 + \frac{16 n^4 \pi^2}{T_0^2} (T_0 t_d + t_d^2)} \\ I_{rms,s} = \frac{\sqrt{6} I_o}{24 \pi} \sqrt{\frac{(5\pi^2 - 48) R^2 T_0^3}{L_m n^4} + \frac{12 \pi^2 (T_0 + 2 t_d)}{T_0}} \\ L_m \end{cases}$. (14)

To ensure ZVS, the upper limit of magnetizing inductance can be derived as

$$L_m \leq \frac{T_{min} t_d}{16 C_{os}}$. (15)

where $C_{os}$ is the equivalent output capacitance of the MOSFETs, $t_d$ is the deadband, and $T_{min}$ is the global minimum switching period. To obtain enough voltage gain and to ensure the ZVS of the primary switches, the maximum $f_s$ is set to be $f_{max} = 250$ kHz. Then, $T_{min}$ can be calculated as $T_{min} = 1/f_{max} = 4 \mu s$. Substitute (15) into (14), the RMS current of the primary and
Fig. 8. Total conduction loss versus the output current and dead time.

The secondary sides can be calculated as

\[
\begin{align*}
I_{\text{rms},p} &= \frac{I_o}{4\sqrt{2}n} \sqrt{\frac{256C_{\text{min}}^2 R_{\text{on}}^2 T_0}{T^2_{\text{min}} + 4T^2_{\text{on}}} + 4n^4\pi^2 \left( \frac{T_0 + 2T_{\text{on}}}{T_0} \right)^2}, \\
I_{\text{rms},s} &= \frac{\sqrt{6}I_o}{24\pi} \sqrt{\frac{256C_{\text{min}}^2 (5\pi^2 - 48) R^2 T^2_0}{n^4\omega^2 T^2_{\text{min}} + 12\pi^2(T_0 + 2T_{\text{on}})} + 12\pi^2(T_0 + 2T_{\text{on}})}.
\end{align*}
\]

Taking the conduction loss with \( f_s = f_r \) in each mode into consideration, the total conduction loss can be calculated as

\[
P_{\text{Cond}} = \sum_{X=\text{I,II,III,IV}} [I_{\text{rms},p,X}^2 (2R_{\text{ds}} + R_{T_{\text{on}}} X) + I_{\text{rms},s,X}^2 (R_{T_{\text{on}}} X + R_{M,X} + 2R_d)]
\]

where \( R_{\text{ds}} \) is the on-resistance of the primary side MOSFETs, \( R_d \) is the equivalent series resistance of the rectifier diodes, \( R_{M,X} \) is the on-resistance of the four-quadrant switches, \( R_{T_{\text{on}}} \) and \( R_{T_{\text{on}}} X \) are the ac resistances of the transformer on the primary side and secondary side, \( I_{\text{rms},p,X} \) and \( I_{\text{rms},s,X} \) are the rms currents on the primary side and secondary side in Mode X, respectively. Fig. 8 shows the total conduction loss with different output currents versus the dead time. As shown, under different output currents, the total conduction loss decreases sharply initially and then barely changes with the increase of dead time. Therefore, in order to obtain an overall high efficiency, \( t_d \) is designed to be 120 ns.

To reduce the MOSFET turning off current and circulating current, \( I_m \) should be sufficiently large. In this article, \( I_m \) is selected to be 350 \( \mu \)H according to (15). Then, the resonant inductance and capacitance are calculated as \( L_r = 100 \mu \)H and \( C_r = 12.8 \) \( \mu \)F.

3) Transformer Design: Fig. 9 shows the configuration of the transformer windings and the equivalent circuit. As shown the secondary side is intermediately tapped with three ports. The resonant inductor is integrated into the transformer primary side to reduce the system volume. There are three critical design parameters: the transformer turns ratios, the magnetizing inductance, and the resonant inductance. Moreover, the transformer core loss and copper loss should be considered when evaluating the efficiency. To avoid magnetic saturation, the magnetic flux variation (\( \Delta B \)) can be expressed as

\[
\Delta B = \frac{V_o T_s}{4n_s A_c} < B_s
\]

where \( n_s \) is the secondary turns count, \( A_c \) is the effective cross-section area of the magnetic core, and \( B_s \) is the saturation flux. Since the transformer core loss (\( P_{\text{core}} \)) can be expressed as

\[
P_{\text{core}} = V_c k_c f_s^3 \Delta B^3
\]

where \( k_c, \alpha, \) and \( \beta \) are coefficients determined by core materials, and \( V_c \) is the core volume. As indicated in (19), at fixed \( f_s \), \( \Delta B \) determines the core loss. On the other hand, the copper loss of one winding can be calculated as

\[
P_{\text{copper}} = \frac{\rho_u \omega A}{A_c} \left[ \sum VA \right] = \rho_u \omega A_{\text{w}} A_{p}
\]

where \( \rho_u \) is the resistivity of the wire, \( A_{\text{w}} \) is the effective cross-section area of the wire. \( I_{\text{rms}} \) and \( I_u \) are the rms current and length of the winding, \( V_u \) is the voltage utilization factor, \( J_0 \) is the current density, and can be calculated as

\[
J_0 = \frac{\sum VA}{K_v f_s \Delta B} k_f k_u A_p
\]

where \( \sum VA \) is the VA rating of all the windings. \( K_v \) is the voltage waveform factor. \( k_f \) is the core stacking factor. \( A_p \) is the core cross section area by the window winding area. Then, the total loss can be expressed as

\[
P_{\text{total}} = P_{\text{core}} + P_{\text{copper}} = V_c k_c f_s^3 \Delta B^3 + \rho_u \omega V_u k_u \left[ \sum VA \right] \frac{1}{K_v k_f k_u A_p} \left[ \frac{1}{2} f_s^2 \Delta B^2 \right]\]

At given \( f_s \), the total loss of the transformer has a global minimum value when

\[
P_{\text{core}} = \frac{2}{\beta} P_{\text{copper}}.
\]

Then, the transformer turns can be obtained as

\[
n_s = \frac{V_s T_s}{4A_c \beta f_s^2 V_c k_c \rho_u \omega V_u k_u \left[ \sum VA \right] \left[ \frac{1}{2} f_s^2 \Delta B^2 \right]}
\]

After the transformer turns counts are determined, the leakage inductance and the magnetizing inductance need to be designed.
The leakage inductance is contributed by the uncoupled magnetic flux between the primary and secondary sides of the transformer. Therefore, it can be tuned by changing the coupling coefficient. The magnetizing inductance is contributed by the coupled magnetic flux between the primary and secondary sides of the transformer. Therefore, it can be tuned by adjusting the length of the air gap. Fig. 10 shows the flowchart of the transformer design.

4) Voltage Stresses: Since ZVS can be implemented over a wide output range in different modes on the primary side, there is no oscillate on the drain source voltages of the primary MOSFETs. Therefore, the voltage stresses on the primary MOSFETs is

\[ V_{\text{stress}_1-4} = V_{\text{DC}}. \]  (25)

When the converter operates in Modes I and II, the voltage stress on \( S_6 \) can be derived as

\[ V_{\text{stress}_6} = n_3 V_o / n_2. \]  (26)

Similarly, the voltage stress on \( S_5 \) in Mode III can be expressed as

\[ V_{\text{stress}_5} = n_2 V_o / n_3. \]  (27)

When the converter operates in Mode IV, both \( S_5 \) and \( S_6 \) are ON. Their voltage drops are close to zero. Moreover, since the energy stored in the leakage inductance can be released during the mode transition, no extra voltage stress is generated during the mode transition.

5) Switching Loss: Since the \( f_s \) range is designed to be close to \( f_r \) in each mode, only \( f_s = f_r \) is taken into consideration. The primary side MOSFETs are turned ON with zero voltage. Therefore, there is no MOSFETs turning-ON loss. Moreover, the secondary side diodes are turned OFF with zero current, there is no diode reverse recovery loss. Thus, the major switching loss is the MOSFET turning-OFF loss. The turning-OFF loss is determined by the turning-OFF current and high \( f_s \) MOSFETs counts. The turning-OFF current \( (I_{\text{off}}) \) of half-bridge \( (I_{\text{off},H}) \) and full-bridge \( (I_{\text{off},F}) \) structure are derived as

\[ I_{\text{off},H} = \frac{V_{\text{DC}} T_s}{8 L_m}, \]

\[ I_{\text{off},F} = \frac{V_{\text{DC}} T_s}{4 L_m}. \]  (28)

when the MOSFET is turned OFF, the MOSFET drain source voltage \( v_{ds} \) rises from zero to \( V_{\text{DC}} \), the current decrease from \( I_{\text{off}} \) to zero. Then, the integral of MOSFET voltage current product equals the absorbed energy. The absorbed energy can be divided into two parts, one is the energy stored in the junction capacitor of the MOSFET, which is released during the ZVS turned ON, the other is the net turning-OFF loss. Hence, the turning-OFF loss \( (P_{\text{off}}) \) can be derived as

\[ P_{\text{off}} = m f_s \left[ \int_0^{t_{\text{off}}} v_{ds}(t) i_{ds}(t) \, dt - \frac{1}{2} C_{\text{oss}} V_{\text{DC}}^2 \right]. \]  (29)

where \( m \) is the high \( f_s \) MOSFETs counts, \( v_{ds}(t) \) and \( i_{ds}(t) \) are the MOSFET voltage and current, \( t_{\text{off}} \) is the rise time of \( v_{ds} \).

IV. Experimental Results

To verify the proposed concept, a 4 A rated converter prototype is designed and tested experimentally. Table I summarizes
the design parameters and components selection. Fig. 11 shows the picture of the designed converter.

The steady-state waveforms of the designed prototype are captured in Fig. 12. Fig. 12(a) shows the experimental steady-state waveforms with \( V_o = 80 \) V in Mode I. As indicated, on the primary side, the current lags the voltage of the resonant tank. This helps to achieve the ZVS turning ON of the primary side. Fig. 12(b) captures the steady-state waveforms with \( V_o = 120 \) V in Mode II when \( f_s \) is above \( f_r \). It means the voltage gain is lower than the transformer turns ratio. The ZCS turns OFF of the diodes is lost on the secondary side. Fig. 12(c) demonstrates the steady-state waveforms with \( V_o = 260 \) V in Mode III when \( f_s \) equals \( f_r \). ZVS is achieved on the primary side and ZCS is achieved on the secondary side. Fig. 12(d) shows the steady-state waveforms with \( V_o = 450 \) V in Mode IV when \( f_s \) slightly below \( f_r \).

Fig. 13 showcases the measured-efficiency versus output voltage with different output currents. In each mode, the performance is optimal when \( f_s \) is close to \( f_r \), the efficiency degrades when \( f_s \) deviates from \( f_r \). Then, an efficiency intersection appears between adjacent modes. These intersection points can be selected as the threshold voltages, which trigger the mode transitions. The converter demonstrates 97.50% peak efficiency. As a comparison counterpart, a traditional full-bridge LLC resonant converter prototype is designed. \( \text{Cr} = 12 \text{ nF}, \text{Lr} = 100 \mu \text{H}, \text{Lm} = 350 \mu \text{H}, n = 30 : 26 \), both the magnetic core and the power semiconductors are unchanged. As indicated in Fig. 13, the traditional LLC converter is unable to achieve the ultrawide output range, the frequency reaches 350 kHz when the output voltage is 250 V. If the switching frequency further increases, the voltage further decreases slightly. However, the switching loss and core loss increase fast, which deteriorates the efficiency. Although the conventional converter has higher peak efficiency when \( f_s \) close to \( f_r \), the proposed converter demonstrates an overall high efficiency over the ultrawide output range.

Fig. 14 shows the loss breakdown of the proposed converter at \( f_r \) with the same output current (1 A) in different modes. Due to the ZVS of the primary side and ZCS of the secondary side, the switching loss is merely the MOSFETs turning-off loss. As indicated, the conduction loss of the primary MOSFETs and the secondary diodes is nearly the same in Modes II–IV, and slightly lower in Mode I. This is because the RMS current of the secondary side diodes dominates the total conduction loss. Besides, due to the low magnetizing current of half-bridge in Mode I, the total conduction loss can be reduced. The transformer copper loss is increased in different modes due to the increase of power transfer. The conduction loss of the mode transition switches is determined by the number of switches and the current. Since the mode transition switches are either constantly ON or OFF, there is no extra switching loss. Additionally, the transformer core loss is significantly reduced in Mode I due to the low transformer volt–second of the half-bridge mode. In Modes II–IV, although the output voltage changes, the volt–second are almost unchanged due to the change of the transformer turns ratio. The turning-off loss decreases significantly in Mode I due to the decrease of the high \( f_s \) MOSFET counts and turning-off
Correspondingly, the load transition experiments are conducted as shown in Figs. 15–17. Fig. 15(a) shows the waveforms of mode transition from Modes I to II. The primary side is reconfigured from half-bridge to full-bridge. $f_s$ steps from the lower bound frequency in Mode I to the upper bound frequency in Mode II. There is a short duration for $L_m$ to release its stored energy during the transition. In Fig. 15(b), the trajectory jumps from Modes I to II. The dc voltage of the resonant capacitor decreases to zero. The current stress decreases with the decrease of the period. Fig. 16(a) shows the waveforms of mode transition from Modes II to III. As indicated, $f_s$ steps from the lower bound frequency in Mode II to the upper bound frequency in Mode III. On the secondary side, $S_5$ is turned off and $S_6$ is turned on. Fig. 16(b) shows the trajectory from Modes II to III. As indicated, the current stress decreases with the increase of the frequency. Also, there is a short duration for $L_m$ to release its stored energy during the transition. Fig. 17 shows the waveforms and trajectory of mode transition from Modes III to IV. As shown, $f_s$ steps from the lower bound frequency in Mode III to the upper bound frequency in Mode IV. The current stress is slightly decreased. The duration for $L_m$ to release its stored energy is similar to that in the transition from Modes II to III. Fig. 18 shows the waveforms when the output voltage change from 450 to 250 V. All of the abovementioned mode transitions occur instantaneously without transient issues.
A comparison between the proposed topology and some recently published wide output range topologies is made as shown in Table II. As indicated, the proposed topology exhibits a low count of high-frequency MOSFETs, transformers and resonant tanks, a wide output range and good overall efficiency.

V. CONCLUSION

In this article, an ultrawide output range LLC converter based on adjustable turns ratio transformer and reconfigurable bridge was proposed. The converter can operate with three effective transformer turns ratios. The half-bridge reconfiguration further extend the output range to its lower bound. The proposed converter has the following advantages:

1) the frequency range is squeezed in each mode, which allows the LLC converters to work with $f_s$ close to $f_r$;
2) design of resonance network parameters is less constrained by the voltage gain requirement;
3) soft switching can be implemented over a wide range;
4) an ultrawide output range can be achieved;
5) the transformer exhibits high copper utilization;
6) singular frequency modulation is adopted, which simplifies the control scheme.

A 4 A rated converter prototype which converts 390 V input to 60–450 V output is designed and tested to verify the proposed concept. The designed prototype demonstrates good efficiency over this ultrawide output range. 97.50% peak efficiency is reported. Smooth mode transitions are realized instantaneously without transient issues.

REFERENCES