Design and Implementation of a Dual-Mode Supercapacitor Fast Charger Employing Continuous and Fine-Tuned Pulse Currents

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***Abstract*— As an energy storage technology, supercapacitors feature a high power density. In particular, supercapacitors can be charged or discharged by a relatively large pulse current for a limited period of time. This paper takes advantage of this characteristic and develops a dual-mode fast charger for supercapacitors that employs both continuous and fine-tuned pulse currents. Based on the conventional forward converter, the proposed charger introduces an energy storage capacitor and a branch resistor to tune the rising and falling edges of the pulse current, respectively. Consequently, the transitions between the continuous and pulse current modes are significantly accelerated, which ultimately shortens the supercapacitor charging time. A prototype is built and tested using a 3 V/6 F supercapacitor. To charge the supercapacitor from 2 to 2.5 V, the proposed charger takes 0.87 and 1 s when it is configured to operate in the dual-mode and the continuous current mode only, respectively, which leads to a 13% reduction in the charging time. Moreover, compared to the forward converter, the pulse characteristics of the proposed charger are significantly improved in that the pulse rising and falling times are dramatically reduced: 2.1 versus 147 μs and 7.2 versus 103 μs, respectively.**

***Index Terms*— Supercapacitor, fast charger, dual-mode charging, pulse current, continuous current.**

I. Introduction

SUPERCAPACITORS including electric double layer capacitors (EDLCs) and hybrid capacitors such as lithium-ion capacitors (LICs) feature a higher power density, a longer cycle life, a wider operating temperature range, and a better thermal stability compared to lithium-ion batteries [2], [3], [4]. However, supercapacitors suffer a significantly lower energy density and a much higher self-discharge rate. On the other hand, compared to high-voltage capacitors with relatively low capacitances, the rated voltage of a single supercapacitor is usually much lower although its rated capacitance can be much higher. Therefore, as an energy storage technology, supercapacitors are well-suited in certain applications in which their advantages can be exploited while their drawbacks are not major concerns.

In fact, supercapacitor-based energy storage systems in which supercapacitors are used as the sole technology or supercapacitors are combined with other technologies to form hybrid systems have been investigated for various electrified transportation systems [5], [6], [7], [8], [9], [10], renewable energy systems [11], [12], [13], [14], [15], low power systems [16], [17], [18], [19], [20], [21], and defense systems [22], [23]. Since the rated voltage and capacitance of a single supercapacitor cell are relatively low, multiple supercapacitor cells are usually connected in series and parallel to form modules and packs to boost the charge, power, and energy capacities of supercapacitor systems. For instance, the nominal capacitance and operating voltage range of the supercapacitor cell used in a tram are 28000 F and 2.8-3.8 V, respectively [24]. The supercapacitor system is configured as a 3P216S pack: 3 cells in parallel as a module and 216 modules in series as a pack. The nominal capacitance of the supercapacitor pack is 389 F and the operating voltage range is 605-821 V. The rated power of the supercapacitor pack is approximately 225 kW, which is determined using the operating current of 100 A and the operating voltage of 3.5 V for a supercapacitor cell. As another example, a supercapacitor system with a rated power of 1.5 MW is developed for the stations along a metropolitan rail transit line [25]. The rated input voltage is 500-1000 V and the rated input current is 0-3000 A. To ensure that supercapacitor-based energy storage systems operate properly and efficiently, various aspects such as isolation and insulation, pressure relief valve and explosion-proof design, grounding and polarity protection need to be considered [26].

In particular, the charging mechanisms and circuits of supercapacitors have been investigated. Like other electrochemical energy storage technologies such as lithium-ion batteries, supercapacitors are usually charged in the constant current (CC), constant voltage (CV), or constant power (CP) modes [27]. However, certain aspects of the charging mechanisms of supercapacitors have not been completely revealed [28], [29]. For instance, charge redistribution is a critical relaxation process within the supercapacitor and its

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effects on various characteristics of the supercapacitor such as the self-discharge rate, voltage pattern, and Peukert constant have been investigated [30], [31], [32]. To minimize the voltage decay during the charge redistribution process, an optimal charging protocol is proposed based on a study of the relationship between the charging parameters (e.g., CC magnitude and CV time) and the charge redistribution process [33]. To minimize the charging time for LICs, a model predictive control-based optimal charging strategy is developed based on an electro-thermal model of LICs [34]. For supercapacitor modules used in tram regenerative braking systems, the module temperature is taken as an input to tune the maximum charging current in the proposed charging algorithm [35]. The supercapacitor charging process can be optimized under the constraint of a user-defined charging time [36]. To maximize the capacity utilization of a hybrid energy storage system including supercapacitors and lithium-ion batteries, an optimal charging method is proposed [37].

On the other hand, various charging circuits and control strategies have been proposed for supercapacitors. For instance, a charging circuit that divides the supercapacitor bank into two parts is proposed for energy-limited fast charging applications [38]. To meet the CC and CP charging requirements of supercapacitors and achieve fast charging, a push converter is adopted [39]. To directly charge the supercapacitor banks from the power grid, matrix converters have been utilized [40], [41]. For supercapacitor banks, a coordinated charging strategy is proposed, which also helps balance the supercapacitors [42]. In the field of wireless power transfer, supercapacitor charging is also being investigated [43]. For example, a wireless charging system is designed for the supercapacitors equipped in a sightseeing car [44]. An accurate supercapacitor model is developed to facilitate designing wireless energy harvesting systems [45]. To enhance the supercapacitor charging efficiency, an inductive power transfer converter with a current-controlled semi-active rectifier is proposed [46]. To analyze and design wireless power transfer systems for supercapacitors used in electric vehicles, a method based on a variable resistance is proposed [47].

While a variety of supercapacitor charging strategies and circuits have been proposed, the fact that supercapacitors can be charged by a relatively large pulse current for a limited period of time has not been fully utilized to develop fast and even ultra fast chargers. In fact, supercapacitor datasheets usually specify a continuous current and a pulse current. For instance, the Eaton 3 V/6 F supercapacitor (part number: TV1020-3R0605-R) can sustain a continuous current of 2.4 A and a pulse current of 7.4 A [48]. To take advantage of these two types of currents the supercapacitor can tolerate, a dual-mode supercapacitor fast charger employing both continuous and pulse currents is proposed [49], which is developed based on a conventional forward converter [50]. The most important feature of the proposed charger is that its pulse characteristics are fine tuned compared to the conventional forward converter. By introducing an energy storage capacitor and a branch resistor in the proposed charger, the rising and falling edges of the pulse current are much sharper than those in the conventional forward converter. Therefore, the proposed charger significantly accelerates the transitions between the continuous and pulse currents. The proposed charger is then improved by removing two switches and introducing one diode to reduce the circuit complexity and facilitate the circuit implementation [1]. A prototype is built and some preliminary experiments are performed to demonstrate the feasibility of the proposed charger.

This paper further enhances [1] in the following three aspects. First, the closed-loop control of the prototype is completely implemented and the prototype is tested with a supercapacitor while the prototype in [1] was only tested using an electronic load because the control of the prototype was not completed yet. Second, the voltage and current stresses of the switches in the charger are analyzed. Third, the design considerations for the key components in the prototype are presented. The experimental results demonstrate the feasibility of the proposed charger in accelerating the supercapacitor charging process by implementing the dual-mode operation involving both the continuous and pulse currents. Moreover, the pulse characteristics of the proposed charger are significantly improved compared to the conventional forward charger.

The remainder of this paper is organized as follows. Section II presents the topology of the proposed charger and analyzes its operation modes. Section III analyzes the voltage and current stresses of the switches in the proposed charger. Section IV discusses the design considerations for the proposed charger. Section V shows the experimental setup and results. Section VI concludes this paper.

II. Topology and Operation of Proposed Charger

The topology of the proposed dual-mode fast charger is shown in Fig. 1, which is derived based on a conventional forward converter [50]. By properly setting the reference current, the conventional forward converter is capable of generating both continuous and pulse currents. However, the transitions between the continuous and pulse currents are relatively slow in a conventional forward converter because the voltage across the output inductor is relatively low. For supercapacitors, the pulse current is significantly higher than the continuous current. If the transitions between the continuous and pulse currents are not sufficiently fast, the pulse current may fail to reach the specified peak value within the pulse width. Therefore, to accelerate the transitions, the proposed charger incorporates an energy storage capacitor C_s and a branch resistor R_f to tune the rising and falling edges of the pulse current, respectively. The operation modes of the proposed charger are elaborated as follows. The key waveforms are illustrated in Fig. 2.

A. Steady Current Modes

When the charger operates in a steady current mode (i.e., the output current is stabilized at the continuous current or the peak value of the pulse current and no transitions between the continuous and pulse currents are needed), the charger acts as a forward converter. As shown in Fig. 2, at t_0, S_1 is turned

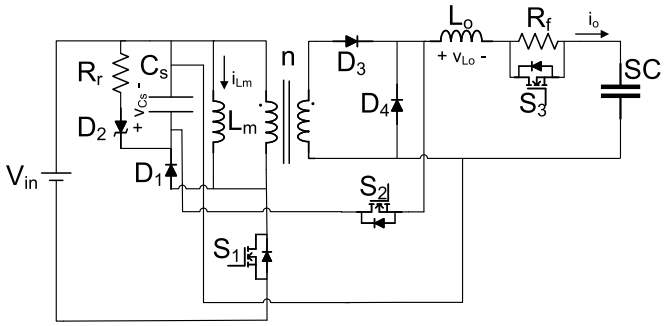


Fig. 1. Topology of proposed charger.

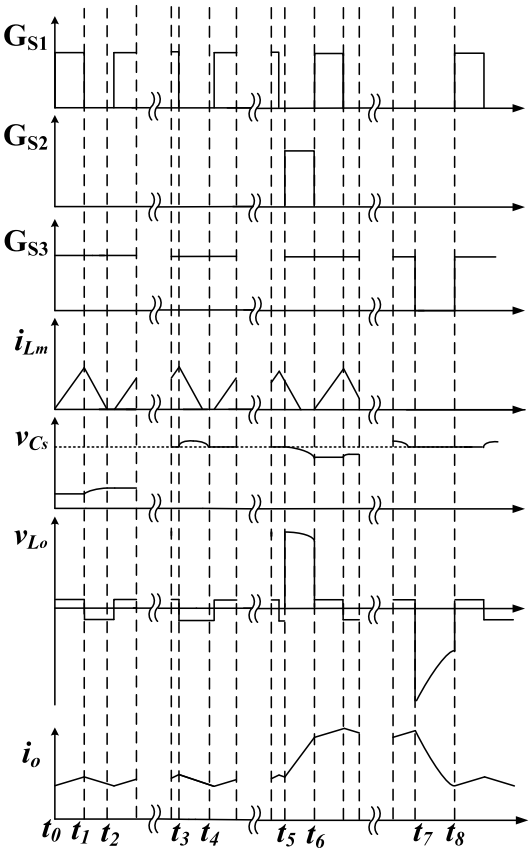


Fig. 2. Key waveforms of proposed charger.

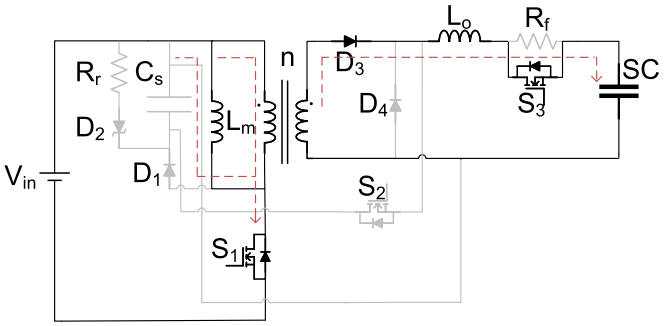


Fig. 3. Steady current mode I: transferring energy from source to supercapacitor through transformer and storing energy in L_m.

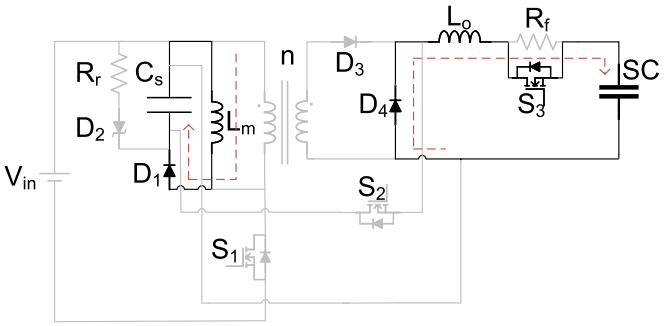


Fig. 4. Steady current mode II: charging of C_s to stabilize its voltage.

on and energy is transferred from the power source V_{in} to the supercapacitor. Fig. 3 shows the equivalent circuit. Note that energy is also stored in the magnetizing inductor L_m during this process.

To ensure that the continuous current mode can be switched to the pulse current mode in a fast transition with a sharp rising edge, C_s needs to build and maintain a high voltage V_Z. As shown in Fig. 4, when S_1 is turned off, L_m charges C_s through D_1 till the current through L_m is reset to zero. During this process, the energy stored in L_m is transferred to C_s. As illustrated in Fig. 2, L_m begins to charge C_s at t_1 and this process ends at t_2.

Actually, if the energy transferred from L_m to C_s is equal to the energy of C_s that needs to be consumed during the pulse rising mode, no additional discharging of C_s is required. However, as the charging process continues, the terminal voltage of the supercapacitor continues to increase. Consequently, the duty cycle D of the charger increases gradually, which leads to an increase in the energy stored in L_m and also an increase in the voltage of C_s. While the C_s voltage needs to be sufficiently high to ensure a fast transition from the continuous current mode to the pulse current mode, its voltage should not be excessively high to avoid potential damages. Therefore, once the C_s voltage exceeds the Zener voltage V_Z, it needs to be discharged to maintain a proper voltage.

The discharging process of C_s may involve three different scenarios, as shown in Fig. 5. Specifically, once the C_s voltage exceeds V_Z, Zener breakdown occurs in the Zener diode D_2. C_s is discharged through D_2 and the discharging resistor R_r. At the same time, the magnetic reset process of L_m may be still in progress and C_s is charged by L_m simultaneously, as shown in Fig. 5(a). As time goes by, the energy stored in L_m is released completely and the magnetic reset process is finished. However, the C_s voltage may still be higher than V_Z and C_s still needs to be discharged, as shown in Fig. 5(b). Note that in Figs. 5(a) and 5(b), S_1 is turned off. The third scenario is shown in Fig. 5(c). If S_1 is turned on and the C_s voltage is still over V_Z, C_s needs to be further discharged through D_2 and R_r. In practice, D_2 turns on and off to ensure that the C_s voltage is stabilized at V_Z. The purpose of adding R_r is to avoid potential damages to D_2 caused by the exponential increase in the current through D_2 as the C_s voltage increases.

B. Pulse Rising Mode

For a conventional forward converter, when its operation changes from the continuous current mode to the pulse current

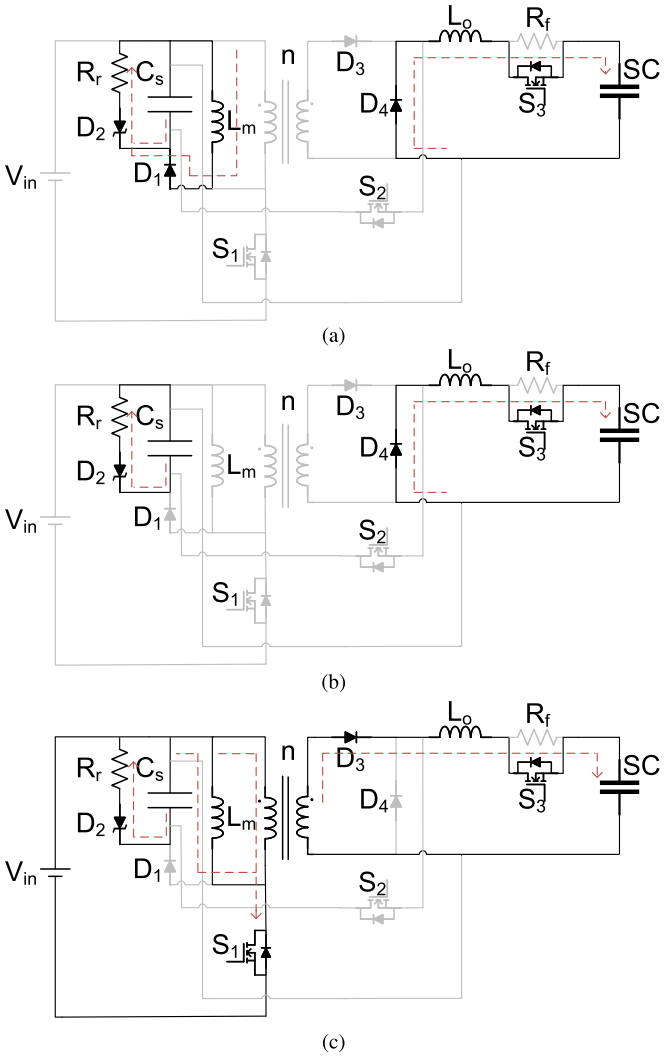


Fig. 5. Steady current mode III: discharging of C_s to stabilize its voltage. (a) Scenario 1. (b) Scenario 2. (c) Scenario 3.

mode, the rising rate of the output current is

$$\frac{\mathrm{d}i_{L_o}}{\mathrm{d}t} = \frac{\frac{V_{in}}{n} - V_{D_3} - V_{SC}}{L_o} \tag{1}$$

where n is the turns ratio of the transformer. On the other hand, when the proposed charger operates in the pulse rising mode, its equivalent circuit is shown in Fig. 6: S_1 is off while S_2 and S_3 are on. The high voltage of C_s established in the steady current modes is applied to L_o and the supercapacitor. Assuming that the voltage of C_s remains constant, the rising rate of the output current is

$$\frac{\mathrm{d}i_{L_o}}{\mathrm{d}t} = \frac{V_Z - V_{SC}}{L_o} \tag{2}$$

Note that $V_Z >> V_{in}/n$. Therefore, compared to the conventional forward converter, the proposed charger implements a much faster transition from the continuous current mode to the pulse current mode. Once the transition is completed, the charger switches to the steady current modes.

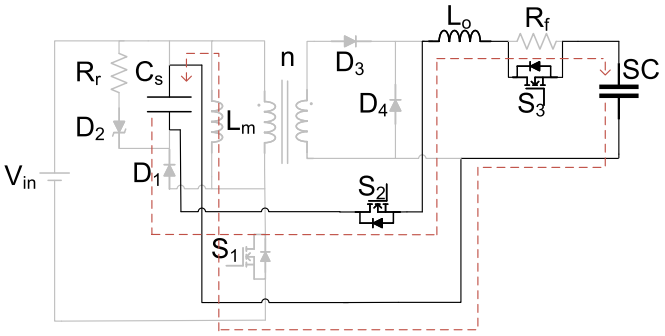


Fig. 6. Pulse rising mode.

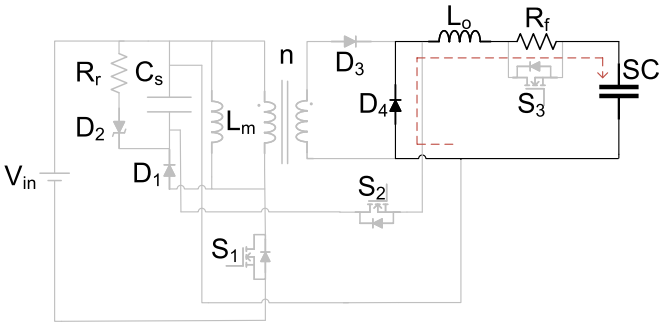


Fig. 7. Pulse falling mode.

C. Pulse Falling Mode

Similar to the pulse rising mode, the conventional forward converter behaves poorly in the pulse falling mode. When the converter switches from the pulse current mode to the continuous current mode, the falling rate of the output current is

$$\frac{\mathrm{d}i_{L_o}}{\mathrm{d}t} = -\frac{V_{D_4} + V_{SC}}{L_o} \tag{3}$$

For the proposed charger, Fig. 7 shows the equivalent circuit in the pulse falling mode. S_1, S_2, and S_3 are turned off. The branch resistor R_f introduces a large voltage drop and accelerates the output current transition:

$$\frac{\mathrm{d}i_{L_o}}{\mathrm{d}t} = -\frac{i_{L_o}R_f + V_{D_4} + V_{SC}}{L_o} \tag{4}$$

where $i_{L_o}R_f >> V_{D_4}$. Again, once the transition is completed, the charger switches to the steady current modes.

III. Voltage and Current Stresses of Switches

To ensure that the proposed charger can be designed and implemented properly, the voltage and current stresses of the switches are analyzed. The continuous and pulse currents are denoted as I_C and I_P, respectively.

The voltage stresses of S_2, D_3, and D_4 are all V_Z. For D_1 and S_1, their voltage stresses are both $V_Z + V_{in}$. Immediately after S_3 is turned off, the current flowing through R_f is I_P. At this moment, S_3 is under the maximum voltage stress:

$$V_{S3} = I_P R_f \tag{5}$$

In particular, the voltage stresses of D_3 and D_4 in the proposed charger are significantly higher than their counterparts in the

forward converter: V_Z versus V_{in}/n. Therefore, the voltage ratings of D_3 and D_4 need to be much higher to implement the proposed charger, which leads to higher component costs, higher component losses, and lower charger efficiency, as further elaborated in Sections IV-A and V-B.

The switch current stresses are

$$I_{S3\_rms} = I_o \tag{6}$$

$$I_{D3\_rms} = \sqrt{D} I_o \tag{7}$$

$$I_{D4\_rms} = \sqrt{1-D} I_o \tag{8}$$

where I_o is the output current. Since the inductance of L_m is a critical parameter, the current stresses of S_1 and D_1 are elaborated as follows.

For S_1, when it is turned on, the current flowing through it is the sum of I_o/n and the current flowing through L_m. Note that I_o is considered to be approximately constant. The current flowing through L_m has been reset to zero before S_1 is turned on. After S_1 is turned on, the current increases linearly with time. Therefore, the current stress of S_1 is

$$\begin{aligned} I_{S1\_rms} &= \sqrt{\frac{1}{T_s}\int_0^{DT_s} (\frac{I_o}{n} + \frac{V_{in}}{L_m} t)^2 dt} \\ &= \sqrt{\frac{V_{in}^2 D^3}{3{L_m}^2 f^2} + \frac{V_{in} I_o D^2}{n L_m f} + \frac{{I_o}^2 D}{n^2}} \end{aligned} \tag{9}$$

where T_s is the switching period, f is the switching frequency, and $T_s = 1/f$. For the continuous and pulse current modes, I_o takes I_C and I_P, respectively.

As indicated in Eqs. (6) through (9), for S_3, D_3, D_4, and S_1, the maximum current stresses correspond to the pulse current mode because I_P is significantly higher than I_C. Therefore, these components are selected based on such worst-case ratings, as further elaborated in Section IV-A.

When S_1 is turned off, a current flows through D_1. During this process, the voltage across C_s is considered to be constant and the current through L_m decreases linearly to zero. The current stress of D_1 is

$$\begin{aligned} I_{D1\_rms} &= \sqrt{\frac{1}{T_s}\int_0^{\frac{DV_{in}T_s}{V_Z}} (\frac{DV_{in}T_s}{L_m} - t\frac{V_Z}{L_m})^2 dt} \\ &= \sqrt{\frac{{V_{in}}^3 D^3}{3V_Z {L_m}^2 f^2}} \end{aligned} \tag{10}$$

For S_2, it is only turned on during the pulse rising process. Given that this process is relatively short, the maximum value of its current is of more interest compared to the effective value:

$$I_{S2\_peak} = I_P \tag{11}$$

IV. Design Considerations

A. General Considerations

A 3 V/6 F supercapacitor (manufacturer: Eaton, part number: TV1020-3R0605-R) [48] with a continuous current of 2.4 A and a pulse current of 7.4 A is used in the experiments. To design and implement the charger prototype, the continuous and pulse currents are set as 2.4 and 7.1 A, respectively. Note that the pulse current magnitude is slightly lower than the specification for safety considerations. The supercapacitor is charged from the initial voltage of $V_i = 2$ V to the final voltage of $V_e = 2.5$ V. The sum of the resistances of L_o, S_3, and the supercapacitor is denoted as R_{on}. The key parameters of the prototype are listed in Table I, which are elaborated as follows.

TABLE I
PROTOTYPE PARAMETERS

Parameter	Symbol	Value
Input voltage	V_{in}	32 V
Output inductor	L_o	100 μH
Transformer turns ratio	n	4
Magnetizing inductor	L_m	100 μH
Branch resistor	R_f	15 Ω
Switching frequency	f	100 kHz
Energy storage capacitor	C_s	4.7 μF
Zener voltage	V_Z	200 V
Discharging resistor	R_r	200 Ω
Diode forward voltage	V_D	1.1 V
Output branch resistance	R_{on}	40 mΩ
DC resistance of Zener diode	R_{ZD}	16 kΩ
Switches 1 and 2	$S_{1,2}$	NCE65T180D
Switch 3	S_3	CI90N120SM
Diodes 1, 3, and 4	$D_{1,3,4}$	SDUR30Q60
Zener Diode	D_2	1N5378BG×2

Referring to Section III, certain switches and diodes are selected as follows. According to Eq. (9), the worst-case current rating of S_1 is about 2.4 A. To implement the prototype, a MOSFET (i.e., NCE65T180D) with a rated current of 21 A is selected [51]. As for D_3 and D_4, their voltage stresses are approximately 200 V (i.e., V_Z). To implement the prototype, the selected diodes (i.e., SDUR30Q60) are rated with a reverse voltage of 600 V and a forward voltage of 1.56 V [52]. For comparisons, the voltage stresses of the diodes in the forward converter are only 8 V (i.e., V_{in}/n). Therefore, the prototype indeed employs components with higher ratings and costs. While the primary objective of implementing the prototype is to demonstrate the feasibility of the proposed dual-mode charging method and the relatively high component ratings and costs are not a major concern, such issues need to be carefully addressed to further improve the proposed charger in the future.

B. Transformer Turns Ratio

To ensure the volt-second balance of L_m, the maximum duty cycle is calculated as

$$D_{lim} = \frac{V_Z}{V_Z + V_{in}} \tag{12}$$

The turns ratio of the transformer is determined as

$$n = \frac{V_{in} D_{lim}}{V_e + V_D + I_P R_{on}} \tag{13}$$

C. Output Inductor

The duty cycle can be found as

$$D = \frac{n(V_{SC} + V_D + I_o R_{on})}{V_{in}} \tag{14}$$

Since the supercapacitor is in the constant current charging stage most of the time, the output current ripple should be as small as possible. In particular, the ripple needs to be less than 10% of the output current when the supercapacitor is charged to V_e with I_C. At this particular time, the current ripple reaches the maximum value. Therefore, the requirement for the output inductor is

$$L_o > \frac{D(\frac{V_{in}}{n} - V_D - I_C R_{on} - V_{SC})}{2\Delta i f} \tag{15}$$

D. Energy Storage Capacitor

For the energy storage capacitor C_s, its voltage should remain almost constant during the pulse rising process. Assuming that its voltage drop is within 1% of V_Z, C_s is sized as follows:

$$C_s > \frac{L_o({I_P}^2 - {I_C}^2)}{({V_Z}^2 - 0.9801{V_Z}^2)} \tag{16}$$

E. Magnetizing Inductor

To determine L_m, it is required that the C_s voltage can still be maintained at V_Z when the output current is I_C at V_i and D takes the minimum value of D_{min}:

$$L_m < \frac{V_{in}^2 D_{min}^2}{f f_P (L_o({I_P}^2 - {I_C}^2) + 2\frac{V_Z^2}{R_{ZD}+R_r})} \tag{17}$$

where f_P is the occurrence frequency of the pulse current and R_{ZD} is the DC equivalent resistance of the Zener diode when the voltage is equal to V_Z.

Considering the DC equivalent resistance of the Zener diode that changes greatly near V_Z and the parasitic capacitance of S_1 that stores energy during the C_s charging process, L_m is finally sized as 100 μH, which is smaller than 320 μH determined by calculations. To implement the transformer, an EC2834 core is selected [53]. The numbers of turns on the primary and secondary sides of the transformer are 40 and 10, respectively. The wire diameter specification is QA2UEWϕ0.1. To tune L_m, additional inductors are connected in parallel with the transformer. From the insulation point of view, the maximum voltage on the primary side of the transformer is V_Z, which is achieved during the C_s charging process. To protect the transformer, its rated voltage needs to be higher than V_Z.

F. Thermal and Loss Analysis

As a key component, R_f is introduced to generate a sharp falling edge for the pulse, which also introduces a significant loss and results in a reduced efficiency for the charger. Specifically, when R_f is just connected to the branch, its current is I_P and its instantaneous power reaches the maximum value of

$$P_{Rf\_ins} = R_f {I_P}^2 \tag{18}$$

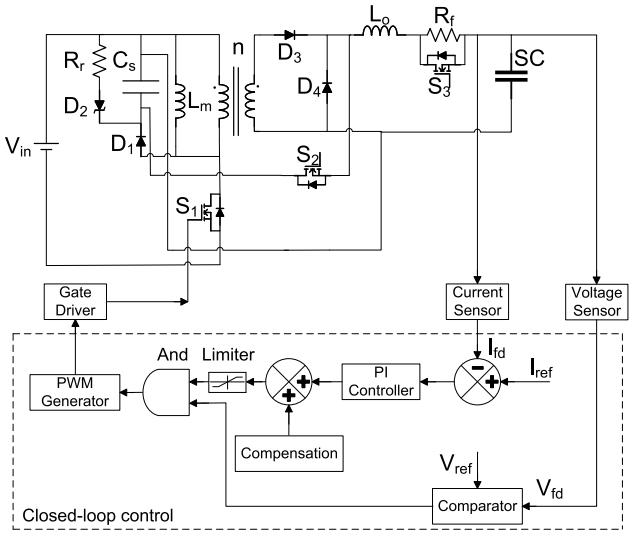


Fig. 8. Control scheme of proposed charger.

According to Eq. (4), when the D_4 forward voltage and the supercapacitor voltage are ignored, the output current can be expressed as

$$i_o = I_P e^{-\frac{R_f}{L_o}t} \tag{19}$$

By integrating i_o, the R_f power can be determined as

$$\begin{aligned} P_{Rf\_con} &= f_P \int_0^{\frac{L_o}{R_f} ln(\frac{I_P}{I_C})} R_f (I_P e^{-\frac{R_f}{L_o}t})^2 dt \\ &= \frac{f_P L_o}{2}({I_P}^2 - {I_C}^2) \end{aligned} \tag{20}$$

On the other hand, R_r together with D_2 also introduce losses when they operate to maintain the stability of the C_s voltage. The power dissipated by R_r and D_2 can be expressed as

$$P_{dis} = \frac{D^2 V_{in}^2}{2 f L_m} - \frac{1}{2} f_P L_o ({I_P}^2 - {I_C}^2) \tag{21}$$

The effects of these losses on the charger efficiency are further elaborated in Section V-B.

G. Control Scheme

The control scheme for the prototype is shown in Fig. 8. The supercapacitor voltage is sampled and compared with the reference V_{ref}. When the sampled voltage V_{fd} is greater than V_{ref}, the PWM signal is set to zero and the charging process is terminated. For the steady current modes, a PI controller is employed to adjust the charging current. Note that the steady current modes include the continuous current mode and the pulse current mode. For the continuous and pulse current modes, I_{ref} is set as I_C and I_P, respectively. Since I_P is higher than I_C, the duty cycle associated with I_P is larger compared to the one associated with I_C. When the current is switched from I_C to I_P, to generate the required duty cycle, additional compensation is added to the control signal generated by the PI controller. To ensure that the transformer is not saturated, the control signal first passes a limiter before it is fed to the AND gate. For the continuous and pulse current modes, the compensation is set as 0 and 0.16, respectively. For S_2 and

S_3, since the pulse rising and falling processes are fast, it is challenging to control them by sampling the current. Instead, they are turned on and off according to the pulse rising and falling times, respectively, which can be determined as

$$t_r = \frac{(I_P - I_C)L_o}{V_Z - V_{SC}} \tag{22}$$

$$t_f = \frac{L_o}{R_f} ln(\frac{I_P}{I_C}) \tag{23}$$

Specifically, for S_2, it is turned on during a period of time equal to the pulse rising time and then turned off. For S_3, it is turned off during a period of time equal to the pulse falling time and then turned on.

V. Experimental Setup and Results

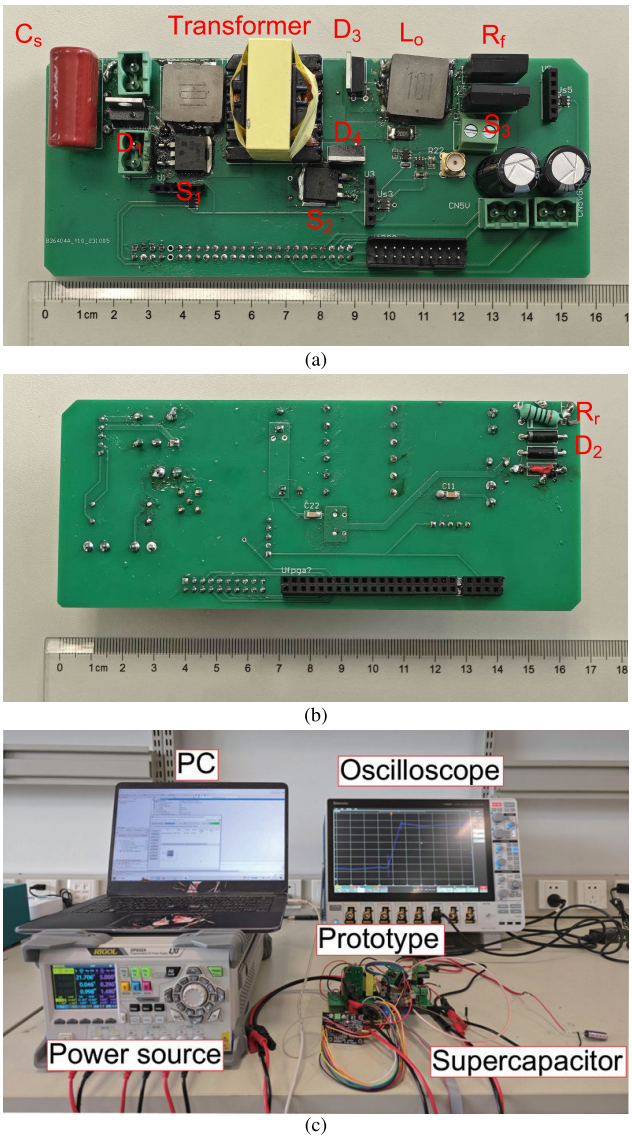
A. Experimental Setup

To evaluate the proposed charger, a prototype is built and tested with an Eaton 3 V/6 F supercapacitor [48], as shown in Fig. 9. In particular, Figs. 9(a) and 9(b) show the front and back views of the prototype, respectively. The key components such as the diodes, switches, transformer, C_s, and R_f are labeled. The test setup is illustrated in Fig. 9(c). For the current pulses, the pulse width is set as 0.25 ms and the pulse period is set as 2.5 ms (or equivalently, the pulse occurrence frequency is set as $f_P = 400$ Hz). Note that these parameters are selected arbitrarily to illustrate the dual-mode operation of the prototype in a proof-of-concept experimental setup.

B. Dual-Mode Operation of Proposed Charger

To verify if the prototype operates properly in both the continuous and pulse current modes, the prototype is used to charge the supercapacitor from 2 to 2.5 V, as shown in Fig. 10. Specifically, Fig. 10(a) shows the supercapacitor voltage V_{SC} and the charging current i_{L_o} during the charging process. Clearly, the supercapacitor voltage increases as the charging process continues. The charging process is terminated when the sampled voltage reaches a particular threshold, which is determined as follows. The maximum equivalent series resistance (ESR) specified in the supercapacitor datasheet is 35 mΩ [48]. Considering the instantaneous voltage change due to the ESR (approximately 0.25 V when the pulse current is 7.1 A), the supercapacitor terminal voltage should be approximately 2.75 V when the expected final voltage is set as 2.5 V. Given the characteristics of the electronics (e.g., resolution of the analog to digital converter) used in the prototype, the charging process is terminated when the sampled voltage reaches 2.78 V. The charging time determined using this process is approximately 0.87 s.

Intuitively, when the pulse period is reduced (or equivalently, the pulse occurrence frequency is increased) or the pulse width is increased, the charging time can be further reduced. However, the thermal management of the charger and the supercapacitor may be more challenging. On one hand, the charger component power ratings may need to be further boosted, as indicated in Eqs. (20) and (21). On the other hand, more heat may be generated within the supercapacitor. Yet, the thermal characteristics of supercapacitors involve



(a)

(b)

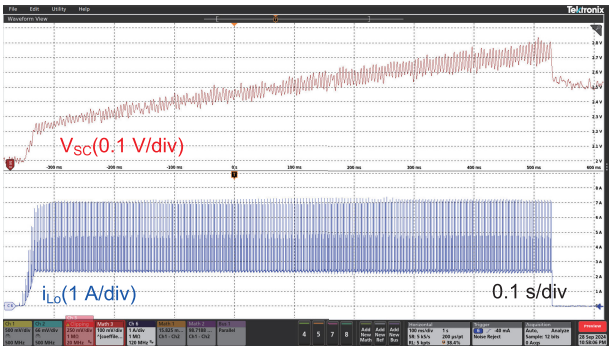
(c)

Fig. 9. Experimental setup. (a) Charger prototype: front view. (b) Charger prototype: back view. (c) Test setup.

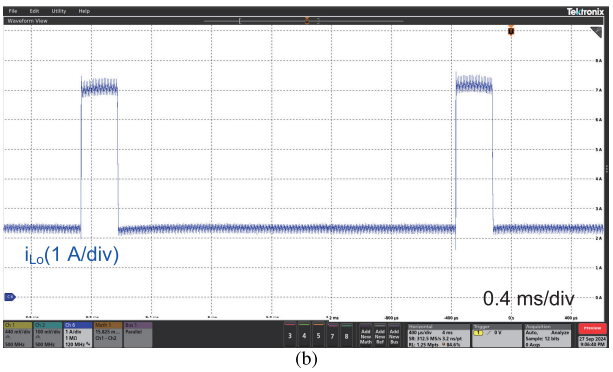
complex physical mechanisms that have not been completely revealed [54], [55]. Therefore, it is challenging to optimize the pulse period and width that lead to the shortest charging time while properly addressing the thermal management of the charger and the supercapacitor for the time being. This problem needs to be rigorously and systematically investigated as a future work.

As for the continuous and pulse currents, Fig. 10(b) zooms in the charging current when the prototype works steadily after the initial 25 ms of charging. The prototype generates a continuous current of 2.4 A and a pulse current of 7.1 A with the predefined pulse period of 2.5 ms and pulse width of 0.25 ms. The current ripples are 0.11 A at 2.4 A and 0.17 A at 7.1 A, respectively. The pulse characteristics are impressive. As listed in Table II, the pulse rising and falling times of the prototype are 2.1 μs and 7.2 μs, respectively. The pulse duration is approximately 0.24 ms.

While the key feature of the proposed charger is to incorporate the pulse current mode to accelerate the charging process



(a)



(b)

Fig. 10. Proposed charger: dual-mode operation. (a) Supercapacitor voltage and charging current during charging process. (b) Continuous and pulse currents.

TABLE II

PULSE CHARACTERISTICS OF PROPOSED CHARGER AND FORWARD CONVERTER

	Proposed Charger	Forward Converter
Rising time	2.1 μs	147 μs
Falling time	7.2 μs	103 μs
Peak current	7.1 A	6 A
Duration	0.24 ms	0 ms

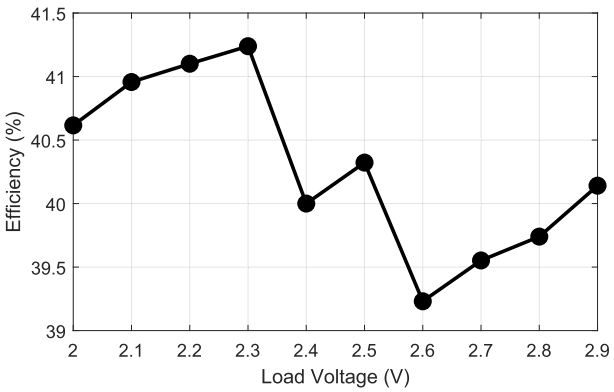


Fig. 11. Proposed charger: efficiency versus load voltage.

and its efficiency is not a major concern, Fig. 11 sweeps the efficiency of the prototype when the load voltage varies. Note that an electronic load instead of the supercapacitor is used to measure the efficiency. Clearly, the efficiency is around 40% when the load voltage changes from 2 to 2.9 V. The relatively low efficiency of the charger is mainly originated from three power losses. First, the power consumed by R_f. As indicated in Eq. (20), the power loss associated with

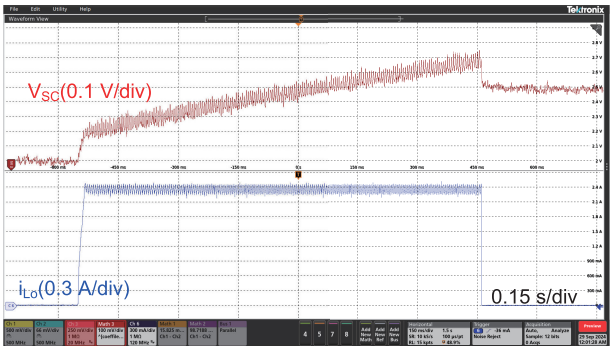


Fig. 12. Proposed charger: continuous current mode operation.

R_f is approximately constant during the charging process. Second, the conduction losses of D_3 and D_4. The supercapacitor voltage is relatively low and the forward voltages of D_3 and D_4 are comparable with the supercapacitor voltage. The charger efficiency can be estimated as

$$\eta = \frac{V_{SC}}{V_{SC} + V_D} \tag{24}$$

which suggests that as the supercapacitor voltage increases, the charger efficiency increases. Finally, the power losses associated with D_2 and R_r. When the supercapacitor voltage increases, the duty cycle of S_1 also increases. According to Eq. (21), the power losses associated with D_2 and R_r increase and the charger efficiency decreases. Given the competing effects of the three power losses on the charger efficiency, Fig. 11 shows that the charger efficiency first increases when the load voltage increases from 2 to 2.3 V, then decreases in general during 2.3-2.6 V, and finally increases again from 2.6 to 2.9 V. Note that although the charger efficiency is relatively low, there are certain applications in which a higher charging speed is more desirable than a higher efficiency such as surge-resistant uninterruptible power supplies [38], [56] and defense systems.

To illustrate the benefits of introducing the pulse current mode, the prototype is configured to operate in the continuous current mode only (i.e., the pulse current mode is disabled). Referring to the topology shown in Fig. 1, S_2 is turned off and S_3 is turned on in this configuration. For the control scheme shown in Fig. 8, the reference current I_{ref} is set as I_C. As shown in Fig. 12, the charging current is fixed at 2.4 A with a ripple of 0.13 A. The supercapacitor is charged from 2 to 2.5 V in 1 s. Using this charging time as the baseline, when the proposed charger operates in the dual-mode, the charging time is reduced by 13%: 0.87 versus 1 s.

As another comparison, Fig. 13 shows the dual-mode charging current generated by the proposed converter when it is configured to operate as a forward converter. Again, S_2 is turned off and S_3 is turned on. For the continuous current mode, I_{ref} is set as I_C. For the pulse current mode, a trial-and-error process is employed to set I_{ref} to ensure that the pulse width is equal to 0.25 ms. Specifically, I_{ref} is first set as I_P for a certain period of time and the current rises from I_C to a particular value, which may be lower than I_P. During this process, the rising edge of the pulse is generated. After that, I_{ref} is set as I_C and the current falls to I_C.

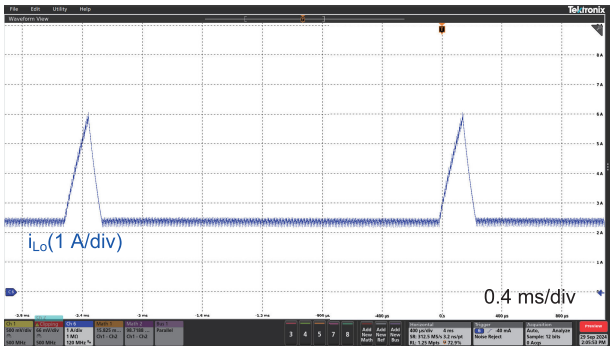


Fig. 13. Forward converter: continuous and pulse currents.

As shown in Fig. 13, within the predefined pulse width of 0.25 ms, the pulse indeed fails to reach the preset peak of 7.1 A. In fact, the maximum value of the current is only 6 A. Based on this maximum value, the pulse rising and falling times are determined as 147 μs and 103 μs, respectively. The pulse duration is therefore determined as 0 ms, as listed in Table II. In summary, these experimental results demonstrate the dual-mode operation and enhanced pulse characteristics of the proposed charger.

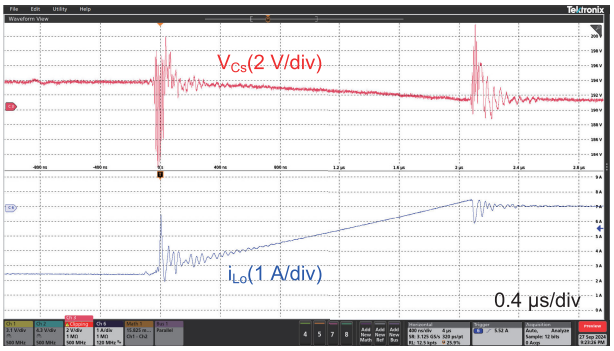
C. Pulse Rising Process

The pulse rising process of the proposed charger is elaborated in this section. As shown in Fig. 14(a), before the L_o current pulse rises, a high voltage of 194 V (i.e., around the Zener voltage V_Z in Table I) has been established across the energy storage capacitor C_s. During the pulse rising process, because C_s is large enough, the voltage across C_s only drops by about 2.4 V. Since the voltage across C_s is very high (i.e., approximately 194 V) and the voltage across the supercapacitor V_{SC} is relatively low (i.e., around 2 V), the L_o current ramps up quickly and leads to a sharp pulse rising edge, as indicated in Eq. (2). The pulse rising time is roughly 2.1 μs. In addition, Fig. 14(b) shows the voltage across L_o during the pulse rising process. Clearly, the L_o voltage is also high. For instance, the L_o voltage for the circled portion is approximately 190 V, which is close to the C_s voltage of 194 V.

For the forward converter, given the parameters in Table I, the L_o current ramping-up rate is much lower compared to that of the proposed charger. In fact, Fig. 15(a) shows the voltage across L_o during the pulse rising process for the forward converter, which is approximately 5.2 V. Therefore, Figs. 14 and 15(a) explain the significant difference between the pulse ramping-up rates of the proposed charger and the forward converter.

D. Pulse Falling Process

On the other hand, Fig. 16 shows the key waveforms during the pulse falling process for the proposed charger. In this case, the current through R_f generates a high voltage (i.e., approximately 100-40 V), which is applied to L_o and ultimately results in a sharp falling edge, as indicated in Eq. (4) and shown in Fig. 16(a).



(a)

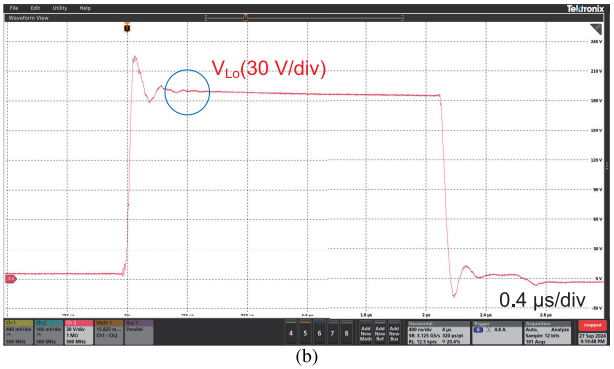


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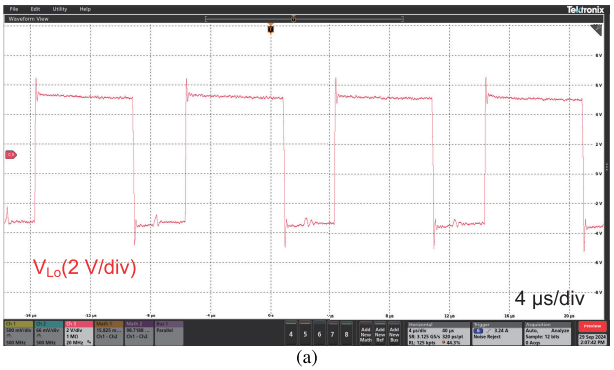
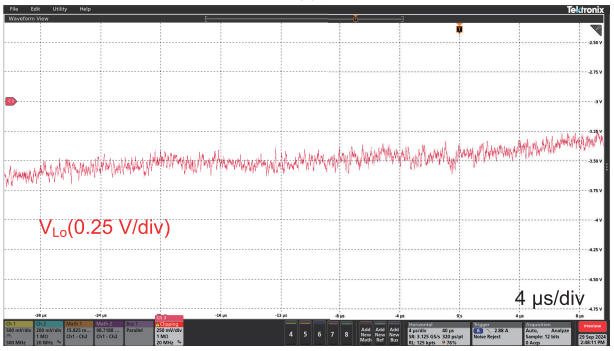
Fig. 14. Proposed charger: pulse rising process. (a) Voltage across C_s and current through L_o. (b) Voltage across L_o.



(a)



(b)

Fig. 15. Forward converter: voltage across L_o. (a) Pulse rising process. (b) Pulse falling process.

Based on the maximum value of 7.1 A and the minimum value of 2.4 A for the L_o current shown in Fig. 16(a), the pulse falling time is determined as 7.2 μs. In addition, Fig. 16(b) shows the voltage across L_o. For the two circled areas, the voltages are -105 and -26 V, respectively. Therefore, the proposed charger generates a sharp pulse falling edge.

TABLE III
COMPARISON OF PROPOSED CHARGER WITH OTHER CONVERTERS

Topologies	Number of Switches	Number of Diodes	Number of Transformers	Voltage Stress	Efficiency	Dynamic Response	Easy to Control
Proposed charger	3	4	1	High	Low	Fast	Yes
Buck	1	1	0	Medium	Medium	Medium	Yes
Full-bridge	4	4	1	Low	Medium	Medium	Yes
Half-bridge	2	2	1	Medium	Medium	Medium	Yes
[57]	4	10	1	Low	Medium	Medium	Yes
[58]	1	2	0	High	High	Medium	No
[59]	2	0	0	Medium	Medium	Medium	Yes
[60]	8	0	0	Medium	Medium	Medium	Yes

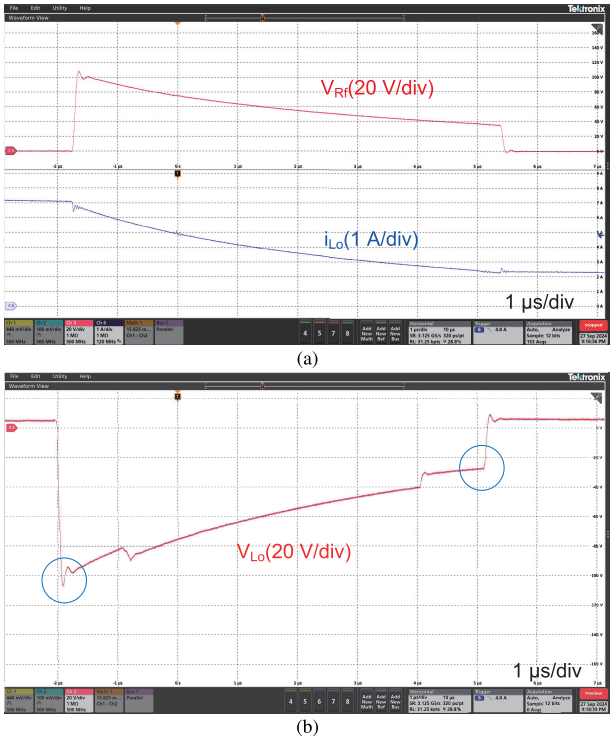


Fig. 16. Proposed charger: pulse falling process. (a) Voltage across R_f and current through L_o. (b) Voltage across L_o.

For the forward converter, Fig. 15(b) shows the voltage across L_o during the pulse falling process. Without the high voltage across R_f, the L_o current ramping-down rate is much lower compared to that of the proposed charger. The L_o voltage is about -3.5 V, which is much lower compared to Fig. 16(b). Ultimately, the proposed charger results in a much sharper pulse falling edge compared to the forward converter.

E. Comparison: Proposed Charger Versus Other Converters

Finally, to further evaluate the overall performance of the proposed charger, a comparison of the proposed charger with other converters is shown in Table III. Since the load (i.e., supercapacitor) of the charger is capacitive and constant current charging is needed, topologies requiring additional filter inductors such as LLC and boost converters are not considered in the comparison. Compared to buck, full-bridge, and half-bridge converters, the proposed charger has a much faster dynamic response at the cost of a lower energy efficiency. The proposed charger utilizes a DC power source to charge the supercapacitor while a charging system is developed to charge the supercapacitor directly from the power grid by including an AC/DC rectifier and a DC/DC boost converter [57]. By adding more components to a buck converter to achieve zero voltage switching (ZVS), a supercapacitor charger with a relatively high efficiency is developed [58]. While the proposed charger can only implement the unidirectional power flow from the DC power source to the supercapacitor, some bidirectional converters have been proposed for supercapacitors [59], [60]. In summary, while the efficiency of the proposed charger is relatively low, it takes advantage of the pulse current mode to accelerate the charging process, which may be well-suited in certain applications.

VI. CONCLUSION

This paper presents the analysis, design, implementation, and evaluation of a dual-mode fast charger for supercapacitors that utilizes both the continuous and fine-tuned pulse currents. The proposed charger is developed based on the conventional forward converter. By introducing an energy storage capacitor and a branch resistor, the rising and falling edges of the pulse current are much sharper in the proposed charger compared to those in the forward converter. Therefore, the transitions between the continuous and pulse current modes are significantly accelerated in the proposed charger, which ultimately shortens the supercapacitor charging time.

A prototype is built and tested using a 3 V/6 F supercapacitor. To charge the supercapacitor from 2 to 2.5 V, the proposed charger takes 0.87 and 1 s when it is configured to operate in the dual-mode and the continuous current mode only, respectively, which leads to a 13% reduction in the charging time. Compared to the forward converter, the proposed charger results in much faster transitions between the continuous and pulse current modes. The pulse rising and falling times for the proposed charger and the forward converter are 2.1 versus 147 μs and 7.2 versus 103 μs, respectively. These improvements in the pulse characteristics are originated from the topology modifications introduced in the proposed charger. In particular, the energy storage capacitor and the branch resistor build relatively high voltages, which are finally applied to the output inductor to accelerate the pulse rising and falling processes. In summary, this paper demonstrates the feasibility of developing dual-mode fast chargers for supercapacitors by utilizing both the continuous and pulse currents.

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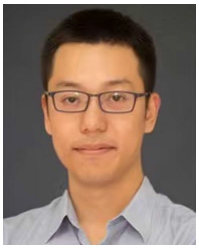

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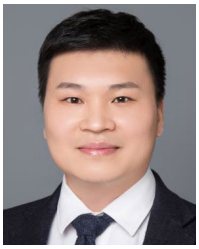

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