Letters

A Megahertz Synchronous Rectifier Based on Resonant Gate Drive

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***Abstract*—This article introduces a resonant gate-driven synchronous rectifier system for megahertz (MHz) wireless charger. The proposed design extracts synchronization signals directly from a voltage-sensing node within the compensated resonant tank, eliminating dedicated sensing circuits. The phase-tunable resonant gate driver concurrently enables sinusoidal gate excitation and phase compensation. Implemented in a 5 MHz prototype, the SR demonstrates 97.5% peak efficiency across a 10–50 Ω load range.**

***Index Terms*—Megahertz (MHz) synchronous rectifier, phase compensation, resonant gate drive, wireless charger.**

I. Introduction

THE rectification efficiency in resonant converter systems is governed by a complex interplay of operational parameters, encompassing operating frequency, power capacity, semiconductor characteristics, and topological design [1]. A representative case lies in wireless charger, where synchronous rectification (SR) has emerged as the dominant strategy for kHz-range power converters owing to its superior conduction loss suppression. Advanced implementations integrate soft-switching mechanisms to curtail switching losses [2], adaptive dead-time regulation to alleviate diode conduction during transient intervals [3], topology-dependent synchronization signal extraction for precision timing, and parasitic effect compensation circuits [4]. These innovations have solidified SR's dominance in medium/low-power kHz applications, supported by mature integrated circuit solutions.

Transitioning to MHz wireless charger reveals exacerbated efficiency limitations: Schottky diode rectifiers achieve peak efficiencies below 92%, while commercial SR implementations plateau at 93%, starkly underperforming relative to kHz counterparts. Critical inefficiencies arise from synchronization signal inaccuracies, dead-time diode conduction losses, and escalating transistor driving losses. Although centralized control architectures with shared synchronization signals have enabled SR operation beyond 10 MHz in academic prototypes, physically isolated wireless chargers necessitate receiver-side synchronization signal derivation through independent control frameworks, imposing stringent precision requirements. Existing methods for synchronous signal acquisition typically involve signals from drain-source voltage [5], [6], drain-source current [7], [8], [9], the receiver coil itself [10], and the optimal drain source voltage tracking method (ODSV) [11]. However, these approaches face challenges such as the significant influence of parasitic parameters at high frequencies or the requirement for additional sensors. Concurrently, resonant gate driving (RGD) technology has demonstrated potential to mitigate MHz driving losses [12], achieving 30 MHz operation in inverters via square-wave-to-resonant gate voltage conversion. Nevertheless, its application remains unexplored in MHz rectification scenarios.

This work presents a MHz SR leveraging RGD technology. By extracting synchronization signals directly from the receiver-side resonant tank node, the design eliminates transmitter–receiver coordination while ensuring circuit simplicity, noise immunity, and dynamic responsiveness. A comprehensive phase analysis quantifies the gate signal misalignment caused by frequency variations, power fluctuations, load dynamics, and parasitic elements. Two RGD parameters are systematically optimized to compensate for phase discrepancies and constrain gate voltage amplitudes. The proposed SR establishes an equilibrium among signal accuracy and gate waveform shaping, addressing a critical gap in high-frequency resonant converter.

II. High-Frequency Rectification

A. System Configuration

This article develops a SR, utilizing the RGD, which is designed to overcome conventionally associated challenges. Fig. 1(a) presents the actual circuit implementation, in which the blue section illustrates both the signal sensing and driving paths. Fig. 1(b) shows a simplified schematic of the entire SR system, divided into the power circuit (upper part) and the signal circuit (lower part). The series-compensated receiver (RX), integrated within a wireless charger, is utilized as the

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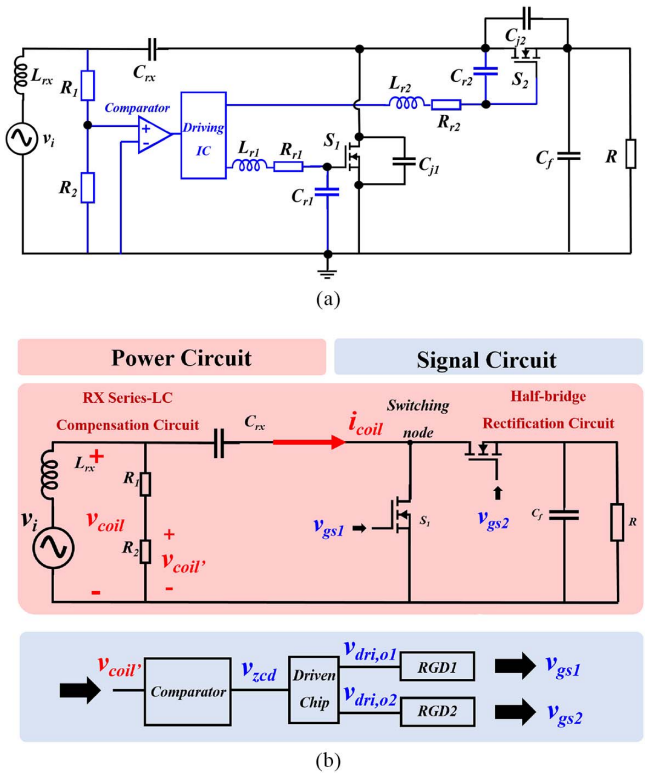

Fig. 1. Proposed SR. (a) Actual circuit. (b) Simplified block diagram.

example power stage to illustrate the operating mechanism of the SR's signal circuitry. This method eliminates the need for any signals from the transmitter (TX) side and yields a quick response, with broad applicability to various resonant converters. The resonant property of the LC tank allows the sensed signal to maintain low noise levels (unlike the device's drain-source voltage) and inherently provides resistance to high-frequency parasitic elements from the switching devices. A phase shift is present between the sensed voltage and the necessary gate driving signal, but the RGD can not only mitigate the driving loss but also make up for the phase difference caused by the signal detection circuit.

B. Phase Difference

The phase difference is illustrated in Fig. 2, and the driving logic for S1 is used as the example. As shown in Fig. 1, the coil voltage v_{coil} (used as the reference with zero phase) is detected by a voltage divider to produce v'_{coil}. This voltage is then compared with ground to generate a square wave signal v_{zcd}. It is important to note that the comparator introduces a relatively fixed phase delay between v'_{coil} and v_{zcd}. A commercial driving IC subsequently amplifies the square wave v_{zcd} to $v_{\text{dri,o1}}$, introducing an additional phase delay. The overall fixed delay of the comparator and driving IC is defined as ϕ_{chip} in Fig. 2. When the voltage supply of the driving chip is $V_{\text{dri,o}}$ (such as 5 V), the square wave $v_{\text{dri,o1}}$ is then shaped into a sinusoidal waveform v_{gs1} with a DC offset $0.5\,V_{\text{dri,o}}$ by the RGD path, consisting of inductance L_r, resistance R_r, and capacitance C_r. The RGD is

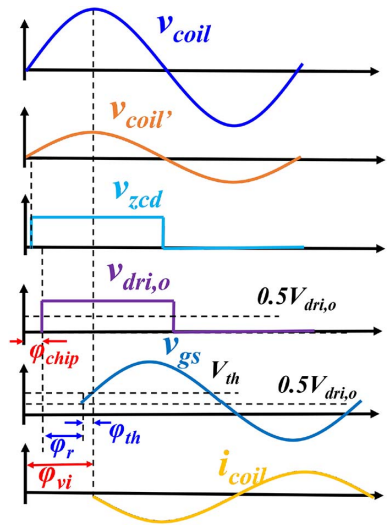

Fig. 2. Signal flow chart.

able to design the phase between $v_{\text{dri,o1}}$ and v_{gs1}, i.e., offering an adjustable ϕ_r.

The sinusoidal nature of the RGD signal introduces noninstantaneous turn-ON behavior in power switches. The GaN turns ON when the sinusoidal v_{gs1} exceeds the threshold voltage V_{th}, creating a fixed phase delay ϕ_{th}. When the desired v_{gs1} (with DC bias) is compared with the device threshold voltage v_{th} to turn ON the SR, the induced gate-source voltage of SR v_{ds} should be in phase with the coil current i_{coil}. The phase difference between v_{coil} and i_{coil}, denoted as ϕ_{vi}, directly influences the efficiency of the SR. According to the signal transfer path, the phase should follow the constrain below

$$\phi_{vi} = \phi_{\text{chip}} + \phi_r + \phi_{th}. \tag{1}$$

Considering the relatively fixed ϕ_{chip} and ϕ_{th}, ϕ_r should be tuned to meet (1). There are multiple factors influencing the phase difference ϕ_{vi}. When the coil L_{rx} is fully compensated by the capacitor C_{rx}, and the rectifier input impedance is modeled as $R + jX$, the coil current can be expressed as follows:

$$\boldsymbol{I}_{\text{coil}} = \boldsymbol{V_i}/(R + jX) \tag{2}$$

where R is defined in Fig. 1.

Accordingly, the voltage across the coil is given by

$$\boldsymbol{V}_{\text{coil}} = \boldsymbol{V_i} - j\omega L_{rx}\boldsymbol{I}_{\text{coil}}. \tag{3}$$

Define the voltage-to-current transfer function as follows:

$$\boldsymbol{G} = \boldsymbol{I}_{\text{coil}}/\boldsymbol{V}_{\text{coil}} = 1/[R + j(X - \omega L_{rx})] \tag{4}$$

then the phase difference ϕ_{vi} of Fig. 1 is derived as follows:

$$\phi_{vi} = 180^\circ - \arctan\left(\frac{\omega L_{rx} - X}{R}\right). \tag{5}$$

This implies that the load resistance (R), the diode junction capacitance (which influences X), and the tank parameters (such as L_{rx}) all have an impact on ϕ_{vi}. This phase behavior is illustrated through simulation in Fig. 3(b). As R decreases

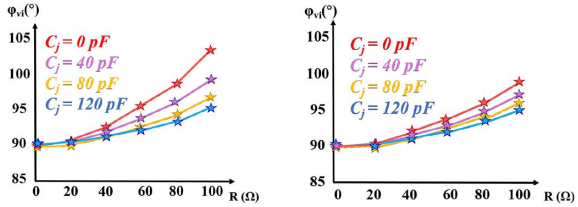

Fig. 3. Phase difference. (a) $L_{rx} = 2\ \mu H$, $C_{rx} = 500\ pF$. (b) $L_{rx} = 5\ \mu H$, $C_{rx} = 200\ pF$.

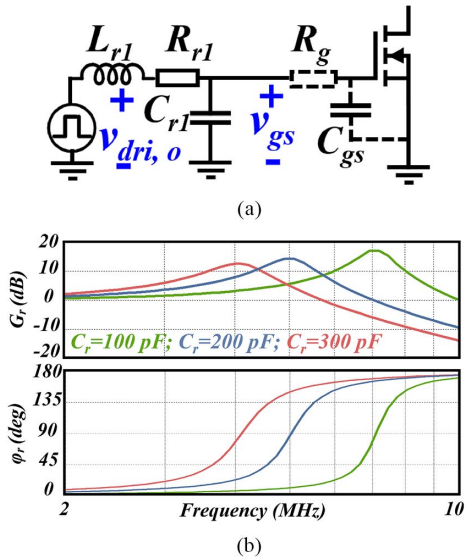

Fig. 4. RGD. (a) Topology. (b) G_r and ϕ_r.

toward zero, ϕ_{vi} tends toward 90°. Furthermore, as the junction capacitance C_j increases, the reactance X becomes more negative, which in turn decreases the phase. Since the proposed driving method is specifically tailored to a fixed power stage, variations in inductance do not need to be considered.

C. Design of RGD

The well-known RGD utilizes sinusoidal excitation to partially recycle the driving energy. As illustrated in Fig. 4(a), the gate signal is denoted by v_{gs1}, with an internal resistance R_g and a gate capacitance C_{gs}. Usually the driving loop would include a external LC loop, i.e., L_{r1} and C_{r1}, to shape the square $v_{\mathrm{dir},o1}$ to a sinusoidal v_{gs1}. The corresponding gate driving loss can be expressed as follows:

$$P_{\mathrm{dri}} = \left(\frac{V_M/\sqrt{2}}{1/2\pi f(C_{r1} + C_{gs1})} \right)^2 \times R_{r1} \tag{6}$$

where V_M denotes the amplitude of v_{gs1}.

Unlike the classical RGD, an additional driving resistance R_r is introduced to address the variation issues of ϕ_{vi}, as discussed in Fig. 3. This modification slightly increases the driving losses.

TABLE I
PARAMATERS OF POWER CIRCUIT AND SIGNAL CIRCUIT

$V_{gs,\max}$	V_{th}	R_g	C_{gs}
15 V	2.1 V	150 $m\Omega$	50 pF
L_{rx}	C_{rx}	C_j	ϕ_{chip}
5 μH	200 pF	27 pF	22.5°

The voltage gain of the RGD, i.e., from $v_{\mathrm{dri},o1}$ to v_{gs1}, can be derived as follows:

$$G_r = \left| \frac{\boldsymbol{V_{gs1}}}{\boldsymbol{V_{dri,o1}}} \right| = \left| \frac{1 + j\omega R_{r1} C_{r1}}{1 - L_{r1} C_{r1} \omega^2 + j\omega R_{r1} C_{r1}} \right|. \tag{7}$$

The defined ϕ_r of Fig. 2 is the absolute value of the voltage gain's phase, can be derived as follows:

$$\phi_r = \left| \arctan\left(\frac{-L_{r1} C_{r1}^2 R_{r1} \omega^3}{1 - L_{r1} C_{r1} \omega^2 + (R_{r1} C_{r1} \omega)^2} \right) \right|. \tag{8}$$

This expression reveals the potential to adjust ϕ_r by tuning the parameters L_{r1}, C_{r1} and R_{r1} to meet the phase demand of Fig. 2. For a given L_{r1} and R_{r1}, G_r and ϕ_r is shown in Fig. 4(b). Its low-pass feature is able to offer sufficient gain and required phase by parameter design.

The RGD should be designed to operate at a fixed frequency. An example system is used to demonstrate the design process, with the circuit parameters provided in Table I. The goal is to design C_{r1} and R_{r1} in such a way that they enable a load variation within the range of $[R_{\min}, R_{\max}]$. It is important to note that fine-tuning L_r is not practical, so it is fixed at 5 μH. G_r and ϕ_r are shown in Fig. 5 when sweeping C_r and R_r. When the condition $v_{gs1} + 0.5\,V_{\mathrm{dri},o1} > V_{th}$ is satisfied, the SR can be activated; however, $v_{gs1} + 0.5\,V_{\mathrm{dri},o1}$ must also remain below the maximum gate-source voltage of the chosen device, $V_{gs,\max}$. These two conditions define the minimum and maximum gain for G_r, as depicted in Fig. 5(a). When an operating point A is selected, whose magnitude gain defines a fixed-length conduction window. This nonideal SR conduction window defines a permissible phase shift range, represented by $\phi_{r,\min}$ to $\phi_{r,\min}$. Any minor perturbations caused by parameter variations are contained within the stable operating region, thereby ensuring system robustness and preventing operational failure. Once the potential parameter variation is too large, it should reselect Point A by lowering the magnitude in Fig. 5(a), and it would directly lead to a larger safety margin in Fig. 5(b).

In the region shown in Fig. 5, an example design point A is used to illustrate the wide-load operation mechanism. Fig. 6 demonstrates the influence of R. In both load conditions, v_{coil} is used as the reference. The duty cycle of the SR, D_{sr}, is always kept below 0.5. The resulting ϕ_r (i.e., point A) ensures the waveform shown in Fig. 6(a) serves as the operational boundary, which helps define $R_{\min}$ for the selected point A. As R increases, ϕ_{vi} increases as well, and a new load boundary is defined by $R_{\max}$. According to (5), the load-dependent ϕ_{vi}

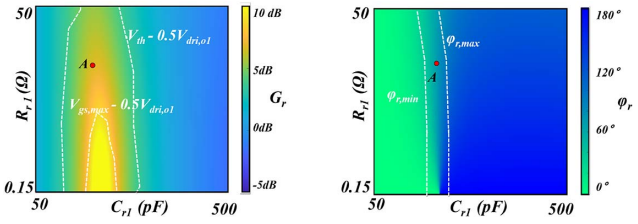

Fig. 5. Gain with different C_{r1} and R_{r1}. (a) Magnitude. (b) Phase.

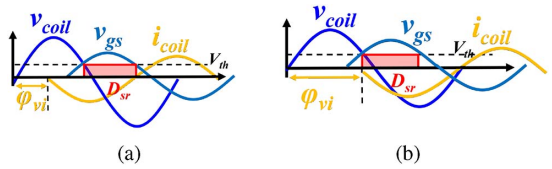

Fig. 6. Phase move of ϕ_{vi} with increasing R. (a) $R_{\min}$. (b) $R_{\max}$.

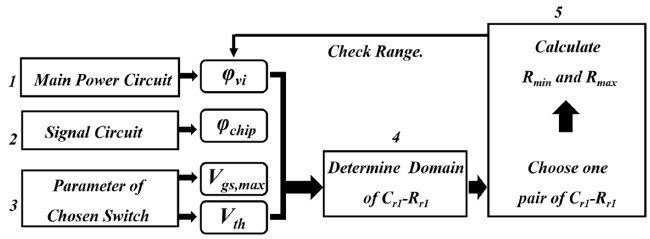

Fig. 7. Design guiding flow chart.

could help derive $R_{\min}$ and $R_{\max}$ as follows:

$$R_{\max} = \frac{\omega L_{rx} - X}{\tan(\pi - \phi_{vi,\max})}, R_{\min} = \frac{\omega L_{rx} - X}{\tan(\pi - \phi_{vi,\min})} \quad (9)$$

where $\phi_{vi,\max}(= \phi_r + (\pi - \pi D_{sr})/2)$, $\phi_{vi,\min}(= \phi_r - (\pi - \pi D_{sr})/2)$ are the maximum and minimun of the ϕ_{vi} which can allow the SR conduct without error. D_{sr} and the permissible phase shift tolerance $\Delta\phi_r$ can be designed respectively according to (10), (11) below

$$D_{sr} = \frac{\pi - \arcsin\left(\frac{2V_{th}}{v_{\text{dri},o}} - 1\right)}{2\pi G_r} \quad (10)$$

$$\Delta\phi_r = 0.5\pi(1 - D_{sr}). \quad (11)$$

It means the red conduction window of Fig. 6 should not move outside the safety region defined by i_{coil}. Within this range, the SR can still conduct positive current. When the SR is off but the corresponding diode should be on, a Schottky diode can be added in parallel to ensure that the bottom switch conducts for a full half-cycle.

A step-by-step design flow is illustrated in Fig. 7. The objective is to determine the values of L_{r1}, C_{r1}, and R_r to ensure wide-load operation, given known chip and transistor specifications.

1) For a fixed load within the range $[R_{\min}, R_{\max}]$, such as the average value $0.5(R_{\max} + R_{\min})$, the load-dependent phase ϕ_{vi} can be calculated accordding to (5).

TABLE II
PARAMETER OF POINT A AND THE LOAD RANGE

L_{r1}, L_{r2}	C_{r1}, C_{r2}	R_{r1}, R_{r2}	ϕ_r	ϕ_{chip}	R
5 μH	150 pF	30 Ω	68.5°	22.5°	10–50 Ω

2) The signal circuit is used to determine ϕ_{chip}.
3) The parateters of the transistor used to determine $V_{gs,\max}$ and V_{th}.
4) For a given L_{r1}, a feasible design domain for C_{r1} and R_{r1} can be identified, as illustrated in Fig. 5.
5) Each design point corresponds to a specific load range $[R_{\min}, R_{\max}]$, as shown in Fig. 6. It is then necessary to verify whether the obtained load range meets or exceeds the target range. If it does, the design is considered successful. Ideally, the achieved load range should exactly match the target specification.

According to (7), increasing R_r woud decrease G_r, and lead to the drop of D_{sr}. And a small D_{sr} is able to extend the load range, but the penatily is the increased conduction loss and driving loss. Therefore, the proposed RGD needs to make a trade off between the load range and SR efficiency. The parameter of Point A and its acheived load range is shown in Table II.

D. Trade Off Between Robustness and Efficiency

In this design, the load resistance is treated as a variable parameter, which inherently impacts the transfer function of the SR driving signal. Additionally, the gate capacitance of the transistor—being nonlinear and sensitive to process and temperature variations—introduces another source of uncertainty that affects the signal transfer characteristics. However, in the considered example, an external gate capacitance of approximately 150 pF is employed, which is significantly larger than the variation range of the intrinsic gate capacitance (around 10 pF). Therefore, the nonlinear effect of the gate capacitance can be neglected in the RGD design.

The proposed SR design does not primarily target the minimization of conduction loss under nominal conditions. For instance, as shown in Fig. 6, the conduction window of the SR is not maximized. Instead, the design parameters are selected such that the SR maintains reliable operation under varying load conditions and other parasitic variations. This reflects a deliberate trade-off between robustness and efficiency.

Based on the SR's operation in Fig. 6, the driving loss P_{dri} and the conduction loss P_{con} of GaN can be derived as follows:

$$P_{\text{dri}} = \left(\frac{V_M/\sqrt{2}}{1/2\pi f(C_{gs} + C_{r1})}\right)^2 R_{r1} = 2\pi^2(C_{r1} + C_{gs})^2 V_M^2 f^2 R_{r1} \quad (12)$$

$$P_{\text{con}} = \int_{t_0}^{t_1} i_{\text{coil}}^2 R_b dt + \int_{t_1}^{t_2} i_{\text{coil}}^2 R_{ds} dt + \int_{t_2}^{t_3} i_{\text{coil}}^2 R_b dt \quad (13)$$

where R_b is the resistance of the body diode of GaN and R_{ds} is its conduction resistance. $t_1 - t_2$ is the on time of GaN and

TABLE III
COMPARISON OF THE PROPOSED AND CONVENTIONAL METHOD

	Extra Component	Low Parasitic Parameter (MHz)	No Comparator	Phase Modulation
Proposed	No	✔	✘	✔
[5], [6]	No	✘	✘	✘
[7], [8], [9]	Sensor	✘	✘	✘
[10]	Sensor and auxiliary winding	✔	✔	✘
[11]	No	✘	✘	✘

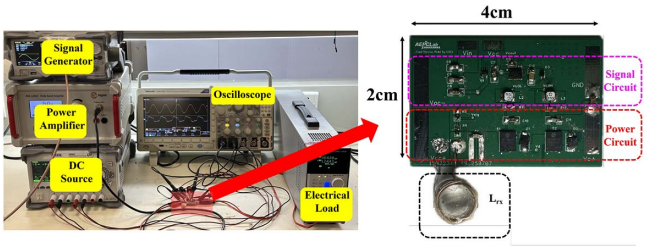

Fig. 8. Experiment platform.

$t_0 - t_1, t_2 - t_3$ is the on time of its body diode. Moreover, since the designed resistance R_{r1} is significantly larger than the switch's gate resistance R_g (which is on the order of $m\Omega$), the influence of R_g can be neglected in the loss calculation.

Table III provides a comparative discussion regarding gate drive complexity versus conventional approaches. Conventional SR schemes typically require additional sensors or auxiliary windings, whereas the comparator introduced in this design is significantly more compact than these components. This approach effectively overcomes the challenge of severely degraded signal extraction accuracy caused by switching parasitic parameters at MHz. Furthermore, the incorporation of the RGD circuit provides superior phase modulation capability and time delay compensation in the signal circuit.

III. EXPERIMENTAL VERIFICATION

The experimental setup is depicted in Fig. 8. A 5 MHz, 10 V square wave was generated by the signal generator, amplified by the power amplifier, and then fed into a half-bridge rectifier through an LC resonant tank. Under different load conditions, the DC output voltage ripple is maintained below 1% of the nominal value. To synchronize the rectification process, v_{coil} is sensed using a voltage divider and fed into a TLV3601 high-speed comparator, which generates a 5 V square-wave reference. This square wave is subsequently amplified by an LMG1210 gate driver IC. Rather than directly driving the lower SR (YHJ-65H225), the amplified signal is filtered through an LRC-based RGD. The diode NRVTSS5100E is used in the passive rectification for comparison. As shown in Fig. 3, all the delays from the chip, main circuit, and RGD are provided in Table II.

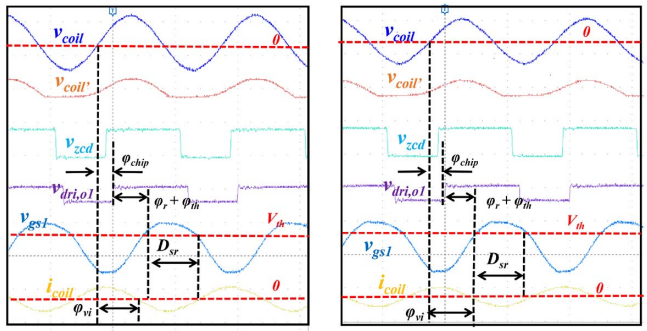

Fig. 9. Waveforms of v_{coil}, v'_{coil}, v_{zcd}, $v_{dri,o1}$, v_{gs1}, i_{coil}. (a) $R = 10\ \Omega$; output: 5 V, 0.5 A. (b) $R = 50\ \Omega$; output: 15 V, 0.3 A.

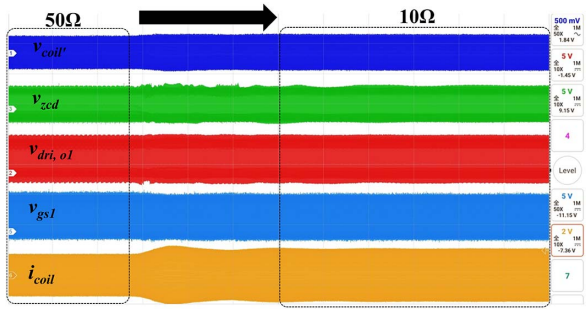

Fig. 10. Waveforms during load transient.

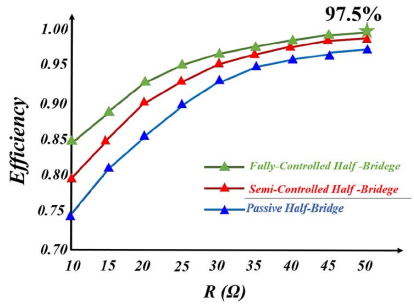

Fig. 11. Efficiency comparison of rectifier in wide load range.

To simplify the validation process, this article adopts a semi-controlled rectification scheme. Fig. 9 presents the key waveform of the proposed RGD circuit. As R varies from 10 to 50 Ω, ϕ_{vi} increases from 90° to 93°. The designed ϕ_r results in a D_{sr} of 6° degrees, which effectively handles the load variation. Fig. 10 illustrates the transient response of the system under load step conditions. It can be observed that even when the load undergoes an immediate step from maximum to minimum, the system rapidly recovers to a steady state and maintains stable synchronous rectification performance.

The efficiencies of three rectifier configurations—namely, a passive rectifier, a semicontrolled rectifier, and a fully-controlled rectifier—are compared in Fig. 11. Across the load range of 10–50 Ω, the proposed SR scheme demonstrates notable efficiency improvements. It achieves a peak efficiency of 97.5% at a 50 Ω load. The improvement is particularly significant under low-resistance conditions, with an efficiency gain of approximately 10% observed at a 10 Ω load.

TABLE IV
COMPARISON WITH OTHER SR SOLUTIONS

Ref.	Topology	f_s (MHz)	Extra Device	V_o (V)	R_o (Ω)	RGD	Eff. (%)
[11]	Class E	6.78	No	24	48	No	97.0
[16]	Full-bridge	6.78	No	24	96	No	97.2
[15]	Class E	13.56	No	40	63	No	93.0
[13]	Full-bridge	1	1*Coil	12	0.8	Yes	96.1
[14]	Full-bridge	1	4*MOS	1	0.005	Yes	92
Proposed	Half-bridge	5	No	15	50	Yes	97.5

Table IV compares the proposed method with state-of-the-art solutions. While [13] and [14] demonstrate significantly higher power capabilities, they are limited to 1 MHz and require complex auxiliary structures. Conversely, although non-RGD designs such as [15] reach higher frequencies (13.56 MHz), they exhibit lower efficiency (93.0%). The proposed method, while verified at a prototype power level, achieves a competitive peak efficiency of 97.5% and successfully extends simplified RGD operation to 5 MHz. This represents a favorable trade-off between structural complexity, operating frequency, and conversion efficiency.

IV. CONCLUSION

This article extends the RGD technique to a MHz SR. Using an example series resonant tank, the tank node voltage is selected to ensure low-noise signal sensing. Various phase propagation delays are examined, and their load sensitivities are studied. The well-known LC-based RGD is employed, with an additional resistor included to design the duty cycle of the SR, which further facilitates wide-load operation. Finally, a semicontrolled half-bridge rectifier and a fully-controlled one are constructed to demonstrate the reduction in conduction loss and the capability for wide-load operation.

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