A Resonant Switched-Capacitor LLC DCX in Data Center Applications

Jiawei Liang, Haoyu Wang
School of Information Science and Technology
ShanghaiTech University, Shanghai, China
wanghy@shanghaitech.edu.cn

Abstract—In this paper, a novel resonant switched-capacitor LLC topology is proposed to serve as the dc transformer (DCX) in data center applications. The proposed DCX is formed by a 2:1 resonant switched-capacitor cell and an LLC converter. To achieve a 4:1 voltage step-down ratio, only an n:1 turns ratio transformer is required. It presents good soft-charging and soft-switching performances to effectively mitigate charge distribution loss and switching loss. Furthermore, the voltage stresses of primary switches are only half of the input voltage, and the current stresses are also lower than that of conventional LLC converter. The operational principle of steady-state circuit and theoretical analysis are provided to highlight its advantages. To verify the proposed concept, a 300W-rated hardware prototype that converts 48 V to 12 V is designed and tested with 1MHz switching frequency.

Keywords—dc transformer, LLC, soft switching, switched-capacitor converter, voltage regulator modules

I. INTRODUCTION

The rapid evolution of various networking applications, such as cloud computing, Internet of Things (IoT), artificial intelligence, and mobile communication, has resulted in a significant surge in power consumption demands for data centers [1]. As a result of the growing electricity demand, there is a shift from the conventional 12V bus architecture to a more advanced 48V bus architecture in data centers to achieve higher efficiency and power density [2], [3]. However, a new challenge emerging from 48V bus is the optimal design of load-side voltage regulator modules (VRMs).

For the 48V VRM, two-stage intermediate bus architecture (IBA) [4] is a prevalent approach due to its superior deployment flexibility and transient performance [5]. This structure utilizes an intermediate bus converter (IBC) in the front end to convert the bus voltage (40V-60V) to an intermediate voltage (5V-12V), and a point-of-load (PoL) converter [6] is employed in the back end to provide final step-down and regulation function for terminal loads. For the front-end IBC, voltage regulation is not mandatory. Thus, the IBC is generally operated as a dc transformer (DCX) to improve performance in efficiency and power density.

Various topologies are suitable for IBCs including switched-capacitor-based solutions and transformer-based solutions [7]. For switched-capacitor-based solutions, switched capacitor converters (SCCs) [8] offer significant advantages in achieving high efficiency and power density due to less magnetics utilization. Moreover, resonant SCC [9]–[11] can further improve the efficiency by incorporating small inductors into the SCC to eliminate the charge redistribution losses. Alternatively, some transformer-based solutions are also potential candidates for DCX, especially in handling high voltage conversion ratios. Among them, LLC DCX [12]–[14] has been regarded as a selection for high-efficiency operation due to its excellent soft-switching characteristics.

This work was supported in part by the National Natural Science Foundation of China under Grant 52077140.

In this paper, a hybrid DCX topology based on resonant switched capacitor converter and LLC converter is proposed to further improve the DCX’s performance. The proposed DCX combines resonant switched-capacitor (RSC) cell with LLC converter by sharing a half-bridge structure. It can achieve a 4:1 voltage conversion ratio with an n:1 turns ratio transformer. Furthermore, the voltage stress on primary switches is only half of that in conventional LLC design, while maintaining lower current stresses at a lower turns ratio. The soft-charging and soft switching features are also achieved in...
the proposed DCX. Basic converter operation is analyzed to depict the concept. A 48V-to-12V converter prototype is built and tested to verify the theoretical analysis.

II. OPERATIONAL PRINCIPLE AND ANALYSIS

A. Proposed Topology and Operating Principle

Fig. 1 shows the schematic of the proposed resonant switched-capacitor LLC DCX with 4:1 conversion ratio. It combines a 2:1 resonant switched-capacitor cell and a half-bridge LLC cell by merging a half-bridge structure. There are four switches with two pairs of complementary gate signals, among which the gate signals of $Q_1, Q_2$ are one pair, and the signals of $Q_3, Q_4$ are the other pair. Both of them have a duty cycle of 50% with certain dead time. The resonant frequency of the resonant tank 2 (RT2) is designed to match the switching frequency so that the LLC cell can achieve optimal efficiency. Depending on a small phase-shift between two pairs of gate signals, all primary switches have the potential to achieve ZVS. To ensure full ZVS, the resonant frequency of the resonant tank 1 (RT1) should be slightly lower than switching frequency to store sufficient energy in $L_1$ during switching transition.

The circuit operation can be divided into eight modes, and the key waveforms are illustrated in Fig. 2. $G_{1,4}$ are the gate signals of $Q_{1,4}, V_{ds(Q_{1,4})}$ represent the drain-to-source voltages of $Q_{1,4}, V_{C1}$ and $v_{L1}$ are the voltages of $C_1$ and $L_1$, $i_{L1}$ represents the resonant current of $L_1$, $i_{Lr}$ and $i_{Lm}$ are the resonant current and magnetizing current in RT2, and the output current is denoted as $i_o$. The corresponding equivalent circuits are shown in Fig. 3. The positive current direction and voltage polarity denoted in Fig. 1. To simplify the analysis, the output parasitic capacitance $C_{oC}$ of the primary switches is assumed to be identical and linear. Due to the operational symmetry, only half switching cycle with four modes are detailed.

Mode 1 ($t_0$-$t_1$): At $t=t_0$, the output capacitor of $Q_1$ and $Q_4$ have already been fully charged and discharged, resulting in the ZVS turn-on of $Q_3$. The corresponding equivalent circuit is illustrated in Fig. 3(a). The output current $i_o$ freewheels through SR2, and the voltage of $L_m$ is clamped by $-V_o$. This interval ends when $i_o$ reaches zero.

Mode 2 ($t_1$-$t_2$): At $t=t_1$, $i_o$ becomes positive, and the equivalent circuit is shown in Fig. 3 (b). The input voltage source $V_i$ charges RT1, RT2, and the output load, while the middle non-resonant capacitor $C_{mid}$ also charges RT2 and the
output load. As a result, the current $i_{L1}$ is the sum of $i_{L1}$ and $i_{Cmid}$; $i_{Lm}$ increases linearly from negative to positive.

Mode 3 ($t_2$-$t_3$): At $t=t_2$, $Q_1$ turns off, and the equivalent circuit is shown in Fig. 3(c). $i_{L1}$ charges and discharges the $C_{oss}$ of $Q_1$ and $Q_2$ until the $C_{oss}$ of $Q_3$ is fully discharged and its body diode conducts, enabling ZVS turn-on of $Q_4$.

Mode 4 ($t_3$-$t_4$): In this interval, the equivalent circuit is shown in Fig. 3(d). $Q_2$ turns on with ZVS, and $Q_3$ is turned off. The resonant current $i_{L1}$ is clamped by $i_{Lm}$, and the difference between $i_{L1}$ and $i_{Lm}$ charges and discharges the $C_{oss}$ of $Q_3$ and $Q_4$ until the $C_{oss}$ of $Q_2$ is fully discharged and its body diode conducts. It enables ZVS turn-on of $Q_4$.

B. ZVS Analysis

During one switching cycle, there are four deadbands, which correspond to Mode 3, Mode 4, Mode 7, and Mode 8. For $Q_1$ and $Q_2$, ZVS is achieved by utilizing the energy stored in $L_1$. However, the ZVS condition of $Q_1$ and $Q_2$ is dependent on the difference current between $i_{L1}$ and $i_{Lm}$. Therefore, two situations should be analyzed to estimate the dead times for different switches.

1) The dead time of $Q_1$ and $Q_2$ can be denoted as $t_{d1}$, and the ZVS condition can be expressed by the inequality:

$$\frac{1}{2} L_1 i_{L1,0}^2 \geq C_{oss} V_{ds}^2$$

where $i_{L1,0}$ represents the current flowing through $L_1$ at the beginning of the dead time, and $V_{ds}$ is the drain-to-source voltage of switch. It is important to note that all primary-side switches have identical $C_{oss}$ and $V_{ds}$, and the $V_{ds}$ value is equal to $V_{in}/2$.

To estimate the minimum dead time $t_{d1}$ for $Q_1$ and $Q_2$, Mode 3 is used as an example. In this case, $v_{C1}$ is assumed to remain constant during the short dead time and is approximately equal to $V_{mid}$. Moreover, the energy stored in $L_1$ is assumed to be precisely enough to fully charge and discharge the $C_{oss}$ of $Q_1$ and $Q_2$. The state equations can be expressed as follows:

$$\begin{align*}
v_{d_{b2}} &= v_{C1} + v_{L1} \\
v_{L1} &= L_1 \frac{di_{L1}}{dt} \\
i_{L1} &= -2C_{oss} \frac{dv_{d_{b2}}}{dt}
\end{align*}$$

with the initial state

$$\begin{align*}
v_{C1} &= V_{mid} \\
v_{d_{b2}}(t_2) &= \frac{V}{2} \\
i_{L1}(t_2) &= i_{L1,0}
\end{align*}$$

Thus, the expressions of $v_{d_{b2}}$ and $i_{L1}$ can be calculated as:

$$\begin{align*}
v_{d_{b2}}(t) &= \frac{V}{2} - I_{L1,0} Z_0 \sin(\omega_b t - t_2) \\
i_{L1}(t) &= I_{L1,0} \cos(\omega_b t - t_2)
\end{align*}$$

where

$$\omega_b = \sqrt{\frac{2C_{oss} L_1}{L_1}}.$$  \hspace{1cm} (5)

Since $v_{d_{b2}}(t)+v_{d_{b2}}(t)=V_{mid} = V_{in}/2$, two trajectories during Mode 3 can be derived:

$$\begin{align*}
\left[ v_{d_{b2}}(t) + \frac{V}{2} \right]^2 &+ [i_{L1}(t) Z_0]^2 = (I_{L1,0} Z_0)^2 \\
\left[ v_{d_{b2}}(t) - \frac{V}{2} \right]^2 &+ [i_{L1}(t) Z_0]^2 = (I_{L1,0} Z_0)^2.
\end{align*}$$

Fig. 4(a) and (b) illustrate the complete trajectories of $i_{L1} Z_0$ with respect to $v_{d_{b2}}(t)$ and $v_{d_{b2}}(t)$. The minimum dead time $t_{d1}$ necessary to achieve ZVS must satisfy the following inequality:

$$t_{d1} \geq \frac{\pi}{2} \frac{1}{\omega_b}. $$

2) For $Q_3$ and $Q_4$, the difference current between $i_{Lm}$ and $i_{L1}$ is responsible for charging and discharging the output capacitance, and the dead time can be denoted as $t_{d2}$. Mode 4 is used as an example to estimate the minimum $t_{d2}$. During this mode, $L_{in}$ can be considered constant, and $I_{L1,1}$ represents the value of $i_{L1}$ at $t=t_3$. Using the same derivation method, the expressions of $v_{d_{b3}}$ and $i_{L1}$ can be calculated as:

$$\begin{align*}
v_{d_{b3}}(t) &= \frac{V}{2} \left[ 1 - \cos(\omega_b(t-t_1)) \right] - (I_{L1,1} - I_{Lm}) Z_0 \sin(\omega_b(t-t_1)) \\
i_{L1}(t) &= I_{Lm} + (I_{L1,1} - I_{Lm}) \cos(\omega_b(t-t_1)) - \frac{V}{2 Z_0} \sin(\omega_b(t-t_1))
\end{align*}$$

Since $v_{d_{b3}}(t)+v_{d_{b3}}(t)=V_{mid} = V_{in}/2$, two trajectories during Mode 4 can be derived:
The current stress on the switches is determined by the voltage across the capacitors. In the RSC cell with 2:1 voltage conversion ratio, the DC components of both \( v_{\text{mid}} \) and \( v_{\text{RTI}} \) are equal to \( V_{\text{n}}/2 \), thereby yielding an equivalent voltage stress of \( V_{\text{n}}/2 \) on switched \( Q_{1,4} \).

The current stress on the switches is determined by the currents \( i_{L_1}, i_{\text{mid}} \) and \( i_{L_2} \). To simplify the analysis, the dead time during switching transition is neglected. The further simplified equivalent circuits are shown in Fig. 5. Thus, the relationships between these currents are satisfied as follows:

\[
\begin{align*}
(i_{\text{mid}} &= i_{L_2} - i_{L_1}, \quad \text{in Mode 1,2} \\
(i_{\text{mid}} &= i_{L_1} - i_{L_2}, \quad \text{in Mode 5,6} .
\end{align*}
\]

Since the durations of Mode 1,2 and Mode 5,6 are both 50% of the switching period without dead time, \( i_{L_1} \) and \( i_{\text{mid}} \) can be approximated as nearly equal to \( i_{L_2}/2 \). By analyzing the current flow through the switches, it becomes evident that the current stresses of switches \( Q_{1,4} \) are all equal to \( i_{L_2}/2 \).

Table I compares the electrical rating between the proposed converter and conventional LLC converter. It indicates that the voltage and current stresses of the primary-side switches in the proposed converter are both lower than that of conventional LLC converter.

### Electrical Rating Analysis

The switch voltage rating is established based on the voltage across the capacitors. In the RSC cell with 2:1 voltage conversion ratio, the DC components of both \( v_{\text{mid}} \) and \( v_{\text{RTI}} \) are equal to \( V_{\text{n}}/2 \), thereby yielding an equivalent voltage stress of \( V_{\text{n}}/2 \) on switched \( Q_{1,4} \).

The current stress on the switches is determined by the currents \( i_{L_1}, i_{\text{mid}} \) and \( i_{L_2} \). To simplify the analysis, the dead time during switching transition is neglected. The further simplified equivalent circuits are shown in Fig. 5. Thus, the relationships between these currents are satisfied as follows:

\[
\begin{align*}
(i_{\text{mid}} &= i_{L_2} - i_{L_1}, \quad \text{in Mode 1,2} \\
(i_{\text{mid}} &= i_{L_1} - i_{L_2}, \quad \text{in Mode 5,6} .
\end{align*}
\]

Since the durations of Mode 1,2 and Mode 5,6 are both 50% of the switching period without dead time, \( i_{L_1} \) and \( i_{\text{mid}} \) can be approximated as nearly equal to \( i_{L_2}/2 \). By analyzing the current flow through the switches, it becomes evident that the current stresses of switches \( Q_{1,4} \) are all equal to \( i_{L_2}/2 \).

Table I compares the electrical rating between the proposed converter and conventional LLC converter. It indicates that the voltage and current stresses of the primary-side switches in the proposed converter are both lower than that of conventional LLC converter.

### III. EXPERIMENTAL VERIFICATION

To verify the operational concept of the proposed topology, a hardware prototype operating at 1 MHz was constructed. The prototype features a 48V input and produces a 12V/25A output. To achieve a compact magnetic profile, a planar transformer was specifically designed for this purpose. Moreover, the leakage inductance of the transformer can be utilized as the resonant inductance \( L_r \) offering the additional advantage of improving the overall power density of the transformer.

The key parameters related to the experimental setup are summarized in Table II, while the corresponding experimental results are depicted in Fig. 6. The waveforms of the drain-to-source voltage \( v_{\text{ds}} \), and the gate-to-source voltage \( v_{\text{gs}} \) of \( Q_{2,4} \) at 80% load are captured in Fig. 6(a) and Fig. 6(b), respectively. These waveforms effectively demonstrate that the ZVS operation is successfully achieved for both switches. Based on the symmetrical operations, it can be deduced that ZVS operation is also achieved for \( Q_{1,3} \). Furthermore, the waveforms of resonant currents \( i_{L_1} \) and \( i_{L_2} \) are consistent with the theoretical analysis.

Table II: Parameters of Prototype

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Meaning</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_n )</td>
<td>Input Voltage</td>
<td>48 V</td>
</tr>
<tr>
<td>( V_o )</td>
<td>Output Voltage</td>
<td>12 V</td>
</tr>
<tr>
<td>( P_o )</td>
<td>Rated Power</td>
<td>300 W</td>
</tr>
<tr>
<td>( f_s )</td>
<td>Switching Frequency</td>
<td>1 MHz</td>
</tr>
<tr>
<td>( n )</td>
<td>Transformer Turns Ratio</td>
<td>1</td>
</tr>
<tr>
<td>( C_1 )</td>
<td>Resonant Capacitor</td>
<td>0.88 ( \mu )F</td>
</tr>
<tr>
<td>( L_1 )</td>
<td>Resonant Inductor</td>
<td>50 ( \mu )H</td>
</tr>
<tr>
<td>( C_{\text{mid}} )</td>
<td>Non-resonant Capacitor</td>
<td>100 ( \mu )F</td>
</tr>
<tr>
<td>( C_r )</td>
<td>Resonant Capacitor</td>
<td>1.98 ( \mu )F</td>
</tr>
<tr>
<td>( L_r )</td>
<td>Resonant (Leakage) Inductor</td>
<td>12 ( \mu )H</td>
</tr>
<tr>
<td>( L_m )</td>
<td>Magnetizing Inductor</td>
<td>350 ( \mu )H</td>
</tr>
</tbody>
</table>

### IV. CONCLUSION

In this paper, a hybrid DCX based on resonant switched-capacitor and LLC converter is proposed for data center applications. It enables 4w1 conversion ratio with an n:w transformer to optimize the transformer design. Meanwhile, all primary-side switches can achieve ZVS, and the ZVS conditions of different switches are analyzed in detail to facilitate the design. Moreover, the primary-side switches have lower voltage and current stresses than that of conventional LLC converter, resulting in enhanced performance.
A 48V input to 12V/25A output hardware prototype is designed and tested. The experimental results are presented to validate the analysis and demonstrate the effectiveness of the hybrid DCX design. The peak efficiency is 94.22% at 50% load. In the future, a more compact converter prototype with smaller parasitic parameters will be designed to further improve efficiency and power density.

**Fig. 6.** Experiment results: (a-b) the drain-to-source and gate-to-source voltage waveforms of $Q_2$, and the resonant current waveforms of $I_{L1}$ and $I_{LR}$. (c) the voltage waveforms of $C_{GS}, C_0, C$, and the resonant current waveforms of $L_r$.

**Fig. 7.** Measured efficiency versus output power.

**REFERENCES**


