A Series-Capacitor Based Zero-Bias Trans-Inductor Voltage Regulator

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***Abstract*—In data-center applications, the trans-inductor voltage regulator (TLVR) has emerged as a favorable Point-of-Load (PoL) converter due to its superior transient response. However, conventional trans-inductor (TL) suffers from high DC bias current, which limits magnetic saturation margins and hinders power density improvement—a critical bottleneck for Vertical Power Delivery (VPD) scenarios. To address this, this paper presents a multi-phase Series-Capacitor Zero-Bias Trans-Inductor Voltage Regulator (SC-ZBTLVR). The proposed topology utilizes a series-capacitor network to extend the voltage step-down ratio and inherently resolve the current-balancing challenges typical of zero-bias configurations. A $24\,\mathrm{V}$-to-$1\,\mathrm{V}$, 8-phase SC-ZBTLVR prototype is built and tested, featuring compact 3-in-1 integrated TL modules. Leveraging the zero-bias mechanism, the converter achieves a peak efficiency of 90.5% and delivers $47.5\,\mathrm{A}$ per phase at full load, realizing a power density of $1645\,\mathrm{W/in^3}$, a current density of $0.533\,\mathrm{A/mm^2}$ at $380\,\mathrm{A}$ output.**

***Index Terms*—Point-of-load (PoL), vertical power delivery (VPD), zero-bias trans-inductor voltage regulator (ZBTLVR), series capacitor (SC), integrated TL.**

I. Introduction

With the rapid advancement of AI, it is widely recognized that power management has lagged behind processor scaling, creating a critical power bottleneck for high-performance processors such as GPUs and ASICs. These devices typically demand low voltage ($< 1.8\,\mathrm{V}$), ultra-high current ($> 2000\,\mathrm{A}$), and ultra-fast transient response ($> 1\,\mathrm{A/ns}$) [1], [2], posing significant challenges for point-of-load (PoL) converters. A conventional mother-board power delivery architecture is illustrated in Fig. 1 (a), where power is delivered from the periphery to the core through a lateral path using a two-stage step-down conversion. Under such conditions, parasitic impedances (e.g., ESR and ESL) in the power delivery network (PDN) introduce substantial conduction losses and limit the converter's transient-response bandwidth. To mitigate these issues, a vertical power delivery (VPD) architecture has been proposed [3]. As shown in Fig. 1 (b), the intermediate bus converter (IBC) performs the initial voltage step-down, and backside-mounted PoL converters delivery power vertically into the chip. This approach drastically shortens the high-current path, significantly reducing conduction losses. With the emergence of PowerVia technology [4], VPD is poised to enable next-generation power delivery solutions for high-performance processors.

Among Buck-type converters used in PoL applications, the trans-inductor voltage regulator (TLVR) has attracted significant industrial interest due to its excellent transient response, scalability and regulation capability [5]–[8]. However, unlike directly coupled-inductor structures, TLVRs require an additional coupled-current path, and face challenges in reconciling high current handling with a compact footprint, limiting their suitability for VPD architectures. The zero-bias TLVR (ZBTLVR) overcomes this limitation through an innovative transformerless interconnection that enables superior DC delivery while retaining the TLVR's fast transient response and scalability [9]–[11]. Nevertheless, ZBTLVR's asymmetric inductor-leg configuration complicates current balancing for zero-bias operation, and its switching voltage stress increases with higher input bus voltage [2], potentially degrading efficiency.

The series-capacitor (SC) structure characterized by a high step-down ratio, high power density, and intrinsic current balancing, has garnered widespread attention in single-stage converter design. Several works integrate SC networks with customized coupled-inductor Buck topology to achieve optimized performance. In [12]–[14], the SC structure serves as a front-end stage to realize a high-efficiency 2:1 conversion ratio. In [15]–[19], multistacked SC structures are embedded within Buck converters to achieve higher step-down ratios and reduced volume.

This paper proposes a multiphase series-capacitor zero-bias TLVR (SC-ZBTLVR) topology, specifically addressing the single-stage voltage step-down ratio and current-balancing challenges of the ZBTLVR. Compared to existing TLVR solutions, the proposed design enables a higher step-down ratio, more compact volume, and exceptional per-phase current-handling capability. The prototype was tested up to a full-load current of $380\,\mathrm{A}$ ($47.5\,\mathrm{A}$ per-phase), achieving a power density of $1645\,\mathrm{W/in^3}$, and a current density of $0.533\,\mathrm{A/mm^2}$.

II. Topology Analysis

A. Operation Principles

Fig. 2 shows the basic circuit schematic of an N-phase SC-ZBTLVR. The control signals of the phases are phase-shifted by $360°/N$. The N-th phase current i_{L_N} flows through the

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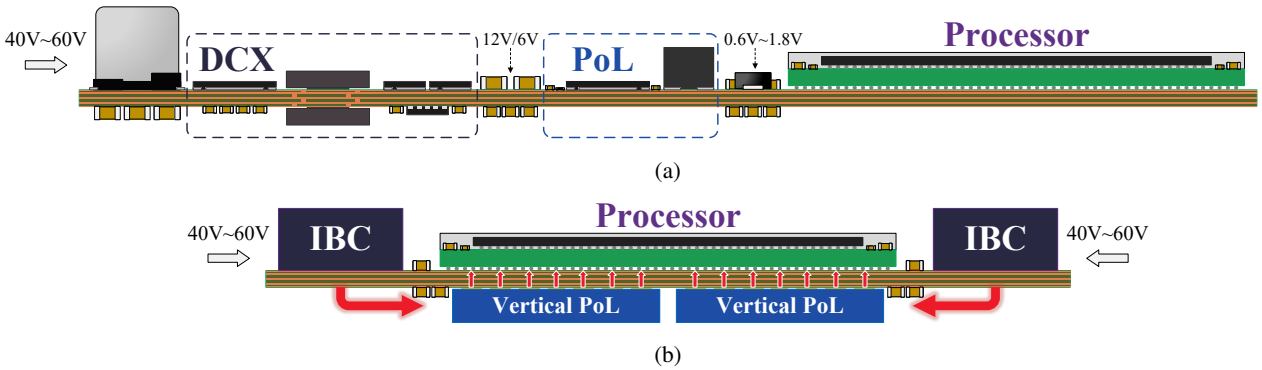


Fig. 1. General power supply architectures in high-performance processor applications. (a) Conventional two-stage lateral power delivery architecture. (b) Emerging VPD architecture.

compensating inductor L_c and enters each TL in the direction opposite to the other phase currents.

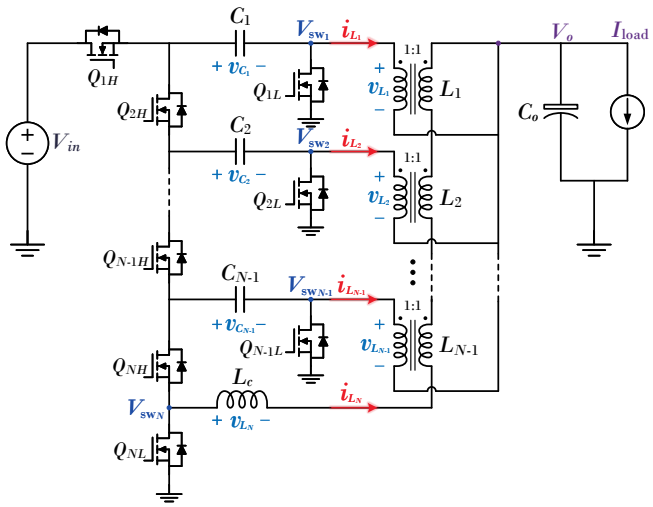


Fig. 2. Schematic of the proposed multi-phase SC-ZBTLVR topology.

The SC structure operates as follows:for the n-th phase, when the high-side switch Q_{nH} turns on, the preceding phase's capacitor C_n transfer charge to the following phase's capacitor C_{n+1} and inductor; when the low-side switch Q_{nL} conducts, the inductor current freewheels through the low-side path. In steady state, the duty ratio of the gate-drive signal for each phase's high-side switch is maintained at D. Based on the charge balance of the series-capacitor in each phase, the equation of per-phase current can be derived as:

$$DI_{n-1} = DI_n \tag{1}$$

Where I_{L_n} is the DC component of the n-th phase current. At steady state, assuming identical duty ratios for all phases, the DC components of each phase are identical. This mechanism is referred to as "self-current-balancing". For the series-capacitor stage, based on the volt-second balance of the inductors, the relationships between the voltage across SCs can be expressed as follows:

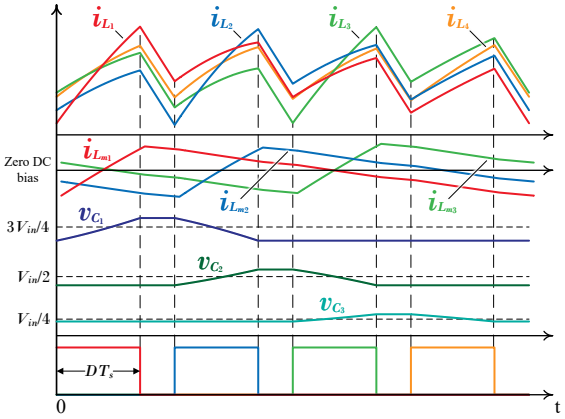


Fig. 3. Typical waveforms of a 4-phase SC-ZBTLVR. DC bias in the equivalent magnetizing currents are canceled when the phase currents are balanced.

$$DV_{L_n} = (1-D)V_o \tag{2}$$

Where $V_{L_n} = Vsw_n - V_o$. When Q_{nL} turns off, V_{sw_n} can be expressed as: $V_{C_{n-1}} - V_{C_n}$ for $1 < n \leq N$. For phase 1, $V_{sw_1} = V_{in} - V_{C_1}$. Based on these mathematical relationships, the voltage across each series-capacitor can be derived as follows:

$$V_{C_n} = (N-n)V_{in}/N \tag{3}$$

Fig. 3 depicts the typical waveforms of a 4-phase implementation of the proposed SC-ZBTLVR topology. The current of each phase will be balanced when each phase has identical duty-ratio.

B. Equivalent Inductor Modeling

For coupled-inductor type structures, the per-phase steady-state inductance L_{pss} is relatively large, whereas the transient inductance L_{ptr} is relatively small [20]. For the ZBTLVR structure, each TL can be modeled as a 1:1 ratio coupled inductor with magnetizing inductance L_m. The simplified

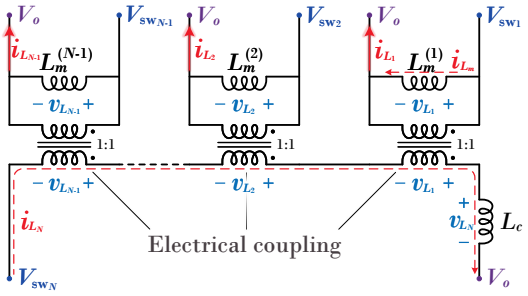


Fig. 4. Equivalent circuit of ZBTLVR.

ZBTLVR circuit schematic is illustrated in Fig. 4, The magnetic flux of each TL can be equivalently represented by its magnetizing current i_{L_m}. For phase n, the magnetizing current can be expressed as $i_{L_n} - i_{L_N}$. It can be demonstrated that the DC component of the equivalent magnetizing current will be canceled to zero when per-phase currents are balanced. Therefore, the SC structure not only reduces switching stress but, thanks to its inherent current-balancing behavior, forces the TLs' DC magnetic flux to remain zero.

As the circuit shown in Fig. 4, for phase-n, based on Kirchhoff's Voltage Law, we can get the equation.

$$V_{L_n} - sL_m^{(n)}(i_{L_n} - i_{L_N}) = 0 \tag{4}$$

where $0 < n \leq N-1$. For phase-N, the equation can be expressed as:

$$\sum_{n=1}^{N} V_{L_n} - sL_N i_{L_N} = 0 \tag{5}$$

Based on the definitions in [20], combining Eq. 4 and 5, we can get the expressions of L_{pss}:

$$L_{pss}^{(n)} = \frac{(1-D)L_m^{(n)} L_c}{(1-ND)L_m^{(n)} + (1-D)L_c} \tag{6}$$

$$L_{pss}^{(N)} = \frac{(1-D)L_c}{1-ND} \tag{7}$$

And also the expressions of L_{ptr}:

$$L_{ptr}^{(n)} = \frac{L_m L_c}{NL_m + L_c} \tag{8}$$

$$L_{ptr}^{(N)} = \frac{L_c}{N} \tag{9}$$

Define $\beta_n = L_c / L_m^{(n)}$, when $0 < n \leq N-1$; $\beta_n = 0$, when $n = N$. The equivalent inductance can be integrated into one equation as:

$$L_{pss}^{(n)} = \frac{(1-D)L_c}{1-ND+(1-D)\beta_{nN}} \tag{10}$$

$$L_{ptr}^{(n)} = \frac{L_c}{N+\beta_{nN}} \tag{11}$$

III. Prototype Design

A. Inductor Design

For TLVR topology, the L_c phase features a relatively long current path, leading to increased conduction losses. This issue becomes more significant in ZBTLVR, in which the compensating phase is required to carry the output current. For a 4-phase SC-ZBTLVR, to enhance power density and efficiency, the three TLs in phases 1-3 need to be integrated.

Thus, a 3-in-1 integrated TL is designed. Fig. 5 shows the 3D model and the assembly relationships. The L_c winding is produced as a monolithic structure through integral machining with low DC resistance. Each phase's winding is magnetically coupled to the L_c winding through the magnetic core with a 1:1 turns ratio. Thanks to the zero-bias mechanism, the per-phase magnetizing inductance is designed approximately 200 nH with only a 5 A saturation current to reconcile the inductance and size. All the magnetic components are fabricated with DMR53 from DMEGC.

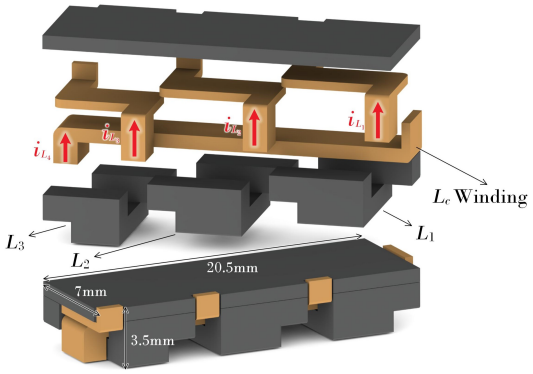


Fig. 5. 3D model and assembly of the designed 3-in-1 integrated TLs. The dimensions are 20.5 mm × 7 mm × 3.5 mm.

Based on the modeling results in Section II-B, to obtain approximately 100 nH per-phase steady-state inductance and approximately 20 nH per-phase transient inductance, thereby balancing steady-state and transient performance, the compensating inductance should be selected as 100 nH. CODACA CSAB0730-R10M is selected as L_c, featuring a soft-saturation behavior, specified at 100 nH with 60 A saturation current. The design parameters of the 3-in-1 integrated TL are shown in Table I.

TABLE I: Design parameters of the 3-in-1 integrated TL.

Parameters	Value
Magnetic inductance, $L_m^{(n)}$	200 nH
Compensating inductance, L_c	100 nH
Phase 1-3, $L_{pss}^{(1)}$–$L_{pss}^{(3)}$	111.11 nH
Phase 4, $L_{pss}^{(4)}$	250 nH
Phase 1-3, $L_{ptr}^{(1)}$–$L_{ptr}^{(3)}$	22.2 nH
Phase 4, $L_{ptr}^{(4)}$	25 nH

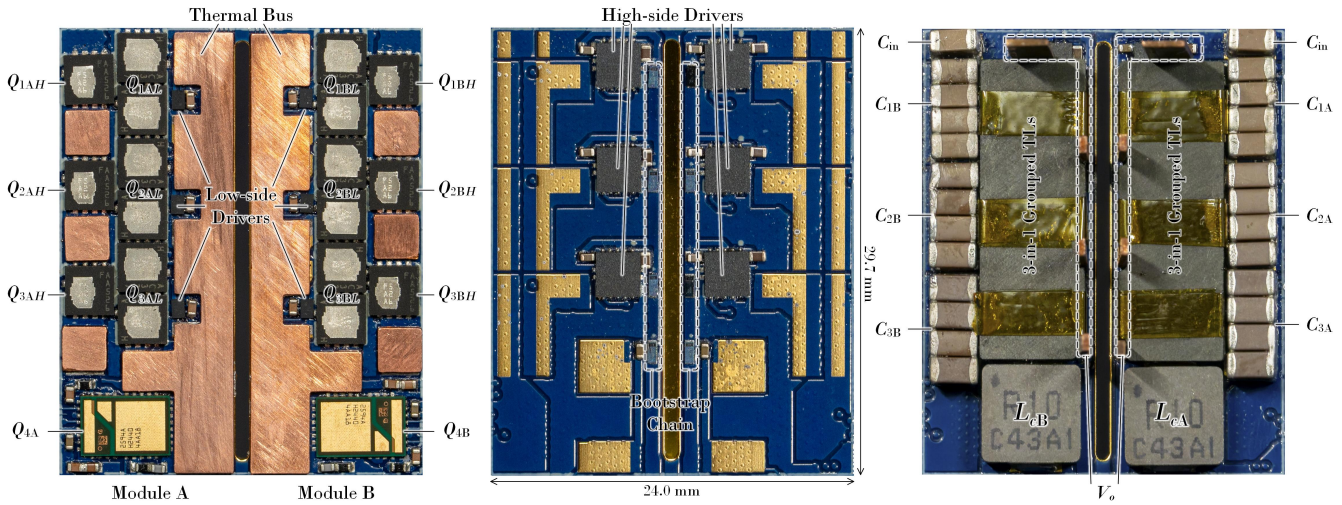


Fig. 6. Photographs of the designed prototype. 3-in-1 integrated TL stacked above the high-side drivers.

B. PCB Design

A PCB prototype was designed to verify the performance of the proposed SC-ZBTLVR topology and the 3-in-1 integrated TL. As shown in Fig. 6, the prototype is constructed with two interleaved 4-phase SC-ZBTLVR modules. For each module, phases 1-3 utilize Infineon IQEH80NE2LM7UCGSC as the high-side switches Q_{nH} with 10 V drive voltage, which is optimized for hard-switching topologies. Two paralleled Infineon IQE004NE1LM7CGSC as the low-side switches Q_{nL} with 5 V drive voltage. For the half-bridge configuration of the fourth phase, Infineon TDA22594AXUMA1 integrated power stage is selected as Q_4, to minimize the footprint and device parasites. All switches were implemented in top-side cooling packages with superior thermal resistance, and matched component heights to guarantee uniform contact with the top-pressing copper heatsink, thus maximizing thermal coupling and heat-transfer efficiency.

To minimize overall thickness, all large-package capacitors are mounted on the bottom side of the PCB, with their height constrained to not exceed that of the inductor. The fabricated PCB uses a 6-layers stack-up with 2-oz copper on the outer layers and 3-oz copper on the inner layers. A 3D rendering of the prototype is shown in Fig. 7. The power stage is vertically interconnected—both electrically and mechanically—to the output board (which hosts the output filter capacitors) via the TL windings and a ground copper bus. The total enclosure dimensions are 29.7 mm × 24.0 mm × 5.3 mm, yielding a volume of 3777.84 mm^3 (0.231 in^3). All components are listed in Table II.

IV. Experimental Results

Experiments are conducted under 24V input, 1V output, with two different switching frequencies. Fig. 8 (a) demonstrates the PWM control signal at 600 kHz. Each phase is controlled in a uniform interleaving pattern with an identical duty ratio. Fig. 8 (b) demonstrates the tested drain-to-source

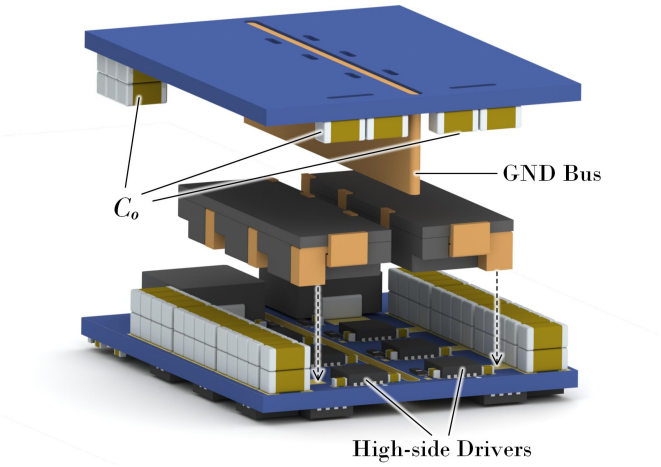
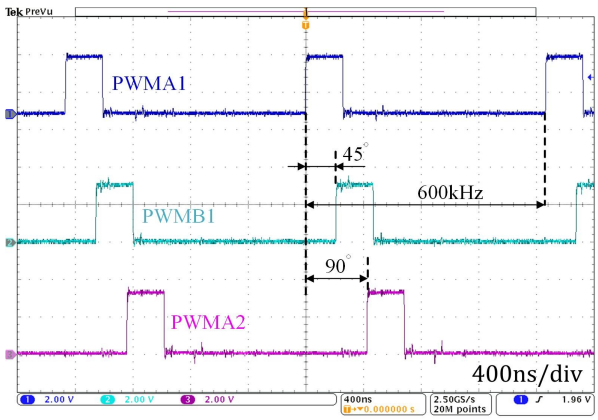


Fig. 7. 3D model and assembly of the 8-phase SC-ZBTLVR prototype. The dimensions are 29.7 mm × 24.0 mm × 5.3 mm.

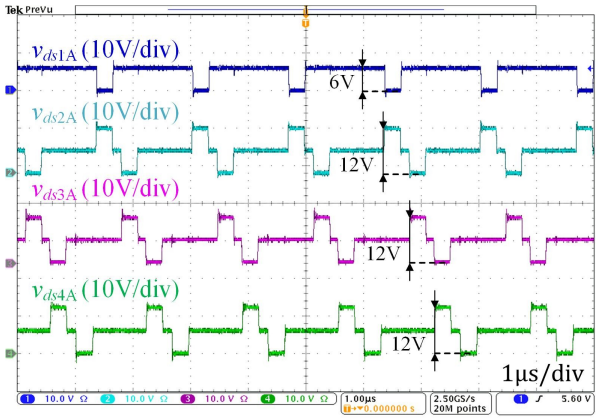
TABLE II: Bill-of-materials

Active Devices	Part Number
$Q_{1H} - Q_{3H}$	Infineon IQEH80NE2LM7UCGSC
$Q_{1L} - Q_{3L}$	Infineon IQE004NE1LM7CGSC×2
Q_4	Infineon TDA22594AXUMA1
High-side Drivers	TI UCC27302A
Low-side Drivers	TI LMG1020
Bootstrap Diodes	Onsemi NSR10F20NXT5G

Passive Devices	Parameters
L_c	CODACA CSAB0730-R10M 100 nH 60 A
C_1	1206 X7S 25 V 22 µF×8
C_2	1206 X7S 16 V 22 µF×8
C_3	1206 X7R 10 V 22 µF×8
C_o	1206 X6S 4 V 220 µF×16



(a)



(b)

Fig. 8. Experimental waveforms at 600 kHz switching frequency. (a) PWM control signal. (b) Drain-to-source voltage v_{ds} of module A.

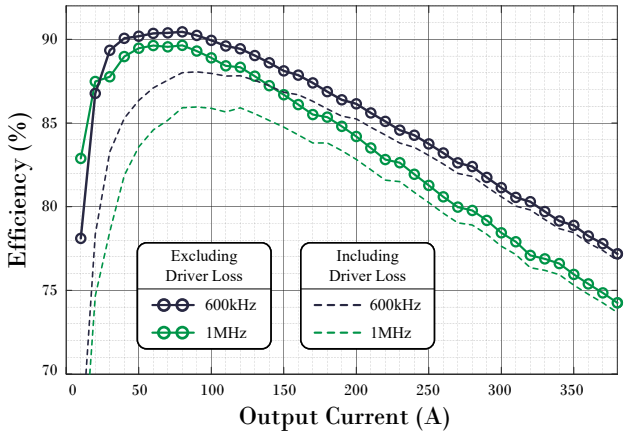


Fig. 9. Measured efficiency versus load current at different switching frequencies.

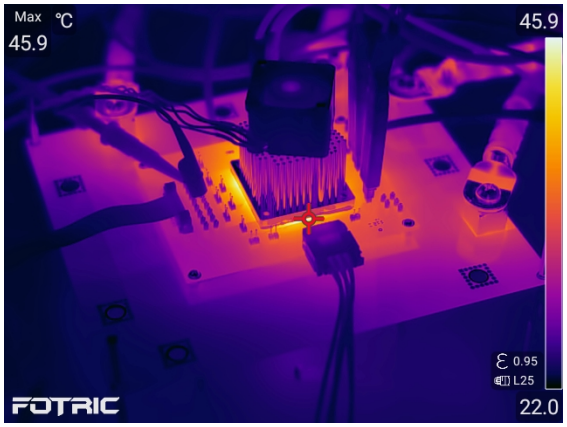


Fig. 10. Thermal image of the SC-ZBTLVR prototype with top-pressing copper heatsink and DC fans. The working condition is 24 V-1 V, 600 kHz and 380 A.

voltage of module A in the two-module prototype. It can be observed that each series-capacitor achieves its steady-state voltage. Based on the analysis in Section II-A, autonomous current balancing is achieved for each phase.

Fig. 9 records the efficiency data. When working at 600 kHz, the peak efficiency is achieved by 90.5% at 80 A load current. When working at 1 MHz, the peak efficiency is achieved by 89.6% at 80 A load current. For both switching frequencies, the full load current is achieved at 380 A with 77.2% and 74.3% efficiency respectively, achieving a power density of 1645 $\mathrm{W/in^3}$ and a current density of 0.533 $\mathrm{A/mm^2}$. A full-load current of 47.5 A per phase demonstrates the topology's high current-handling capability. The thermal image at full load condition with top-pressing copper heatsink is shown in Fig. 10. The efficiency drop at high current is primarily attributed to conduction losses in the PCB traces and magnetic windings due to the ultra-high per-phase current and power density. The heatsink edge temperature remains below 50 °C, indicating outstanding thermal management capability.

V. Conclusions

This paper proposes a novel multi-phase SC-ZBTLVR topology for data-center PoL applications. By integrating a series-capacitor network with the ZBTLVR architecture, the converter achieves a higher voltage conversion ratio with reduced switching voltage stress. Crucially, the series-capacitor configuration ensures inherent current sharing and enforces zero DC bias in the TLs, allowing for a significant reduction in magnetic volume. A 380 A, 8-phase prototype incorporating a compact 3-in-1 integrated TL design was developed to validate the concept. Experimental results demonstrate a robust high-current capability of 47.5 A per phase, a peak efficiency of 90.5%, and effective thermal management under full-load conditions, proving the suitability of the topology for next-generation high-density power delivery.

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