A 95.86%-Efficient 48-V/1.8-V ZVS Voltage Regulator Based on Current Ninefold Rectifier

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***Abstract*—In 48 V data center voltage regulation, the current doubler rectifier offers a high step-down ratio and structural simplicity but suffers from hard-switching, elevated voltage stress, and load-dependent voltage spikes. To overcome these limitations, this article proposes a voltage regulator based on the current ninefold rectifier topology. The proposed design achieves zero-voltage switching (ZVS) for all primary-side switches and employs Δ-connected primary windings to cancel circulating current, thereby reducing both switching loss and conduction loss while enhancing current-transfer capability. A 48-V/1.8-V, 180 A prototype operating at 500 kHz is built and tested. Experimental results confirm primary-side ZVS operation and demonstrate a peak efficiency of 95.86% and a full-load efficiency of 94.29%, verifying the efficiency benefits enabled by ZVS and reduced circulating current.**

***Index Terms*—Current doubler rectifier (CDR), current ninefold rectifier (CNR), data center, voltage regulator (VR), zero-voltage switching (ZVS).**

I. Introduction

With the rapid advancement of modern information technologies, data center power consumption is surging and projected to reach 8% of global electricity use by 2030 [1]. Consequently, power supply efficiency has become increasingly critical. To reduce distribution losses, 48-V server architectures are replacing traditional 12 V buses [2]. However, achieving high efficiency under such a high step-down ratio remains a key challenge [3]. Concurrently, output current demands have risen sharply, with modern CPUs, GPUs, and ASICs requiring over 220 A at voltages below 1.8 V. Furthermore, the wide input range (40 V–60 V) from backup batteries—especially during local UPS engagement—imposes stringent regulation requirements on voltage regulators (VRs) [4]. Insufficient regulation under these conditions may compromise system stability.

To address the design challenges in 48 V server architectures, various single-stage solutions [3], [5], [6], [7] have been proposed alongside two-stage approaches [2], [8], attracting growing interest due to their higher power density and efficiency. For instance, hybrid switched-capacitor converters achieve high power density [7], but suffer from excessive component count [9]. Transformer-based sigma converters [3] offer high efficiency due to their quasi-parallel LLC-buck configuration, and their transient response can be further enhanced through adaptive voltage positioning designs as proposed in [10]. In contrast, the half-bridge current doubler rectifier converter (CDR), derived from the Buck topology, offers minimal components, high efficiency, and simple voltage regulation [9], [11], [12], [13], [14], [15], [16], [17].

Meanwhile, half-bridge CDRs also face several challenges. On the primary side, hard-switching losses, voltage overshoots, and body diode conduction during the off-state remain critical concerns [11]. To handle high load currents, conventional CDR topologies often adopt parallel module configurations. For instance, two CDRs are paralleled in [9] to increase current capacity, yet this approach fails to overcome the inherent limitations of half-bridge CDRs under heavy loads. As load current scales up, switching losses, voltage spikes, and circulating currents become more pronounced [9], [11], [12]. Ensuring reliable operation under such conditions requires modular expansion on the primary side, which increases the number of switches and leads to underutilization of their current-handling capability.

Zero voltage switching (ZVS) of primary-side switches offers a potential solution to these issues [12], [13], [18], [19]. On one hand, soft switching significantly reduces switching loss; on the other hand, the complementary conduction behavior of a soft-switched half bridge eliminates the conduction loss caused by leakage-inductance freewheeling through the body diodes during the off-state in conventional CDR converters. Moreover, ZVS not only improves efficiency but also enables operation at higher switching frequencies, thereby providing the potential for increased power density. Both pulsewidth modulation (PWM) [12] and phase-shift (PS) control [13], [18], [19] can be employed to achieve ZVS for the primary-side switches.

Direct application of PWM control to a half-bridge CDR, however, imposes duty cycle mismatch on the high-side switches of a two-phase Buck converter, resulting in significant current imbalance [12]. This imbalance compromises system stability and thermal distribution. To mitigate this, asymmetrical control combined with a secondary-side series capacitor—proposed in [12]—achieves phase current balancing. Yet, the added

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capacitor complicates magnetic integration and undermines the inherent simplicity of the CDR topology.

Phase-shifted full bridge (PSFB) CDRs leverage complementary control to achieve primary-side ZVS [13], [18], [19]. To reduce the transformer turns ratio, a multilevel phase-shifted CDR incorporating an additional secondary-side capacitance C_r is proposed in [18]. However, a single-phase PSFB CDR module with only two output inductors suffers from limited current capability. To meet high-current requirements, the secondary-side phase count can be increased using a matrix transformer architecture [13], or an input-parallel output-parallel configuration can be employed [19], thereby boosting the total output current. Despite these enhancements, primary-side challenges remain: the circulating current induced by phase-shift control increases with load, leading to degraded efficiency under heavy-load conditions.

To address these challenges, we propose a current ninefold rectifier (CNR)-based VR in this article. The proposed design features topology-level modular optimization to enhance the output current capability of conventional CDRs. It employs complementary PWM control to achieve ZVS for all primary-side switches, thereby reducing switching losses. A Δ-connected transformer facilitates circulating current cancellation on the primary side, which alleviates switches' current stress and improves efficiency under heavy-load conditions. On the secondary side, a nine-phase architecture maximizes the current-handling capability of the primary switches and significantly enhances power delivery.

Compared with the conventional half-bridge CDR topology, the proposed CNR achieves ZVS for all primary-side switches, thereby reducing switching losses and suppressing voltage spikes. It also enables PWM-based voltage regulation without inducing current imbalance on the secondary side. In contrast to PSFB CDRs—which also support primary-side ZVS—the proposed CNR exhibits lower primary-side current stress under identical output current conditions, contributing to improved efficiency and thermal performance.

The remainder of this article is organized as follows. Section II presents the topology derivation and operation principle of the proposed CNR. Section III derives the primary and secondary current stresses of the CNR and analyzes the ZVS condition. Section IV details the key hardware design of the prototype. Section V provides experimental results and performance comparisons. Finally, Section VI concludes the article.

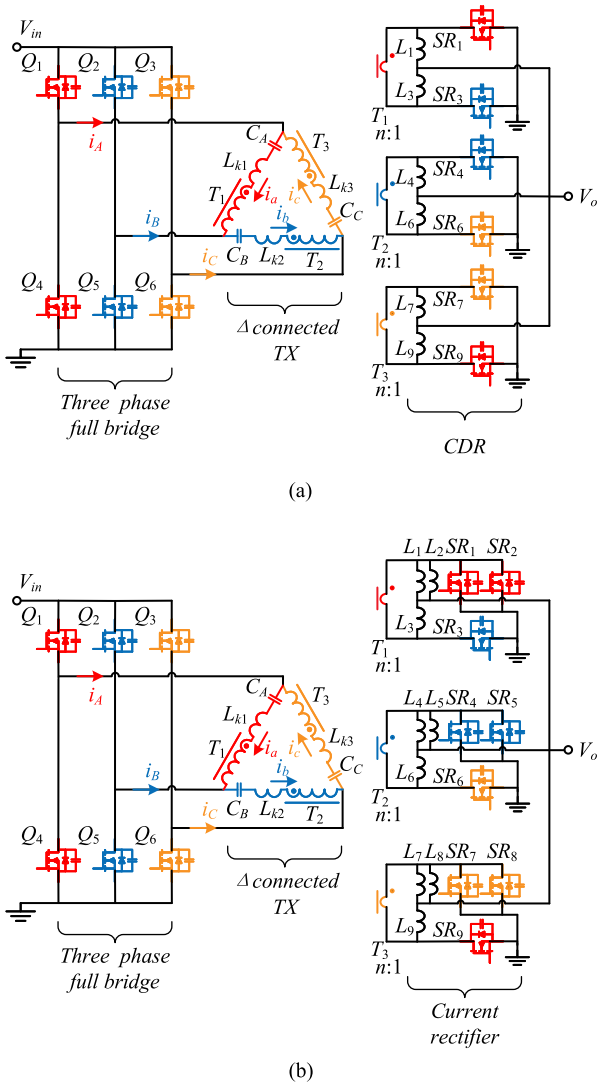


Fig. 1. Topology derivation of the proposed CNR: (a) CDR with Δ-connected transformer and (b) CNR.

II. Topology Derivation and Operation Principle

A. Topology Derivation

To mitigate the primary-side current stress of the PSFB CDR and enhance the output current capability and efficiency of individual modules, this article proposes a topology-level modular CDR scheme, shown in Fig. 1(a), where n denotes the transformer turns ratio. On the primary side, the topology employs a three-phase full bridge combined with a Δ-connected transformer. Compared with the PSFB CDR, the proposed CNR benefits from current cancellation among primary windings enabled by the Δ configuration. This mechanism effectively reduces current stress on primary-side switches and improves efficiency under heavy-load conditions, as discussed in Section III. On the secondary side, the rectifier structure enhances output current capability, providing a scalable solution tailored to data center requirements. Notably, the proposed CNR adopts PWM control, a well-established technique that simplifies system modeling and control design.

The topology illustrated in Fig. 1(a) exhibits current imbalance within the secondary-side CDR module. This imbalance arises from the ampere-second asymmetry of the series capacitor on the primary side of the transformer. Due to the 120° phase shift among the three-phase full bridges, the discharge duration of the series capacitor is nearly twice its charging duration. Taking the first phase as an example, the capacitor's charging/discharging current is proportional to the currents through output inductors L_1 and L_3, resulting in a current ratio of approximately 2:1 between L_1 and L_3. To mitigate this imbalance, an additional current-sharing branch is introduced in each module, forming the proposed CNR topology shown in Fig. 1(b). The current-balancing mechanism will be analyzed in detail in Section III.

B. Steady-State Operation

As shown in Fig. 1(b), the topology comprises three parts: primary-side three-phase full bridge, Δ-connected transformer, and secondary-side CNR. The upper and lower switches in each half-bridge operate complementarily, with a 120 ° phase shift between adjacent phases.

Fig. 2 illustrates the key waveforms over one switching cycle T_s. Gate signals $\text{PWM}_{1,4}$, $\text{PWM}_{2,5}$, and $\text{PWM}_{3,6}$ drive switches Q_1/Q_4, Q_2/Q_5, and Q_3/Q_6, respectively. The drain-source voltages v_{ds1}–v_{ds6} and the corresponding switch currents i_{Q1}–i_{Q6} are associated with switches Q_1–Q_6. Secondary-side synchronous rectifier (SR) drain-source voltages are labeled v_{dsSR1}–v_{dsSR9}, while the corresponding source–drain currents are denoted i_{SR1}–i_{SR9}. Inductor currents i_{L1}–i_{L9} correspond to output inductors L_1–L_9. In addition, i_A, i_B, and i_C represent the output currents of the three primary-side half-bridge switching nodes, whereas i_a, i_b, and i_c denote the primary winding currents of the three transformers. Fig. 3 illustrates the equivalent circuits of each operating mode from the turn ON of Q_1 to the turn ON of Q_2. Note that the colored arrows in Fig. 3 indicate the actual current directions: the red arrows represent the inductor charging currents, whereas the blue arrows denote the inductor freewheeling currents. The defined positive current directions are those specified in Fig. 1(b).

When Q_1, Q_2, or Q_3 conducts, their corresponding output inductors charge; when all three are OFF, the inductors discharge. Based on these charge–discharge states, the proposed topology operates mainly in two modes: energy transfer and freewheeling, with two short auxiliary modes—soft-switching and duty-loss—also occurring. Owing to phase symmetry and waveform periodicity, analysis focuses on a single phase. Phase A—comprising Q_1, Q_4, capacitor C_A, leakage inductance L_{k1}, transformer T_1, output inductors L_1–L_3, and SRs SR_1–SR_3—is used to illustrate the operating principle and key waveforms from t_0 to t_4.

Mode 1 (t_0–t_1)—Energy Transfer Mode: The equivalent circuit corresponding to this operating interval is shown in Fig. 3(b).

Primary switches Q_1, Q_5, and Q_6 are ON, while Q_2, Q_3, and Q_4 are OFF. On the secondary side, SR_3—SR_8 conduct, while SR_1, SR_2, and SR_9 are OFF.

Given that the leakage inductance L_{k1} is much smaller than the reflected inductance $n^2\,L/2$ (assuming $L_1 = L_2 = L$), the voltages across L_1 and L_2 are approximately clamped at $(V_{in} - nV_o)/n$. Consequently, their currents increase linearly at a rate of $(V_{in} - nV_o)/nL$, storing energy. In contrast, the voltage across L_3 is clamped to $-V_o$, causing i_{L3} to decrease linearly at a rate of $-V_o/L$, releasing energy.

Mode 2 (t_1–t_2)—Q_4 Soft Turn- ON Mode: Switch Q_1 turns OFF at t_1. The equivalent circuit corresponding to this operating interval is shown in Fig. 3(c).

According to Kirchhoff's current law (KCL), the output current of the first primary half-bridge switching node is given by $i_A = i_a - i_c$. Prior to the turn OFF of Q_1, the primary winding currents satisfy $i_a = (i_{L1} + i_{L2})/n$ and $i_c = -i_{L9}/n$. Therefore, the node current becomes $i_A = (i_{L1} + i_{L2} + i_{L9})/n$.

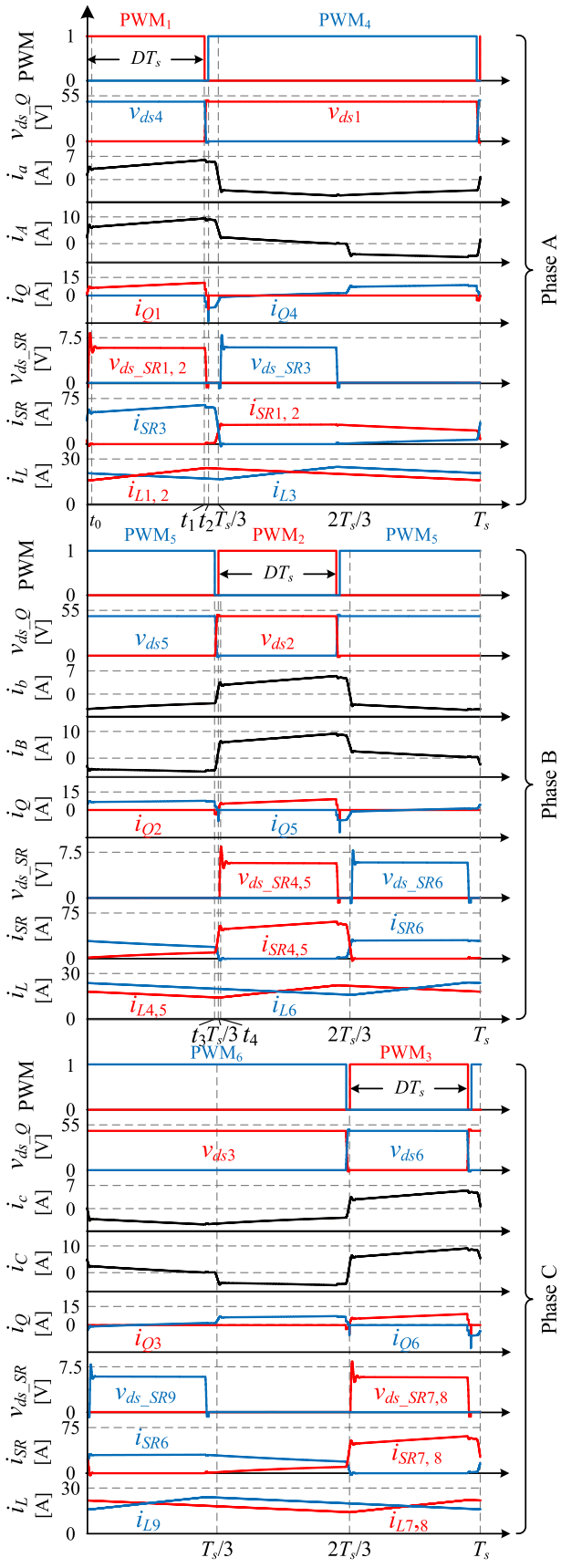


Fig. 2. Key steady-state waveforms.

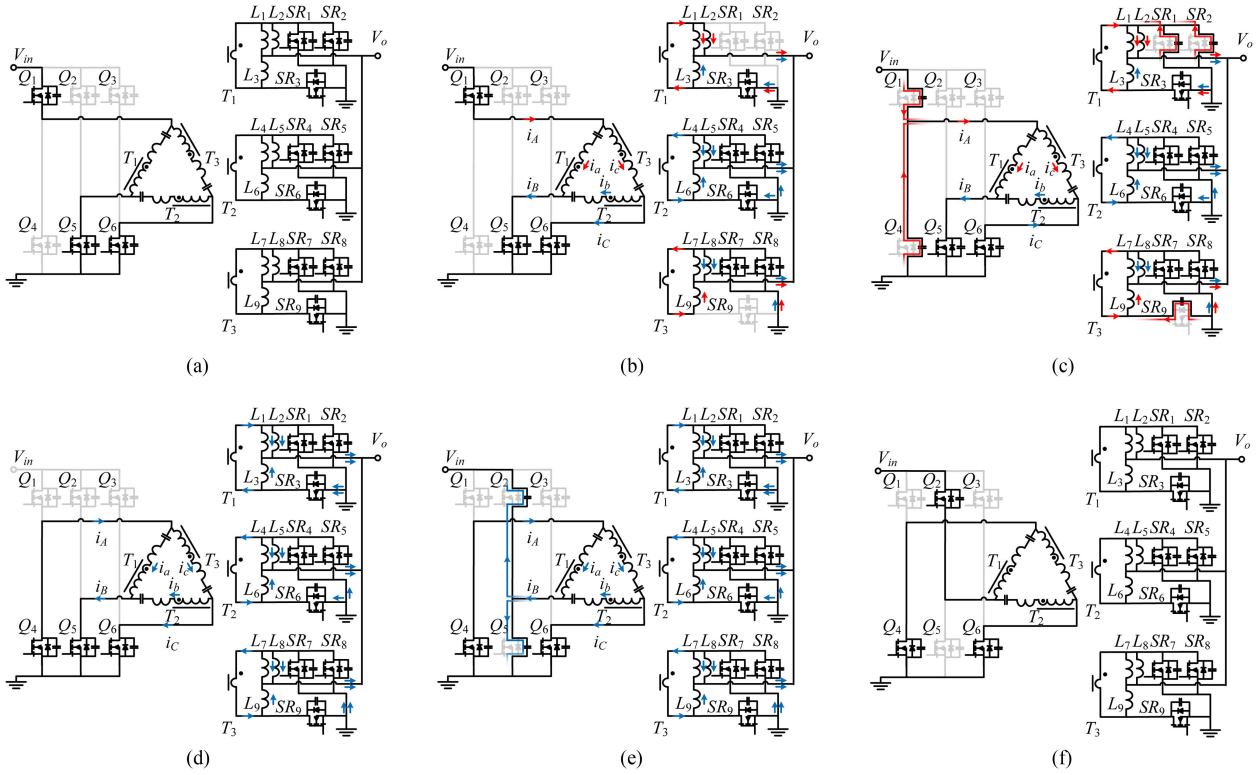


Fig. 3. Equivalent circuits of each operating mode from the turn ON of Q_1 to the turn ON of Q_2: (a) duty-loss mode (0–t_0), (b) energy transfer mode (t_0–t_1), (c) Q_4 soft turn-ON mode (t_1–t_2), (d) freewheeling mode (t_2–t_3), (e) Q_2 soft turn-ON mode (t_3–$T_s/3$), and (f) duty-loss mode ($T_s/3$–t_4).

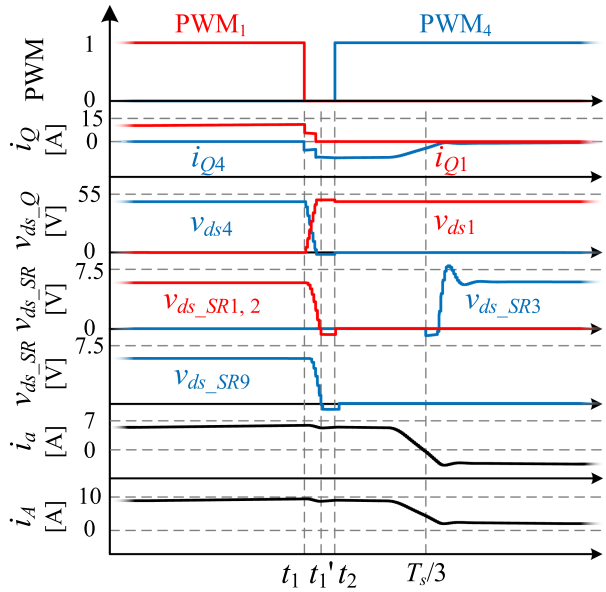


Fig. 4. Enlarged dead-time voltage and current waveforms of Q_4 and $SR_{1,2,9}$.

To more clearly illustrate the circuit behavior during the dead time, the waveform segment within the dead-time interval is enlarged, as shown in Fig. 4.

After Q_1 turns OFF, the positive current i_A charges C_{oss1} of Q_1 and discharges C_{oss4} of Q_4. As the voltage of C_{oss4} decreases, the secondary-side winding voltage of transformer T_1—which is also the drain-source voltage of SR_1 and SR_2—remains at V_{in}/n. This applies a negative voltage across the leakage inductance L_{k1}, causing the primary current i_a to decrease. The secondary winding current also decreases. Because the output-inductor currents are nearly constant, the reduced secondary current forces the junction capacitances of SR_1 and SR_2 to provide increasing discharge currents according to the KCL. After removing the elements that are not involved in the dead-time behavior, the equivalent circuit can be simplified to the form shown in Fig. 5(a), where the output inductor is modeled as a constant current source.

When the voltages of C_{oss4} and the SR output capacitances fall below zero, their body diodes conduct at t_1', marking the beginning of the second half of the dead-time interval. The equivalent circuit then becomes the form shown in Fig. 5(b).

The leakage inductance L_{k1} is then subjected to a positive voltage of $nV_{Dsec} - V_{Dpri}$, where V_{Dpri} is the body-diode drop of the primary switch, and V_{Dsec} is the body-diode drop of the secondary switches. As a result, the primary winding current i_a increases. During the entire dead-time interval, i_a first decreases during $t_1 - t_1'$ and then increases during $t_1' - t_2$, producing a noticeable "dip" in the simulated current waveform. A similar behavior occurs in the primary winding current i_c, and therefore the combined current i_A also exhibits a clear dip.

Mode 3 (t_2–t_3)—Freewheeling Mode: In Mode 2, the body diodes of Q_4 and SR_1, SR_2, and SR_9 conduct. Therefore, these devices achieve ZVS turn ON at t_2. The equivalent circuit for this operating interval is shown in Fig. 3(d).

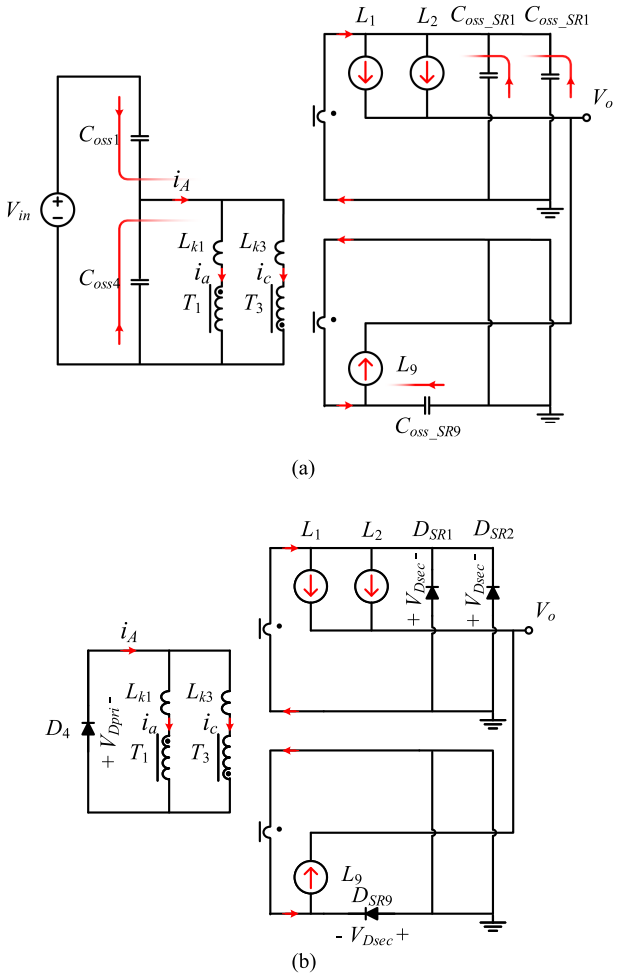


Fig. 5. Simplified equivalent circuits during the dead-time interval: (a) interval $t_1 - t_1'$ and (b) interval $t_1' - t_2$.

The voltages across L_1–L_9 are clamped to $-V_o$, so their currents decrease linearly. Meanwhile, the voltages of the leakage inductors L_{k1} and L_{k3} are clamped at zero, and their currents remain unchanged. Because the primary winding currents do not vary significantly in Mode 2, the winding-current relationships remain approximately the same as in Mode 1, that is, $i_a \approx (i_{L1} + i_{L2})/n$ and $i_c \approx -i_{L9}/n$.

Mode 4 (t_3–$T_s/3$)-Q_2 soft turn- ON *mode:* Q_5 turns OFF at t_3. The equivalent circuit for this operating interval is shown in Fig. 3(e).

According to the KCL relationship, $i_B = i_b - i_a$. From the previous analysis of the freewheeling interval, $i_a \approx (i_{L1} + i_{L2})/n$. The primary winding current i_b remains in the freewheeling mode throughout Modes 1–3, with both its magnitude and direction unchanged. Therefore, its value can be traced back to the interval before Mode 1, when Q_3 is conducting. During the conduction of Q_3, transformer T_2 transfers energy to charge the secondary inductor L_6, leading to $i_b = -i_{L6}/n$. Consequently, $i_B \approx -(i_{L1} + i_{L2} + i_{L6})/n$ and this negative current charges C_{oss5} while discharging C_{oss2}, enabling the ZVS turn ON of Q_2. Since all secondary SRs are conducting in this interval, all transformers are effectively short-circuited, and the circuit can be further simplified to the form shown in Fig. 6. Clearly, the energy stored in L_{k1} and L_{k2} is used to achieve the ZVS turn ON of the upper switch Q_2.

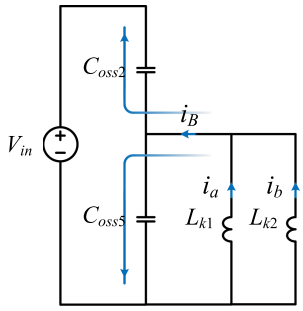


Fig. 6. Simplified equivalent circuit for the interval $(t_3 - T_s/3)$.

Mode 5 ($T_s/3$–t_4)—Duty loss mode: Switch Q_2 turns ON at $T_s/3$, and whether full ZVS is achieved depends on whether the energy stored in the leakage inductances during Mode 4 is sufficient. All secondary SRs remain conducting. The equivalent circuit for this operating interval is shown in Fig. 3(f).

The voltages across output inductors L_1–L_9 are clamped at $-V_o$, causing their currents to decrease linearly at a rate of $-V_o/L$. Meanwhile, the winding voltages of transformers T_1 and T_2 are clamped at zero. As a result, the voltage across L_{k1} is clamped to $-V_{in}$, while the voltage across L_{k2} is clamped to V_{in}. Consequently, the current i_a decreases rapidly with a slope of $-V_{in}/L_k$, whereas the current i_b increases rapidly with a slope of V_{in}/L_k.

This process continues until i_a decreases to $-i_{L3}/n$ and i_b rises to $(i_{L4} + i_{L5})/n$. At that moment, the secondary current of transformer T_1 decreases to $-i_{L3}$, while the secondary current of transformer T_2 increases to $i_{L4} + i_{L5}$. Ultimately, according to the KCL relationship, SR_3, SR_4, and SR_5 naturally achieve ZCS turn OFF.

Starting at t_4, phase B resumes the operating pattern of phase A, followed by phase C, which mirrors phase B.

C. Voltage Gain

The voltage gain is derived using the volt-second balance principle applied to the output inductors. The analysis focuses on L_1 and L_2. From Fig. 2, during t_0 to t_1 (duration DT_s, where D is the duty cycle of the primary upper switches), the voltages across L_1 and L_2 are constant at $(V_{in} - nV_o)/n$.

Neglecting the duty loss mode, from t_2 to T_s, the interval lasts $(1 - D)T_s$. Ignoring the dead-time mode, the voltages across L_1 and L_2 during this period are clamped to $-V_o$.

Applying volt-second balance to L_1 and L_2:

$$\frac{V_{in} - nV_o}{n} DT_s + (-V_o)(1 - D)T_s = 0. \tag{1}$$

The voltage gain can be derived as

$$\frac{V_o}{V_{in}} = \frac{D}{n}. \tag{2}$$

III. Current Stress and ZVS Condition Analysis

To achieve high-efficiency power transmission, it is essential to reduce switching losses and minimize the conduction losses of power switches. This section analyzes the current stress and the conditions for ZVS in the proposed CNR topology.

A. Current Stress Analysis

Prior to deriving the current stress of the switches, it is necessary to analyze the rectifier module on the secondary side. Taking the first phase as an example and referring to Fig. 2, during the interval t_0 to $T_s/3$, which consists of 1/3 of the switching period, dead-time and duty-loss intervals are neglected. Assuming output inductances are sufficiently large, the currents of L_1 and L_2 are ripple-free and remain constant at I_{L1} and I_{L2}, respectively. Therefore,

$$i_a = \frac{I_{L1} + I_{L2}}{n}. \tag{3}$$

From $T_s/3$ to T_s, spanning 2/3 of the switching period, dead-time and duty-loss intervals are neglected. Assuming L_3 is ideal, its current remains constant at I_{L3}. Thus,

$$i_a = -\frac{I_{L3}}{n}. \tag{4}$$

Applying charge balance to the series capacitor C_A, we obtain

$$\frac{I_{L1} + I_{L2}}{n} \times \frac{T_s}{3} - \frac{I_{L3}}{n} \times \frac{2T_s}{3} = 0 \tag{5}$$

$$I_{L1} + I_{L2} = 2I_{L3}. \tag{6}$$

Since the output inductors L_1 and L_2 are paralleled, their currents naturally equalize

$$I_{L1} = I_{L2}. \tag{7}$$

Combining (6) with (7), it can be derived

$$I_{L1} = I_{L2} = I_{L3}. \tag{8}$$

Under ideal conditions, the proposed CNR topology evenly distributes the output current among nine output inductors, resulting in a bias current of $I_o/9$ per inductor. Since all three modules operate identically, the following analysis focuses on the first module.

The current stress of the switches can be obtained by segment-wise calculation of their RMS current. According to Fig. 3(b), the current of Q_1 can be regarded as the sum of the primary currents of transformers T_1 and T_2. In Mode 1, the secondary currents of T_1 and T_2 correspond to the combined currents of inductors L_1 and L_2, and the current through inductor L_9, respectively. For simplification of calculations, the inductor current ripple is neglected, along with the short-duration dead-time and duty cycle loss modes. Consequently, the average current of Q_1 in Mode 1 can be expressed as follows:

$$I_{Q_1,Mode1} = \frac{I_o}{3n}. \tag{9}$$

The current flows through Q_1 for approximately DT_s, and remains zero during the rest of the switching cycle. Therefore, its RMS value is given by

$$I_{Q_1,RMS} = \frac{I_o}{3n}\sqrt{D}. \tag{10}$$

The current flowing through Q_4 can be approximately divided into four distinct stages for analysis:

1) *Stage I ($t \in [0, t_1)$):* During the conduction of Q_1, Q_4 remains off, resulting in zero current through Q_4:

$$I_{Q_4}^{(I)} = 0. \tag{11}$$

2) *Stage II ($t \in [t_1, T_s/3)$):* After Q_1 turns OFF, the current through Q_4 is determined by the sum of the currents in inductors L_1, L_2, and L_9, scaled by the transformer turns ratio, i.e.,

$$I_{Q_4}^{(II)} = -n \cdot (i_{L_1} + i_{L_2} + i_{L_9}) = -\frac{I_o}{3n}. \tag{12}$$

3) *Stage III ($t \in [T_s/3, 2T_s/3)$):* In this interval, the current is given by the sum of L_3 and L_9 currents multiplied by the turns ratio. Since the primary currents of transformers T_1 and T_3 flow in opposite directions, the current through Q_4 is approximately zero:

$$I_{Q_4}^{(III)} = n \cdot (i_{L_3} - i_{L_9}) = 0. \tag{13}$$

4) *Stage IV ($t \in [2T_s/3, T_s)$):* The current through Q_4 is the sum of the currents in L_3, L_7, and L_8, scaled by the transformer turns ratio

$$I_{Q_4}^{(IV)} = n \cdot (i_{L_3} + i_{L_7} + i_{L_8}) = \frac{I_o}{3n}. \tag{14}$$

Therefore, the RMS current of Q_4 over one switching cycle T_s can be expressed as

$$a = \int_0^{DT_s} 0^2\, dt = 0$$

$$b = \int_{DT_s}^{T_s/3} \left[-n(i_{L_1} + i_{L_2} + i_{L_9})\right]^2 dt$$

$$c = \int_{T_s/3}^{2T_s/3} \left[n(i_{L_3} - i_{L_9})\right]^2 dt = 0$$

$$d = \int_{2T_s/3}^{T_s} \left[n(i_{L_3} + i_{L_7} + i_{L_8})\right]^2 dt$$

$$I_{Q_4,\mathrm{RMS}} = \sqrt{\frac{1}{T_s}(a + b + c + d)} = \frac{I_o}{3n}\sqrt{\left(\frac{2}{3} - D\right)}. \tag{15}$$

The current stresses of Q_2 and Q_3 are identical to that of Q_1, while the current stresses of Q_5 and Q_6 match that of Q_4.

The primary-side current stress of the PSFB CDR topology is given by [20]:

$$I_{PSFB\_pri,RMS} = \frac{I_o}{2n}\sqrt{\frac{1}{2}}. \tag{16}$$

From (10), (15), and (16), it is evident that the three-phase full bridge of the CNR topology exhibits significantly lower current stress compared with the full bridge of the PSFB. This reduction is not only attributed to the larger number of switches

in the three-phase full bridge, but also to the circulating-current cancellation effect inherent in the Δ-connected three-phase transformer. Under the condition of employing the same number of switches, the primary-side conduction loss of the CNR is only two-thirds that of the PSFB.

During one switching cycle, SR_3 conducts for one-third of the period and carries the combined current of L_1, L_2, and L_3, which equals the total output current of the submodule, i.e., $I_o/3$. Meanwhile, SR_1 and SR_2 each conduct for two-third of the switching cycle, carrying half of the submodule output current, i.e., $I_o/6$. Therefore, the RMS current stresses of SR_1, SR_2, and SR_3 can be calculated as

$$I_{SR_{1,2}\_\mathrm{RMS}} = \sqrt{\frac{2}{3}\left(\frac{I_o}{6}\right)^2} = \frac{I_o}{6}\sqrt{\frac{2}{3}} \tag{17}$$

$$I_{SR_3\_\mathrm{RMS}} = \sqrt{\frac{1}{3}\left(\frac{I_o}{3}\right)^2} = \frac{I_o}{3}\sqrt{\frac{1}{3}}. \tag{18}$$

The secondary-side current stress of the PSFB CDR topology is given by [20]

$$I_{PSFB\_\mathrm{sec},RMS} = I_o\sqrt{\frac{1}{2}}. \tag{19}$$

While the proposed CNR topology reduces current stress on the secondary-side SRs compared to the PSFB CDR, this is primarily due to the higher component count. Specifically, the CNR prototype utilizes twelve switches, with SR_3, SR_6, and SR_9 each consisting of two parallel devices. If the PSFB CDR were scaled to use the same total number of switches—six in parallel per SR—its conduction losses would be comparable to those of the CNR topology.

B. ZVS Condition Analysis

The proposed CNR can achieve ZVS for primary-side switches. In conjunction with the mode analysis presented in Section II, this section focuses on the operating principles and condition analysis for realizing ZVS in the primary side.

The ZVS principle for the primary low-side switches is consistent, and Q_4 is selected for the analysis. The ZVS of Q_4 occurs during Mode 2, as described in Section II. In this mode, the SR_1, SR_2, and SR_9 also achieve ZVS simultaneously, corresponding to the equivalent circuit shown in Fig. 3(c). The ZVS condition is

$$t_2 - t_1 \geq \max\left\{\frac{2nQ_{oss,Q}}{I_{L1}+I_{L2}+I_{L9}}, \frac{2Q_{oss,SR}}{I_{L1}+I_{L2}}, \frac{Q_{oss,SR}}{I_{L9}}\right\} \tag{20}$$

where $Q_{oss,Q}$ and $Q_{oss,SR}$ are the output charge of the primary switch and SR. Since the ZVS of the primary-side low-side switch and the secondary-side SRs is achieved through the output-inductor current, and the output inductance is sufficiently large to be regarded as a constant-current source during the dead time. As shown in Fig. 7(a), the drain–source voltage of Q_4 decreases almost linearly within this interval. As a result, Q_4 achieves ZVS even under no-load conditions. As the output power increases, the required dead time for ZVS becomes shorter. Therefore, as long as the dead time is sufficient, the primary-side low-side switches can achieve ZVS. In practice, the dead time is fixed, allowing both the primary-side low-side switches and the secondary-side SRs to achieve ZVS under light-load conditions. However, this inevitably results in a longer body-diode conduction interval at heavy load, leading to additional conduction loss.

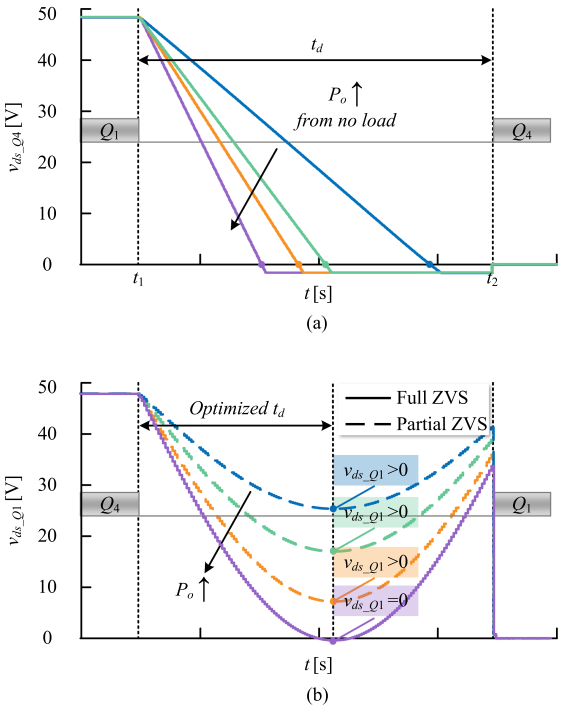


Fig. 7. Drain-to-source voltage waveforms during the dead time. (a) Q_4. (b) Q_1.

In the half-bridge structure, complementary switching between the upper and lower switches provides an opportunity for the high-side device to achieve ZVS. Specifically, the leakage inductor current discharges the junction capacitance of the high-side switch during the dead time.

This ZVS transition occurs in Mode 4, as described in Section II, and the corresponding equivalent circuit is illustrated in Fig. 3(e). Taking Q_2 as an example, the ZVS condition for Q_2 is

$$\frac{L_k}{2}\sum_{m=a,b} {i_m}^2(t_3) \geq Q_{oss,Q}V_{in}. \tag{21}$$

According to (21) and the simplified equivalent circuit in Fig. 6, the ZVS of the primary-side upper switches is achieved through the energy stored in the leakage inductance. Since the leakage inductance is relatively small, it cannot be regarded as a constant-current source during the dead time. Therefore, this ZVS process essentially corresponds to the resonance between the switch output capacitances and the leakage inductance, as illustrated in Fig. 7(b), where the drain–source voltage of Q_1 exhibits a resonant transition. Under light-load conditions, the current flowing through L_k is relatively small, making ZVS difficult to achieve. Nevertheless, partial ZVS can still be obtained by appropriately optimizing the dead time. As the load increases, the energy stored in L_k also increases, thereby enabling full ZVS for the primary-side switches.

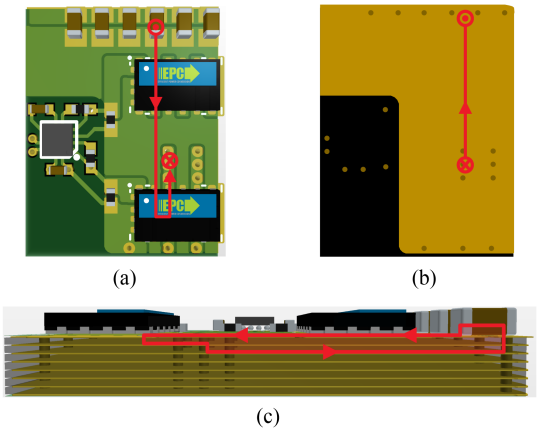


Fig. 8. Optimal power loop with eGaN FETs: (a) top view, (b) inner layer 1, and (c) side view.

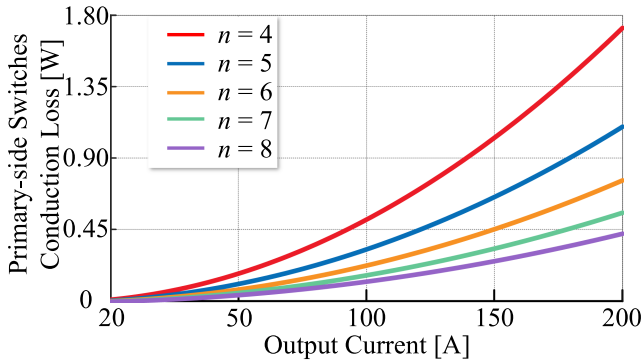


Fig. 9. Primary-side switches conduction loss-based optimization of transformer turns ratio.

IV. Design Considerations

A. PCB Layout Optimization

Since the primary-side switches in CDRs turn OFF at peak current, the parasitic inductance of the PCB trace has a significant impact on the turn OFF voltage spike. Minimizing the loop area of the power path is an effective approach to suppress these voltage spikes by reducing the associated parasitic inductance.

To mitigate this issue, an optimized layout strategy for the primary-side half bridge is adopted [21]. The power flow path is carefully arranged to shorten the switching loop and improve electromagnetic performance. Taking one half bridge as an example, the current flow is illustrated in Fig. 8. The current flows from the positive terminal of the input capacitors through the top layer, passing the two switches that form the half bridge. It then enters the second layer via vias and returns to the negative terminal of the input capacitors. This layout strategy effectively minimizes the power loop path, thereby reducing parasitic inductance and suppressing voltage spikes during switching transitions.

B. Magnetics Design

One advantage of CDR is its compatibility with magnetic integration, where the transformer's magnetizing inductor is utilized as the output inductor. However, this approach compromises the winding utilization of the transformer, leading to increased winding loss under high-current conditions and hindering efficiency improvement. Therefore, the transformer and output inductors are designed separately.

According to (2), to achieve a voltage conversion from 48–60 V to 1–1.8 V while ensuring that the duty cycle D does not exceed $1/3$, the transformer turns ratio n must satisfy the following inequality:

$$n < \left[\frac{V_{in}}{3V_o}\right]_{\min} = \frac{48}{3\times 1.8} = 8.89. \tag{22}$$

As indicated by (10) and (15), a higher transformer turns ratio n can effectively reduce the current stress on the primary-side switches. Fig. 9 illustrates the primary-side conduction losses under different transformer turns ratios. It can be observed that a higher turns ratio effectively reduces the conduction losses of the primary-side devices. Furthermore, increasing the number of primary winding turns enhances the primary-side leakage inductance, which helps us to extend the ZVS range of the primary switches. Therefore, a turns ratio of $n = 8$ is selected in this design. DMEGC's DMR51 W core material is chosen for high-frequency optimization.

The effective cross-sectional area A_e of the magnetic core is optimized based on core loss constraints, which is shown in Formula (23):

$$\Delta B \geq \frac{\left(\frac{V_{in}}{n} - V_o\right) D}{n f_{sw} A_e} \tag{23}$$

where ΔB is the maximum acceptable magnitude of magnetic flux, D is the duty cycle, and f_{sw} is the switching frequency, which is 500 kHz. A_e should satisfy this constraint to limit the core loss.

Finally, the DMR51 W ECW14.5 A magnetic core from DMEGC is adopted. Furthermore, to achieve an 8:1 turns ratio, the primary winding is wound eight turns in series on each magnetic core, and the secondary windings are wound eight turns in parallel.

The output inductance L can be calculated based on

$$L_o = \frac{\left(\frac{V_{in}}{n} - V_o\right) D}{f_{sw} \times 2\Delta i_L} \tag{24}$$

where Δi_L is the inductor current ripple. In this design, the inductor current ripple Δi_L is set to 20% of the full-load current. Therefore, even under half-load conditions, the converter still operates in continuous conduction mode (CCM). Substituting the specific design parameters into (24), the expression becomes

$$\begin{aligned} L_o &= \frac{\left(\frac{V_{in}}{n} - V_o\right) D}{f_{sw} \cdot 2\Delta i_L} = \frac{\left(\frac{V_{in}}{n} - V_o\right)\left(\frac{V_o}{V_{in}}\right) n}{f_{sw} \cdot 2 \cdot \frac{I_o}{9} \cdot 20\%} \\ &= \frac{\left(\frac{48}{8} - 1.8\right)\left(\frac{1.8}{48}\right) 8}{500\times 10^3 \times 2 \times \frac{180}{9} \times 20\%} \\ &= 315\,\text{nH}. \end{aligned} \tag{25}$$

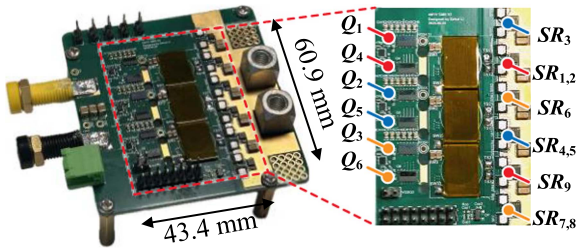


Fig. 10. Picture of the designed prototype.

TABLE I
COMPONENTS LIST AND KEY PARAMETERS

Parameter	Value
V_{in}	48 V–60 V
V_o	1 V–1.8 V
f_s	500 kHz
I_o	180 A–200 A
Transformer Turns Ratio	8:1
Primary Switches Q_1–Q_6	EPC2306
Secondary Switches SR_1–SR_9	IQE004NE1LM7CGSC IQE004NE1LM7SC
Primary Drivers	LMG1205
Secondary Drivers	NCP81074A
Magnetic Core	DMR51W ECW14.5A
Output Inductors	7443081030 (300 nH)
Input Capacitance	60 μF
Output Capacitance	800 μF

A 300 nH inductor from Würth Elektronik (part number 7443081030) is selected as the output inductor in the final design.

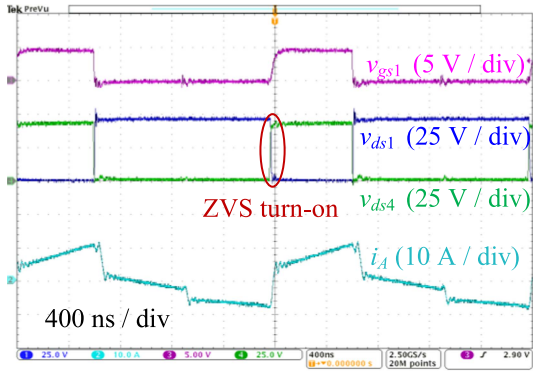
V. EXPERIMENTAL RESULTS

To validate the proposed concept, a 48-V/1.8-V/500-kHz CNR prototype is developed, as shown in Fig. 10. The primary switches are EPC2306, the SRs are IQE004NE1LM7CGSC and IQE004NE1LM7SC, and the magnetic core is a DMR51W ECW14.5 A from DMEGC. The experimental setup employs a Chroma 63206 A electronic load, a Chroma 62100H DC source, and a TI TMS320F280039 C controller. The components list is summarized in Table I.

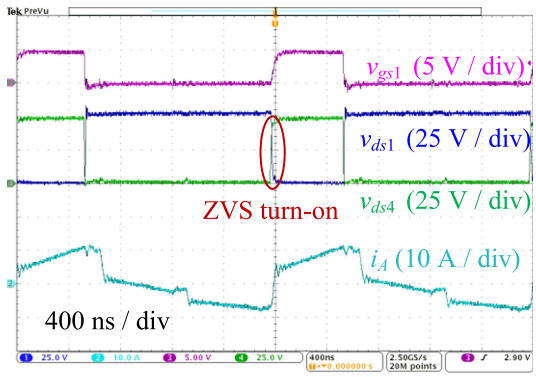
Experimental waveforms for 48 V/1.8 V operation are shown in Fig. 11(a). The phase-shifted gate signals of Q_1, Q_2, and Q_3 exhibit identical switching patterns with 120° separation. Taking Q_1 as an example, Fig. 11(a) shows v_{gs1}, v_{ds1}, v_{ds4}, and primary current i_A, confirming ZVS turn ON. Figs. 11(b) further verify ZVS operation at 54 V/1.8 V.

Fig. 12 shows the efficiency curves versus load current at 1.8 and 1-V output voltage for input voltages of 48, 54, and 60 V. Peak efficiencies reach 95.86% at 48/1.8 V (90 A), 95.51% at 54/1.8 V (100 A), and 95.17% at 60/1.8 V (110 A). Meanwhile, the proposed CNR topology maintains high efficiency under heavy-load conditions, primarily due to the reduced current stress on the primary-side switches and the realization of ZVS.

Fig. 13 illustrates the calculated loss distribution at 48/1.8 V and 180 A full-load conditions. Benefiting from ZVS turn ON, the primary switches Q_1–Q_6 experience only turn-OFF loss, resulting in relatively small total switching loss on the primary side.



(a)



(b)

Fig. 11. Experimental waveforms at different input voltages: (a) 48 V/1.8 V and and (b) 54 V/1.8 V.

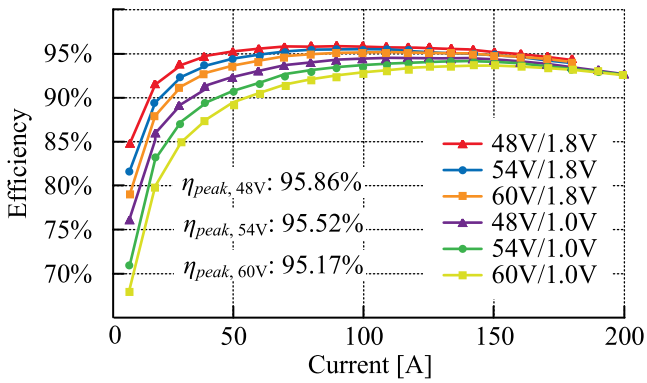


Fig. 12. Measured efficiency versus load current at different input voltages (driving loss excluded).

In addition, owing to the circulating-current cancellation effect, the conduction loss of the primary switches is also reduced. The dominant losses therefore occur in the conduction loss of the secondary winding, the SRs, and the output inductors.

Table II concludes the comparison between the proposed CNR and other solutions. The comparison includes not only other promising 48-V VRM schemes [3], [6], [22], [23], [24], but also the hard switching CDR [9], [14] and the ZVS CDR [12], [13]. Among the evaluated solutions, the proposed CNR converter demonstrates the highest peak efficiency and full-load efficiency,

TABLE II
COMPARISON WITH OTHER 48 V BUS VOLTAGE SOLUTIONS

Year	Solution	V_{in} / V_o	f_s (Voltage Regulator)	Peak efficiency	Full load efficiency	Power density
2020 [3]	Sigma	42–55 V / 0.8–1 V	600 kHz	94.0%	92.5% (80 A)	420 W/in^3
2020 [22]	TSAB	48 V / 1 V	500 kHz	91.5%	85.0% (90 A)	36 W/in^3
2021 [23]	HSC	48 V / 1.8 V	500 kHz	93.3%	85.0%* (33.3 A)	112 W/in^3
2022 [6]	MLB	48 V / 1–1.8 V	250 kHz	94.4%	91.5% (60 A)	474 W/in^3
2022 [24]	LEGOPoL	48 / 1 V	1 MHz	91.1%	85.7% (450 A)	294 W/in^3
2020 [14]	Stacked-bridge CDR	36–60 V / 0.8–1.2 V	500 kHz–1 MHz	92.7%	90.0%* (45 A)	14.8 W/in^3
2022 [13]	Quasi-resonant CDR	48 V / 1.8 V	168 kHz–282 kHz	92.8%	92.0% (80 A)	/
2024 [9]	Half-bridge CDR	40–60 V / 1.3–1.8 V	600 kHz	93.1%	87.8% (120 A)	1037 W/in^3
2024 [12]	Series-Capacitor CDR	48 V / 1 V	500 kHz	90.6%	86.5%* (30 A)	52 W/in^3
This work	CNR	48–60 V / 1–1.8 V	500 kHz	95.86%† 95.14%†	94.29%† (180 A) 93.92%† (180 A)	212 W/in^3

* Data extracted from the provided experimental results, rather than being directly supplied by the authors.
† The higher efficiency results exclude the gate driver losses, whereas the lower efficiency results include them.

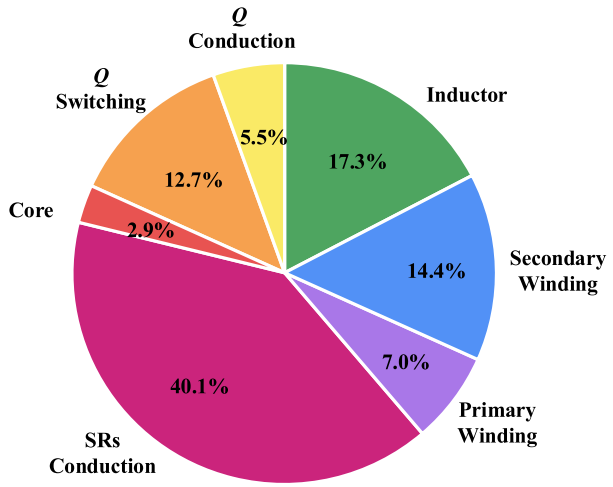


Fig. 13. Power loss breakdown of the designed CNR prototype at 48 V/1.8 V and 180-A full-load conditions.

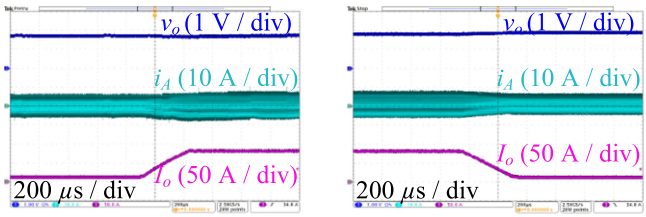


Fig. 14. Experimental waveforms during the transient process: (a) load step-up from 10 to 80 A and (b) load step-down from 80 to 10 A.

consistently outperforming others under identical load current conditions.

It is worth noting that the proposed CNR topology does not exhibit a competitive power density. This limitation primarily arises from the lack of magnetic integration, as the three-phase transformers are implemented discretely. In addition, the output inductors have significantly greater height compared to other components, which further reduces the overall power density.

The transient experimental results are shown in Fig. 14. The current slew rate of the electronic load is set to 10 A/μs. Fig. 14(a) presents the experimental waveforms during a load step-up from 10 to 80 A, while Fig. 14(b) illustrates the step-down transition from 80 to 10 A. The output voltage undershoot and overshoot are both maintained within 100 mV.

VI. CONCLUSION

This article introduces a three-phase CNR to enhance the power delivery capability of conventional CDRs while improving overall efficiency. The proposed topology achieves ZVS for all primary-side switches and effectively eliminates voltage overshoot. The secondary side supports a nine-phase configuration, fully utilizing the current-handling capability of the primary switches. A 48–60-V/1.8-V/500 kHz/180 A prototype is built and tested. Experimental results confirm ZVS operation across the 48–60 V input range, with 95.86% peak efficiency (at 48 V). The proposed converter meets the demanding requirements of high step-down ratio, high output current, and high efficiency in 48 V data centers.

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