Active Clamped Half-Bridge CDR Converter for 48 V Data Center Voltage Regulator Modules

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***Abstract*—In 48 V data center voltage regulator modules (VRMs), current doubler rectifier (CDR) converter is favorable due to its high step-down ratio and structural simplicity. However, CDR converters suffer from excessive voltage stress on primary components caused by high switch turn-OFF currents. This work addresses this limitation through an active clamp technique. The proposed design achieves zero-current switching (ZCS) in primary switches, eliminates voltage spikes, and maintains stability across a 40–60 V input range. Experimental validation via a 48 / 1.8 V, 500 kHz prototype demonstrates 92.24% peak efficiency while confirming: 1) ZCS operation in primary switches; 2) suppression of body-diode freewheeling; 3) elimination of duty-cycle loss; and 4) robust voltage regulation under wide input variations.**

***Index Terms*—Active clamp, current doubler rectifier (CDR), voltage regulator modules (VRMs), zero-current switching (ZCS).**

I. INTRODUCTION

THE energy efficiency of data center power supply becomes critically important as its power demand grows rapidly [1]. To reduce the distribution loss at the bus, a 48 V server data center architecture is proposed to replace conventional 12 V architecture [2], [3], as shown in Fig. 1. The 48 V bus architecture introduces critical challenges for load-side voltage regulator modules (VRMs), notably a high step-down voltage ratio (48 / 1.8 V) [4], [5]. Concurrently, output current requirements escalate, with modern central processing units (CPUs), graphics processing units (GPUs), and application-specific integrated circuits (ASICs) demanding > 220 A at < 1.85 V. Further complexity arises from the backup battery's wide input range (40–60 V), demanding robust voltage regulation from VRMs—particularly during local uninterruptible power supply (UPS) activation [6]. Inadequate regulation risks system instability during power contingencies.

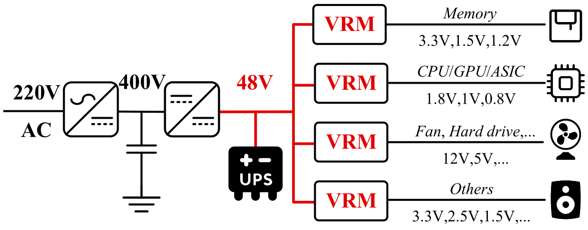

Fig. 1. 48 V data center power conversion architecture.

A two-stage solution [5] requires an intermediate bus with independent stage operation, whereas a single-stage solution [4], [7], [8] operates without an intermediate bus or with collaborative stage control. Current 48 V architectures predominantly adopt two-stage designs, typically combining a DCX converter (e.g., LLC [2] and switches capacitor [9]) with a multiphase Buck voltage regulator.

LLC converter achieves high efficiency via zero-voltage switching (ZVS), while switched capacitor topologies offer high power density. The downstream Buck stage enables fast transient response and high bandwidth. However, two-stage designs struggle to simultaneously achieve high power density and efficiency, driving growing interest in single-stage solutions [3], [10].

Hybrid switched capacitor converters [10] face switching frequency limits from high-frequency inefficiency. The high-frequency design in [7] uses output inductor energy for zero-current switching (ZCS) but suffers from excessive components [11]. The 2:1 charge pump with series-capacitor Buck modules in [12] introduces added complexity and losses. While Buck-integrated solutions dominate, all require redundant capacitors and components. Transformer-based sigma converters [4] achieve efficiency but compromise bandwidth via quasi-parallel LLC-Buck configurations [13]. Most single-stage solutions [3], [4], [7], [12] derive from two-stage architectures.

The core requirement for 48 V bus architectures lies in achieving a high step-down ratio (48/1.8 V), where the half-bridge current-doubler rectifier (CDR) converter [11] excels. Derived from the Buck converter, the half-bridge CDR

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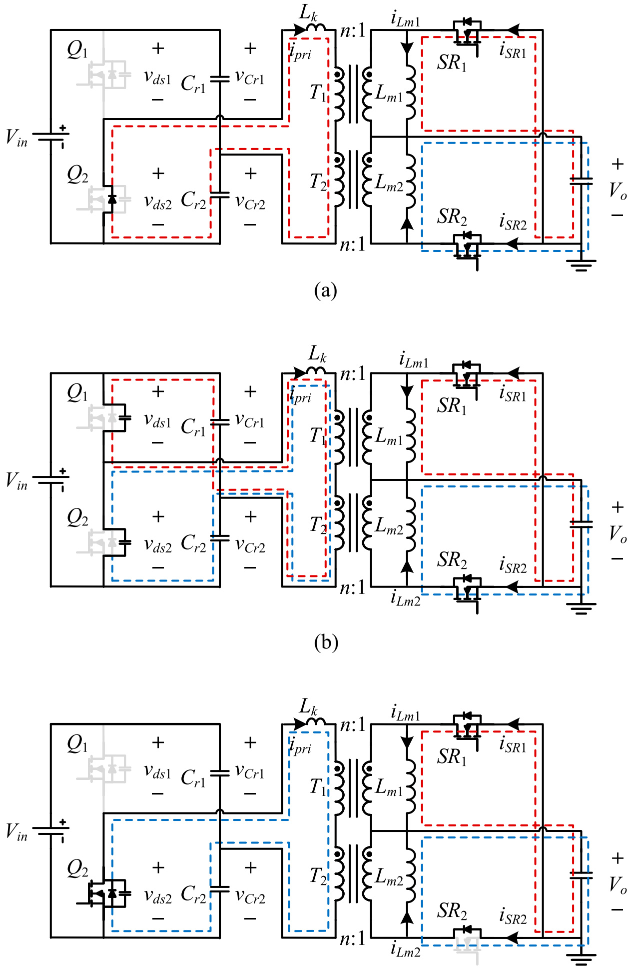
replaces the inductor with a transformer, offering advantages such as scalability, minimal components, fast transient response, and straightforward voltage regulation. In addition, the transformer's magnetizing inductor can function as the Buck converter's output inductor, enabling magnetic integration. Critically, the topology provides two control freedoms—transformer turns ratio and duty cycle—to adjust voltage gain. This allows for achieving the target step-down ratio without extreme duty cycles or additional capacitors/components, reducing costs and control complexity.

While the half-bridge CDR converter achieves a high step-down ratio, it introduces challenges [14], [15], [16], [17]. First, similar to the Buck converter, the primary-side switches in the half-bridge CDR converter experience high-current hard turn-OFF, necessitating a higher voltage margin [11]. In addition, circulating currents exist on both the primary and secondary sides, leading to increased conduction losses. Furthermore, the issue of duty cycle loss hinders the timely charging of the magnetizing inductors. These challenges associated with the half-bridge CDR converter are analyzed in detail in Section II. Many studies focus on improving the performance of the CDR converter. In [17], a stacked primary-side half-bridge circuit reduces device voltage ratings and simplifies the transformer, but merely redistributes voltage stress rather than resolving the voltage spike. Complementary primary-side device operation offers a potential solution. For example, asymmetrical control in [14] pairs with a secondary-side series-capacitor CDR for phase current balancing. Nevertheless, the incorporation of an additional transformer complicates magnetic integration, thereby compromising the intrinsic advantages of the CDR topology. In addition, phase-shifted full-bridge CDRs [15], [16] implement complementary control to realize ZVS of the primary-side devices. The voltage spike can be solved, but this solution suffers from four primary-side switches, duty cycle loss, and conduction-loss-inducing circulating currents.

To address the aforementioned challenges of the half-bridge CDR converter while maintaining its inherent advantage of magnetic integration, this article proposes an active-clamped ZCS CDR augmenting the conventional half-bridge CDR with a primary-side resonant capacitor and secondary-side dual active-clamp switches. The novel integration of an active-clamp circuit with the half-bridge CDR topology demonstrates tight coordination between the clamp network and the main power stage. By synchronizing the primary switches' turn-ON duration to half the resonant period (L_k and C_r), the primary-side switches can achieve ZCS. Compared with the conventional half-bridge CDR, the topology offers several distinct advantages: 1) it eliminates primary-side voltage spikes and reduces voltage stress; 2) the ZCS operation mitigates freewheeling losses in both primary and secondary circuits; and 3) it resolves duty cycle loss issues of conventional half-bridge CDRs.

This article is organized as follows. Section II analyzes the limitations of the conventional CDR. Section III details the operating modes of the proposed topology. Section IV details the circuit analysis and parameter design. The experimental results are presented in Section V. Finally, Section V concludes this article.



(a)

(b)

(c)

Fig. 2. Submodes of conventional CDR converter: (a) submode a (t_a-t_b): Q_1 body diode freewheels; (b) submode b (t_b-t_c): L_k and C_{oss} resonant; and (c) submode c (t_c-t_d): SR_2 body diode freewheels.

II. LIMITATIONS OF CONVENTIONAL CDR

This section examines the inherent limitations of conventional half-bridge CDR. To identify the root causes, we systematically analyze the three critical suboperation modes. Fig. 2 illustrates their equivalent circuits, while Fig. 3 presents the key operational waveforms. Due to circuit symmetry, we focus our analysis on the representative internal between t_a and t_d, as shown in the waveforms.

A. Primary-Side Hard-Switching and Voltage Spike

At t_a, the primary-side current reaches its peak. Considering the parasitic inductor of the PCB and components, turning OFF the primary-side switches at this moment generates a significant voltage spike [11], [14], [17]. Since parasitic inductor cannot be eliminated, this voltage spike is a typical issue in hard-switching half-bridge circuits. It is noteworthy that the voltage spike is not visible in Fig. 3, as it is hard to model parasitic inductance introduced by PCB layout and device packaging in simulation

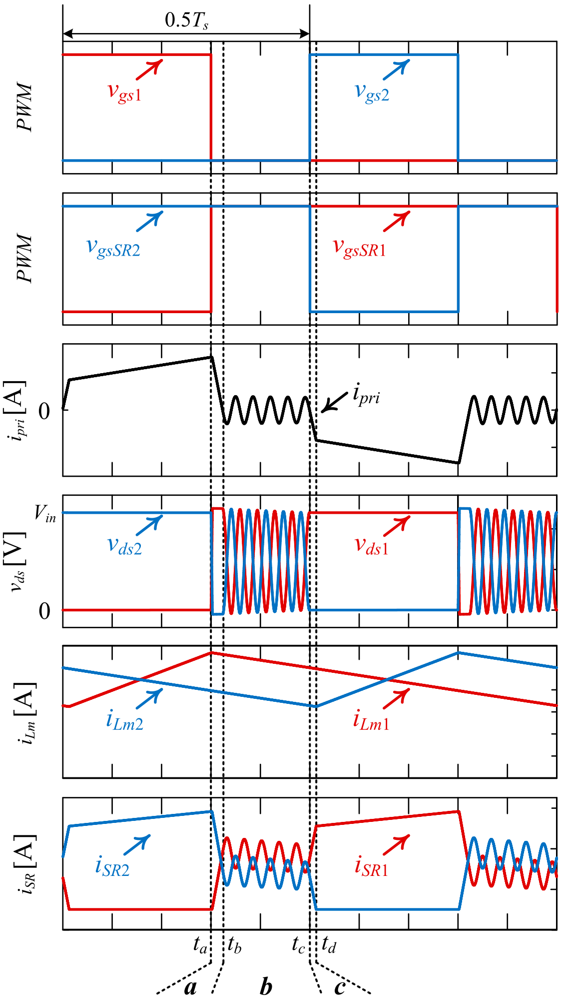


Fig. 3. Key waveforms of the conventional half-bridge CDR converter.

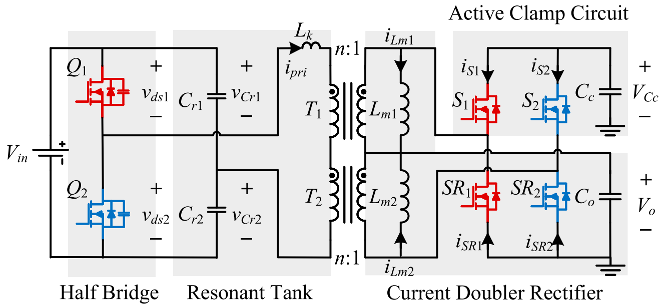


Fig. 4. Schematic of the proposed active clamped CDR converter.

software. This phenomenon is widely observed in CDR-based designs [11], [14], [17].

This spike will increase the voltage stress on the primary-side switches. For input voltages ranging from 40 to 60 V, switches with an 80 V voltage rating are typically sufficient. However, due to voltage spikes caused by hard switching, 100 V-rated switches are often required to ensure safe operation [11]. This additional voltage margin increases the overall cost.

B. Primary-Side Circulating Current

In submode a, although the channel of the Q_2 switch is turned OFF, its body diode conducts to freewheel the transformer leakage inductor current. This circulating current increases conduction losses, and the peak current at time t_a further intensifies body diode conduction losses.

To minimize hard-switching losses, GaN devices are commonly chosen due to their lower switching losses compared to Si devices. However, during reverse conduction, GaN devices tend to exhibit a higher conduction voltage drop than Si devices, further emphasizing the increased conduction losses caused by circulating current. Consequently, eliminating primary-side circulating current becomes essential for reducing losses.

C. Secondary-Side Circulating Current and Duty Cycle Loss

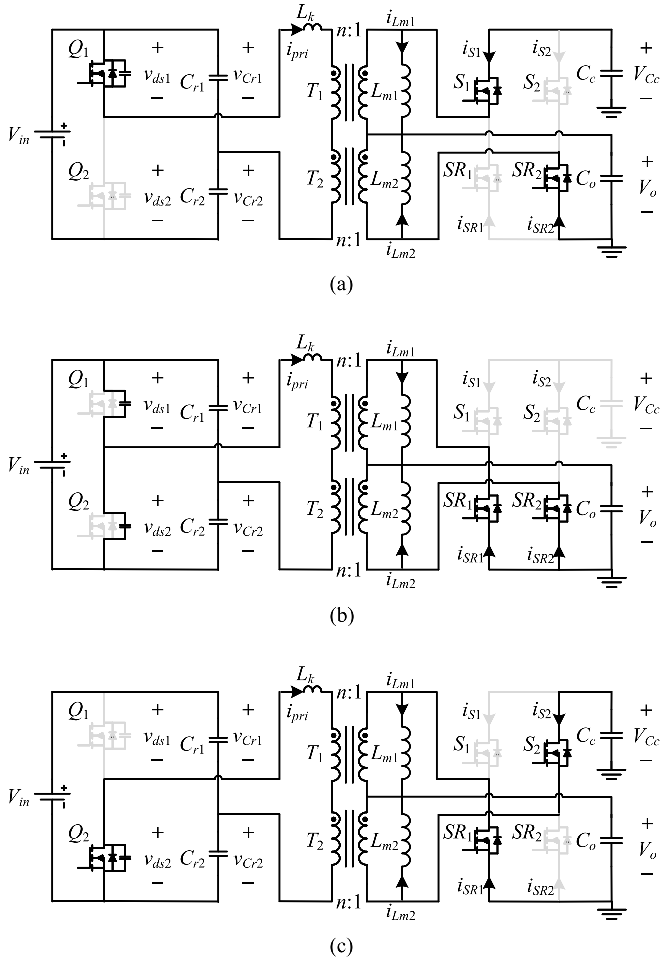
As the primary-side current falls to zero, C_{oss} starts resonating with L_k, transitioning into submode b. When Q_2 is turned ON, submode c begins. In submode c, although the channel of the SR_2 is turned OFF, the body diode conducts. This is because n times the leakage inductor current is less than the magnetizing inductor current at t_c. The body diode of SR_2 continues conducting until the n times leakage inductor current matches the magnetizing inductor current. This phenomenon not only causes body diode conduction loss in secondary side, but also leads to a duty cycle loss, preventing the timely charging of the magnetizing inductors when the primary switches are ON.

The analysis in this section reveals that the large current during the turn-OFF instant (t_a) not only generates a significant voltage spike but also induces freewheeling losses on both the primary and secondary sides. In addition, the conventional half-bridge CDR suffers from duty cycle loss. This article offers a detailed examination of the freewheeling process in primary and secondary switches, which is rarely explored in previous studies.

III. TOPOLOGICAL OPERATION PRINCIPLES

The proposed active clamp CDR converter is shown in Fig. 4, where V_{in} represents the input voltage, V_o represents the output voltage, and n is the transformer turns ratio. It has four parts, which are half-bridge circuit, resonant tank composed of leakage inductor and resonant capacitors, CDR, and active clamp circuit.

Fig. 5 illustrates the three operating modes of the proposed converter. Fig. 6 illustrates the key waveforms of the proposed converter in one switching period. $v_{\text{gs}_{1,2}}$ represents the gate drive signals for Q_1 and Q_2, $i_{L_{m1}}$ and $i_{L_{m2}}$ are the magnetizing inductor currents of the two transformers, i_{pri} is the primary current, v_{ds_1} and v_{ds_2} are the voltages of Q_1 and Q_2, v_{Cr_1} and v_{Cr_2} are the voltage of the resonant capacitor C_{r1} and C_{r2}, and i_{S_1} and i_{S_2} are the currents of the active clamp devices S_1 and S_2. The drive signals of Q_1 and Q_2 are 180° out of phase. The drive signals of SR_1 and SR_2 are complementary to those of



(a)

(b)

(c)

Fig. 5. Key operation modes: (a) Mode 1 (t_0-t_1); (b) Mode 2 (t_1-t_2); and (c) Mode 3 (t_2-t_3).

Q_1 and Q_2, respectively, while the drive signals of S_1 and S_2 are identical to those of Q_1 and Q_2.

To facilitate the analysis, several assumptions are made. The output voltage V_o is assumed to remain constant throughout one switching period T_s, owing to the sufficiently large C_o. Similarly, the clamp capacitor C_c is considered to have negligible voltage ripple, ensuring that its voltage V_{Cc} remains constant during the switching period. Besides, it is assumed that $|i_{\mathrm{Cr1}}(t)| = |i_{\mathrm{Cr2}}(t)|$, and ZCS is achieved.

A. Mode 1 (t_0-t_1)

Q_1 is ON, Q_2 is OFF, SR_1 is OFF, SR_2 is ON, S_1 is ON, and S_2 is OFF. L_k resonates with C_{r1} and C_{r2}. Assuming the capacitance of C_{r1} and C_{r2} is C_r.

The primary-side current i_{pri} equals to the sum of i_{Cr1} and i_{Cr2}. According to Kirchhoff's current law (KCL) and Kirchhoff's voltage law (KVL), we have

$$\begin{cases} L_k \frac{di_{\mathrm{pri}}(t)}{dt} & = V_{\mathrm{in}} - v_{\mathrm{Cr2}}(t) - n(V_{\mathrm{Cc}} - V_o) - nV_o \\ i_{\mathrm{pri}}(t) & = i_{\mathrm{Cr1}}(t) + i_{\mathrm{Cr2}}(t) \\ i_{\mathrm{Cr1}}(t) & = -C_{r1} \frac{dv_{\mathrm{Cr1}}(t)}{dt} \\ i_{\mathrm{Cr2}}(t) & = C_{r2} \frac{dv_{\mathrm{Cr2}}(t)}{dt}. \end{cases} \tag{1}$$

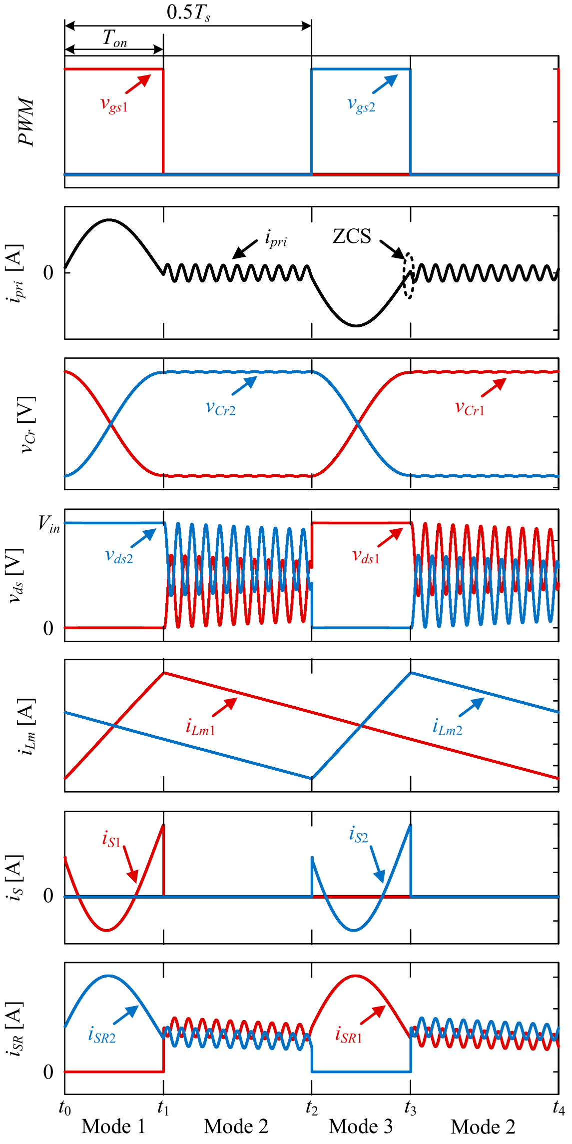


Fig. 6. Key operation waveforms.

With Laplace transform, the expression of $i_{\mathrm{pri}}(t)$ can be obtained

$$i_{\mathrm{pri}}(t) = \sqrt{\frac{2C_r}{L_k}} \times (V_{\mathrm{in}} - nV_{\mathrm{Cc}} - v_{\mathrm{Cr2}}(t_0)) \sin\left(\frac{t - t_0}{\sqrt{2L_kC_r}}\right). \tag{2}$$

The resonant frequency f_{r1} is

$$f_{r1} = \frac{1}{2\pi\sqrt{2L_kC_r}}. \tag{3}$$

In this mode, S_1 clamps the voltage of the transformer T_1 to the voltage of C_c, and the magnetizing inductor current $i_{L_{m1}}$ rises

$$i_{Lm1}(t) = i_{Lm1}(t_0) + \frac{V_{\mathrm{Cc}} - V_o}{L_{m1}}(t - t_0). \tag{4}$$

According to KCL, the current through S_1 is the difference between $i_{L_{m1}}$ and the winding current, as shown in Fig. 6.

At t_1, the primary current resonates to zero, and Q_1 is turned OFF to achieve ZCS. Since the primary current is zero at t_1, no energy is stored in the leakage inductor. Thus, the resonance between L_k and junction capacitors of the primary switches is reduced. Therefore, the condition for ZCS of the primary switches is that the conduction time equals half the resonant period. The conduction time for the primary switches is

$$T_{\text{on}} = \pi\sqrt{2L_k C_r}. \tag{5}$$

B. Mode 2 (t_1-t_2)

Both Q_1 and Q_2 are OFF, SR_1 and SR_2 are ON, S_1 and S_2 are OFF. L_k resonates with the junction capacitors at primary side, assuming the capacitance of the junction capacitors is C_{oss}.

To find the expression of $i_{\text{pri}}(t)$ during t_1-t_2, $v_{\text{ds}}(t)$ during Mode 2 needs to be analyzed. According to the KCL and KVL of the primary side, the following equation can be obtained:

$$\begin{cases} i_{\text{pri}}(t) = i_{\text{coss1}}(t) - i_{\text{coss2}}(t) \\ v_{\text{ds1}}(t) + v_{\text{ds2}}(t) = V_{\text{in}} \\ v_{\text{ds2}}(t) - v_{\text{Cr2}}(t_1) - v_{\text{Lk}}(t) = 0. \end{cases} \tag{6}$$

With Laplace transform, the expression of $i_{\text{pri}}(t)$ can be obtained

$$i_{\text{pri}}(t) = \sqrt{\frac{2C_{\text{oss}}}{L_k}} \times [v_{\text{ds2}}(t_1) - v_{\text{Cr2}}(t_1)] \sin\left(\frac{t - t_1}{\sqrt{2L_k C_{\text{oss}}}}\right). \tag{7}$$

The resonant frequency f_{r2} is

$$f_{r2} = \frac{1}{2\pi\sqrt{2L_k C_{\text{oss}}}}. \tag{8}$$

SR_1 starts freewheeling, and $i_{L_{m1}}$ decreases

$$i_{Lm1}(t) = i_{Lm1}(t_1) - \frac{V_o}{L_{m1}}(t - t_1). \tag{9}$$

C. Mode 3 (t_2-t_3)

Similar to t_0-t_1. At t_2, Q_2 and S_2 turn ON, SR_2 turns OFF, SR_1 is ON, and S_1 is OFF. ZCS is achieved for the primary switches. $i_{L_{m2}}$ rises, and i_{S_2} is the difference between $i_{L_{m2}}$ and the winding current.

D. Mode 4 (t_3-t_4)

Similar to t_1-t_2. At t_3, Q_2 and S_2 turn OFF, SR_2 turns ON, SR_1 is ON, and S_1 is OFF. SR_2 starts freewheeling, and $i_{L_{m2}}$ decreases. L_k resonates with the junction capacitors of primary switches.

Zero current turn-OFF can eliminate the voltage spikes caused by hard switching, as there is no oscillation energy between the junction capacitor and parasitic inductor. Moreover, the primary-side circulating current disappears, as there is no freewheeling current at the turn-OFF moment. In addition, the proposed solution also mitigates secondary-side circulating currents and resolves the duty cycle loss issue.

IV. CIRCUIT ANALYSIS AND DESIGN CONSIDERATIONS

A. Voltage Gain Analysis

To derive the voltage gain, the voltage of resonant capacitor is calculated. The voltage of C_{r2} is taken as the example. During t_0-t_1, the expression of $v_{\text{Cr2}}(t)$ can be solved from (1)

$$\begin{aligned} v_{\text{Cr2}}(t) &= V_{\text{in}} - nV_{\text{Cc}} \\ &\quad - (V_{\text{in}} - nV_{\text{Cc}} - v_{\text{Cr2}}(t_0)) \cos\left(\frac{t - t_0}{\sqrt{2L_k C_{r2}}}\right). \end{aligned} \tag{10}$$

Similarly, $v_{\text{Cr2}}(t)$ during t_2-t_3 can also be calculated

$$v_{\text{Cr2}}(t) = nV_{\text{Cc}} + [v_{\text{Cr2}}(t_2) - nV_{\text{Cc}}] \cos\left(\frac{t - t_2}{\sqrt{2L_k C_{r2}}}\right). \tag{11}$$

Since the voltage of capacitor is balanced during every switching period, combined with (10) and (11), we can derive the relationship between V_{in} and V_{Cc}

$$\frac{V_{\text{in}}}{2} = nV_{\text{Cc}}. \tag{12}$$

Based on the volt-second balance of the magnetizing inductor L_{m1} or L_{m2}, we have

$$(V_{\text{Cc}} - V_o)DT_s - V_o(1 - D)T_s = 0 \tag{13}$$

where D is the duty cycle of the primary switch.

Equation (13) can be simplified as

$$V_{\text{Cc}}D = V_o. \tag{14}$$

Combine (12) and (14), the voltage gain of the proposed converter can be obtained

$$\frac{V_{\text{in}}}{V_o} = \frac{D}{2n}. \tag{15}$$

B. Design of Resonant Capacitor

We aim to reduce the voltage spikes of primary switches during turn-OFF time, which is Mode 2 in Fig. 6. Therefore, v_{ds} during Mode 2 needs to be analyzed. According to (6), we can get the expression of v_{ds1} and v_{ds2}. v_{ds2} is taken as the example

$$\begin{aligned} v_{\text{ds2}}(t) &= v_{\text{Cr2}}(t_1) - v_{\text{Cr2}}(t_1) \cos\left(\frac{t - t_1}{\sqrt{2L_k C_{\text{oss}}}}\right) \\ &\quad + v_{\text{ds2}}(t_1) \cos\left(\frac{t - t_1}{\sqrt{2L_k C_{\text{oss}}}}\right) \\ &\quad + \frac{i_{\text{coss2}}(t_1)}{C_{\text{oss2}}} \sqrt{2L_k C_{\text{oss}}} \sin\left(\frac{t - t_1}{\sqrt{2L_k C_{\text{oss}}}}\right). \end{aligned} \tag{16}$$

From (16), if ZCS is achieved for the primary switches, $i_{\text{coss2}}(t_1)$ equals zero, and v_{ds2} can be expressed as

$$\begin{aligned} v_{\text{ds2}}(t) &= v_{\text{Cr2}}(t_1) - v_{\text{Cr2}}(t_1) \cos\left(\frac{t - t_1}{\sqrt{2L_k C_{\text{oss}}}}\right) \\ &\quad + v_{\text{ds2}}(t_1) \cos\left(\frac{t - t_1}{\sqrt{2L_k C_{\text{oss}}}}\right). \end{aligned} \tag{17}$$

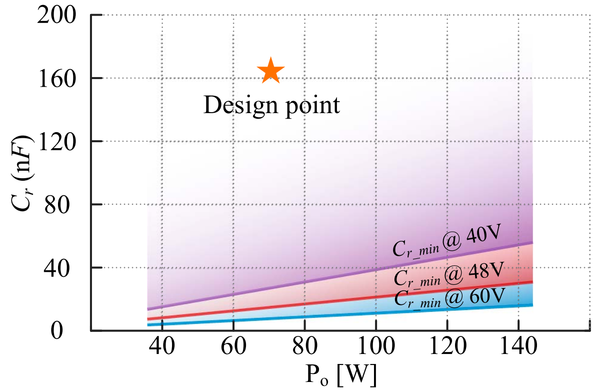


Fig. 7. Design of resonant capacitor C_r.

The maximum v_{ds2} is the voltage stress of the primary switches

$$\begin{aligned}&\max|v_{\mathrm{ds2}}(t)|\\&=\max\left|v_{\mathrm{Cr2}}(t_1)-[v_{\mathrm{Cr2}}(t_1)-v_{\mathrm{ds2}}(t_1)]\cos\left(\frac{t-t_1}{\sqrt{2L_kC_{\mathrm{oss}}}}\right)\right|\\&=\begin{cases}v_{\mathrm{ds2}}(t_1), & 0\le v_{\mathrm{Cr2}}(t_1)\le v_{\mathrm{ds2}}(t_1)\\2v_{\mathrm{Cr2}}(t_1)-v_{\mathrm{ds2}}(t_1), & v_{\mathrm{Cr2}}(t_1)>v_{\mathrm{ds2}}(t_1).\end{cases}\end{aligned} \tag{18}$$

Equation (18) can be further simplified

$$\max|v_{\mathrm{ds2}}(t)|=\begin{cases}V_{\mathrm{in}}, & 0\le v_{\mathrm{Cr2}}(t_1)\le V_{\mathrm{in}}\\2v_{\mathrm{Cr2}}(t_1)-V_{\mathrm{in}}, & v_{\mathrm{Cr2}}(t_1)>V_{\mathrm{in}}.\end{cases} \tag{19}$$

Therefore, to ensure the voltage stress at the primary side equals V_{in}, $v_{\mathrm{Cr2}}(t_1)$ should be positive and smaller than V_{in}.

Substitute this condition into (10), the requirement for $v_{\mathrm{Cr2}}(t_0)$ can be found

$$v_{\mathrm{Cr2}}(t_0)\ge 0. \tag{20}$$

The relationship between v_{Cr} and C_r can be obtained by the energy conservation

$$2\times\int_0^{DT_s} i_{\mathrm{Lk}}(t)\times V_{\mathrm{in}}dt=P_{\mathrm{out}}\times T_s \tag{21}$$

$$8V_{\mathrm{in}}C_{r2}\times[V_{\mathrm{in}}-nV_{\mathrm{Cc}}-v_{\mathrm{Cr2}}(t_0)]=P_{\mathrm{out}}\times T_s. \tag{22}$$

Substitute (20) into (22), we can get

$$-\frac{P_{\mathrm{out}}\times T_s}{8V_{\mathrm{in}}C_{r2}}+V_{\mathrm{in}}-nV_{\mathrm{Cc}}\ge 0. \tag{23}$$

Therefore, C_r not only needs to meet the requirement of (5) to ensure the ZCS of the primary switches, it but also should be large enough to satisfy (23) to reduce the voltage spike at the primary side. The design point is shown in Fig. 7.

C. Transformer Design

In conventional CDR converters, the output inductor can be integrated into the transformer, enabling the magnetizing inductor to function as the output inductor for improved power density. Consequently, the transformer's magnetizing inductance directly influences the CDR's output current ripple. Key design considerations include.

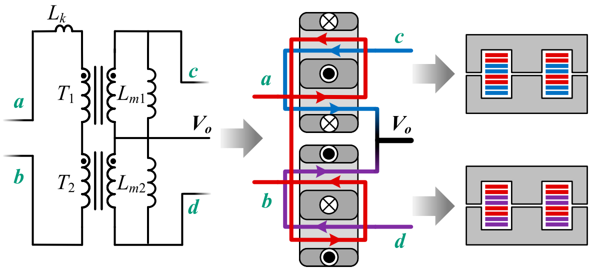


Fig. 8. Planar PCB winding structure.

1) Select n, Current Ripple, and Magnetic Material: To address 40–60 V regulation requirements and winding complexity, a turns ratio of $n=4$ (4:1 primary-to-secondary) is selected. Current ripple is targeted at 30% of per-phase current, with DMEGC's DMR51W material chosen for high-frequency optimization.

2) Calculate L_m: L_m can be calculated based on the following equation:

$$L_m=\frac{(V_{\mathrm{Cc}}-V_o)D}{f_{sw}\times\Delta i_L} \tag{24}$$

where f_{sw} is the switching frequency, which is 500 kHz.

3) Design of A_e: The effective cross-sectional area A_e of the magnetic core is optimized based on core saturation constraints and core loss constraints, which are shown in the following equations [18]:

$$B_{\mathrm{sat}}\ge\frac{L_mI_{\mathrm{peak}}}{nA_e} \tag{25}$$

where, B_{sat} is the saturation flux, and I_{peak} is the peak current of L_m. A_e should meet this requirement to ensure the core will not saturate during the operation

$$\Delta B\ge\frac{L_m\Delta i}{nA_e} \tag{26}$$

where, ΔB is the maximum acceptable magnitude of magnetic flux, and Δi is the current ripple of L_m. A_e should satisfy this constraint to limit the core loss. An appropriate A_e can be obtained with formula (25) and (26).

4) Calculate l_g: The airgap of the transformer, l_g, can be calculated based on the following equation:

$$L_m=\frac{\mu n^2A_e}{l_g} \tag{27}$$

where, μ is the relative permeability of the magnetic material.

Finally, based on the above four steps, the DMR51W ECW14.5A magnetic core from DMEGC is adopted. Furthermore, to achieve a 4:1 turns ratio while shortening the winding length, a specialized planar PCB winding is designed, as shown in Fig. 8. The primary winding is wound 4 turns in series on each magnetic core, and the secondary windings are wound 4 turns in parallel.

V. EXPERIMENTAL RESULTS

To verify the concept, a 48 V / 1.8 V / 500 kHz ZCS half-bridge CDR converter is designed and tested. The prototype

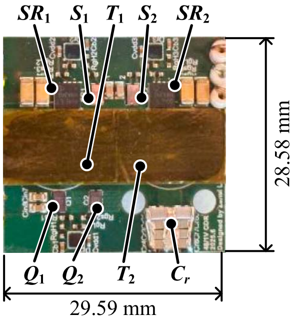


Fig. 9. Picture of the designed prototype.

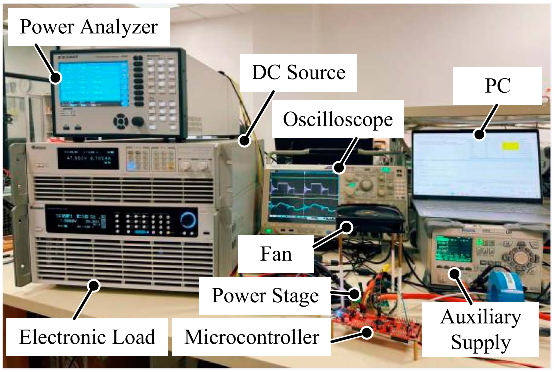


Fig. 10. Experimental setup and test bench.

TABLE I
COMPONENTS LIST

Q_1, Q_2	EPC2204A (80 V, 6 mΩ)
SR_1, SR_2	IQE004NE1LM7 (15 V, 0.45 mΩ)
S_1, S_2	EPC2055 (40 V, 3 mΩ)
Drivers	TI LMG1205
Magnetic core	DMEGC DMR51W ECW14.5A

is shown in Fig. 9. The experimental setup and test bench is shown in Fig. 10. The electronic load is Chroma 63206A (CC mode), the dc source is Chroma 62100H (CV mode), and the microcontroller is TI TMS320F280039C. The control diagram is shown in Fig. 11. The control loop performs PI compensation on the sampled output voltage and calculates the corresponding switching period, thereby achieving constant-on-time control by adjusting the switching period. The components selection is summarized in Table I. The input voltage is 40–60 V, the output voltage is 1.8 V, the output current is 40 A, C_r is 166 nF, and L_k is about 110 nH.

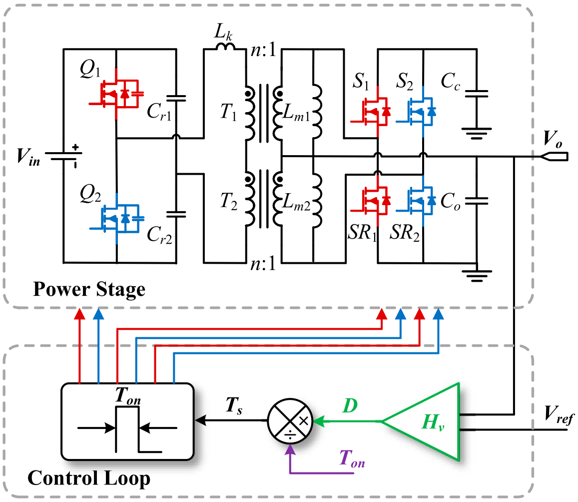


Fig. 11. Control diagram of the prototype.

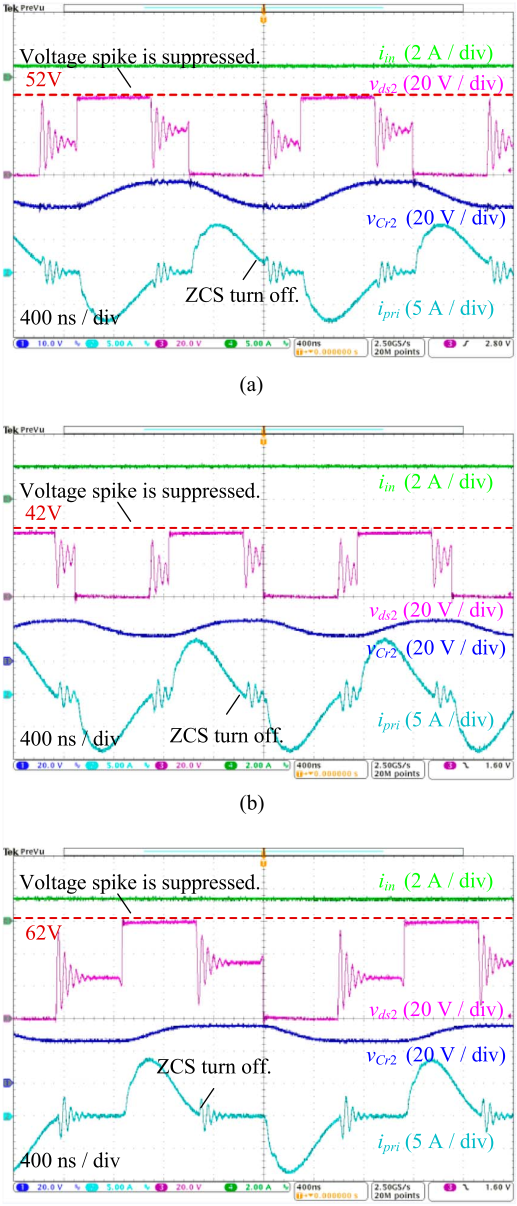
Experimental waveforms for 48 / 1.8 V operation are shown in Fig. 12(a). The phase-shifted gate signals of Q_1 and Q_2 exhibit identical switching patterns with 180° separation. Using Q_2 as an example, Fig. 12(a) illustrates i_{in}, v_{ds2}, v_{Cr2}, and transformer current i_{pri}. During Q_2's conduction, C_{r2} discharges while C_{r1} charges, enabling L_k–C_r resonance. Therefore, during this period, v_{Cr2} decreases, and i_{pri} resonants. At resonant current zero-crossing, Q_2 achieves ZCS turn-OFF. During the subsequent L_k–C_{oss} resonance, v_{Cr2} remains constant until the turn-ON of Q_1. This ZCS operation eliminates voltage spikes (peak $v_{\mathrm{ds2}} \approx 52$ V) and suppresses switching losses at the primary side. In addition, ZCS mitigates primary/secondary circulating currents and duty cycle loss inherent to conventional half-bridge CDRs.

Equation (15) confirms the topology's voltage regulation capability across 40–60 V. Fig. 12(b) and (c) validates ZCS operation at 40 / 1.8 V and 60 / 1.8 V, respectively. Primary-side voltage spikes remain bounded (42 V at 40 V input, 62 V at 60 V input), enabling 80 V-rated switches versus 100 V requirements in traditional designs [11]. The active clamp circuit further resolves duty cycle loss across input voltages.

The thermal image of the prototype operating at an input voltage of 48 V and an output current of 40 A is shown in Fig. 13(a). Under full-load conditions, the temperature of the secondary-side SR reaches 79.7°C. The power loss breakdown is illustrated in Fig. 13(b). It is worth noting that the loss model does not account for all losses present in the prototype, such as PCB conduction losses and termination losses, which are excluded from the analysis.

Fig. 14 presents the efficiency curves versus load current at 1.8 V output voltage, and input voltages of 40, 48, and 60 V. Efficiency curves show peak values of 92.24% at 48 V (8 A), 92.6% at 40 V (6 A), and 91.38% at 60 V (11 A).

The transient experimental results are shown in the Fig. 15. The current slew rate of electronic load is set to 10 A/μs. Fig. 15(a) displays the experimental waveforms during a load step up from 10 to 30 A, while Fig. 15(b) shows the step-down transition from 30 to 10 A. The output voltage undershoot and overshoot remain within 100 mV, and primary-side voltage spikes can be effectively suppressed during the transient events.

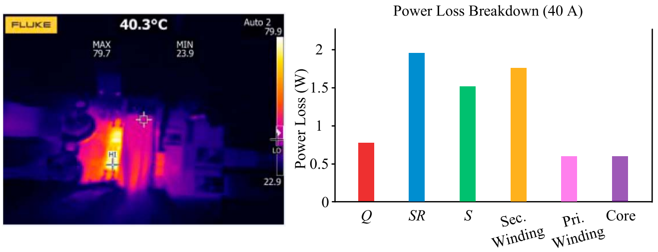


(a)

(b)

(c)

Fig. 12. Experimental waveforms at different input voltages: (a) 48 / 1.8 V; (b) 40 / 1.8 V; and (c) 60 / 1.8 V.



(a) (b)

Fig. 13. Loss distribution at 48 V full load: (a) thermal image; and (b) power loss breakdown.

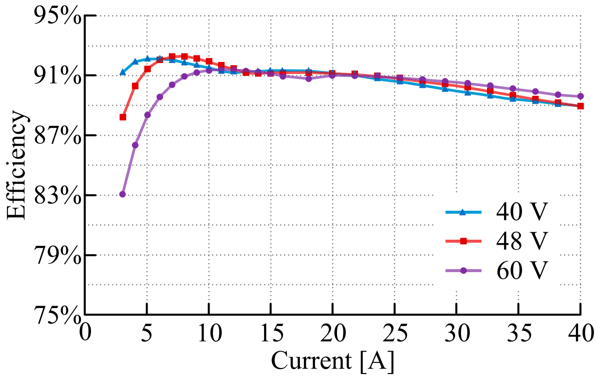
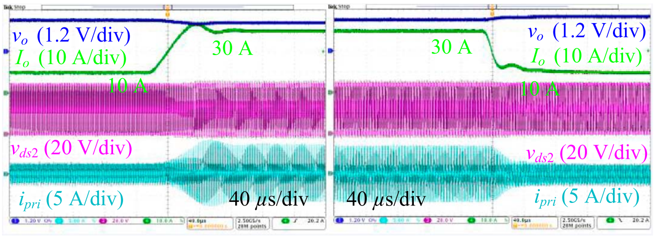


Fig. 14. Measured efficiency versus load current at different input voltages.



(a) (b)

Fig. 15. Transient experiment waveforms: (a) load steps up (10–30 A); and (b) load steps down (30–10 A).

Table II summarizes several VRM solutions for 48 V bus data centers to facilitate comparison with the proposed solution. The two-stage and merged two-stage solutions in [7] and [8] offer higher power density via magnetic integration, but at the cost of requiring many switches. The Sigma converter in [4] achieves high efficiency but faces control bandwidth limitations due to its quasi-parallel LLC resonant and Buck converter configuration [21]. In [17], replacing the CDR's primary side with a stacked bridge prevents soft switching, leading to increased voltage stress. The phase-shifted full-bridge CDR in [16] uses integrated magnetics for higher power density but is constrained by limited operating frequency. The half-bridge CDR in [11] achieves high power density and efficiency through transformer integration, though primary-side switches experience hard switching, causing load-dependent voltage spikes. Finally, the series-capacitor CDR in [14] enables primary-side switch soft switching but its topology hinders magnetic integration, limiting power density improvements.

The proposed active clamp CDR can realize both magnetic integration and soft switching of the primary-side switches. ZCS operation can reduce voltage stress on the primary-side switches.

To address data centers' high current demands, scalability is critical. The proposed topology achieves ZCS on the primary side without significant voltage spikes under increasing load current, enabling full utilization of primary-side switch current capabilities. In contrast, conventional half-bridge CDRs exhibit increasing primary-side voltage spikes as the load current rises,

TABLE II
COMPARISON WITH OTHER 48V BUS VOLTAGE SOLUTIONS

Year	Solution	V_{in} / V_o, I_o	f_s (Voltage Regulator)	Peak Efficiency	Power Ddensity	Voltage Stress @ Pri. Side (V_{in} = 48 V)	Component Count†
2022 [7]	LEGOPoL	48 / 1 V, 450 A	1 MHz	91.1%	294 W/in^3	/	16 + 24
2023 [8]	MSCPoL	48 / 1 V, 450 A	400–602 kHz	93.1%@400 kHz	621 W/in^3	/	4 + 14
2021 [19]	ADI	30–58 / 0.5–1.5 V, 50 A	350 kHz	90.8%	88.5 W/in^3	/	Power chip
2020 [20]	TSAB	48 / 1 V, 100 A	500 kHz	91.5%	36 W/in^3	/	10 + 8
2020 [4]	Sigma converter	42–55 / 0.8–1 V, 80 A	600 kHz	94%	420 W/in^3	/	14
2020 [17]	Stacked-bridge CDR	36–60 / 0.8–1.2 V, 45 A	500 kHz–1 MHz	92.7%@500 kHz	310 W/in^3	/	6
2022 [16]	Quasi-resonant CDR	48 / 1.8 V, 80 A	168 kHz–282 kHz	92.1%	/	/	8
2024 [11]	Half-bridge CDR	40–60 V / 1.3–1.8 V, 120 A	600 kHz	93.1%	1037 W/in^3	79.8 V	2 × 4
2024 [14]	Series-Capacitor CDR	48 / 1 V, 30 A	500 kHz	90.6%	52 W/in^3	60 V*	5
This work	Active clamp CDR	40–60 V / 1.8 V, 40 A	400–600 kHz	92.6%@600 kHz	349 W/in^3	52 V	6

Note: * Data extracted from the provided experimental waveforms, rather than being directly supplied by the authors. † The device count for two-stage or merged two-stage architectures is expressed as the sum of devices in the first stage and the second stage, i.e., "first-stage device count + second-stage device count".

which prevents full utilization of the switches' current capability. This advantage supports paralleling secondary-side modules while sharing primary-side switches—a strategy enabled by a matrix transformer [4], [16] to scale secondary-side modules and boost power density.

VI. CONCLUSION

In this article, we propose an active-clamp half-bridge CDR topology achieving ZCS for primary switches. The design eliminates voltage spikes, suppresses circulating currents on both primary and secondary sides, and resolves duty cycle loss. A complete analytical framework is presented, including voltage gain derivation and key parameter design methodology. Experimental validation employs a 500 kHz prototype (48–1.8 V, 40 A) tested across 40–60 V inputs. Measured results demonstrate stable 1.8 V output regulation across the full input range. ZCS implementation reduces primary-side voltage stress by 33%, enabling 80 V GaN device utilization despite 60 V input conditions.

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