800 V On-Board Charger with Reduced DC-Link Capacitance via Embedded Active Power Decoupling

Qishan Pan[1], Guanjiang Liu[1], Dejun Zhang[1], and Haoyu Wang[1,2]
[1] *School of Information Science and Technology, ShanghaiTech University, Shanghai, China*
[2] *Shanghai Engineering Research Center of Energy Efficient and Custom AI IC, Shanghai, China*
wanghy@shanghaitech.edu.cn

2026 IEEE Applied Power Electronics Conference and Exposition (APEC) | 979-8-3315-7544-1/26/$31.00 ©2026 IEEE | DOI: 10.1109/APEC51134.2026.11517092

***Abstract*—On-board chargers (OBCs) face challenges from bulky DC-link electrolytic capacitors, oversized isolation transformers, and efficiency loss in the isolated DC/DC stage over wide battery voltage ranges. Conventional active power decoupling (APD) circuits can reduce DC-link capacitance requirements. However, they typically rely on additional external switches and energy storage components dedicated to a single function. To improve, this work introduces a two-stage 800 V OBC architecture with reduced DC-link capacitance via embedded active power decoupling. The proposed design employs an integrated APD unit, thereby lowering capacitance demand, minimizing transformer volume, and enhancing the performance of the isolated DC/DC stage under wide gain conditions. A 3.3 kW prototype, supporting an output voltage range of 600–900 V, achieves a peak full-load efficiency of 95.96%, while consistently maintaining high performance across the entire operating range.**

***Index Terms*—Active power decoupling, high power density, on-board charger, partial power processing, wide voltage range**

I. Introduction

With the rapid growth of the electric vehicle (EV) industry, demand for compact, high-efficiency onboard charging systems has intensified. On-board chargers (OBCs) serve as the critical interface between the power grid and the traction battery, directly influencing charging performance [1], [2].

Two-stage OBCs partition power conversion into a front-end power factor correction (PFC) stage and a back-end isolated DC/DC stage, as shown in Fig. 1. The PFC stage interfaces with the AC grid, ensuring high power factor, low total harmonic distortion (THD), and a regulated DC-link voltage, while the isolated stage provides galvanic isolation, output voltage regulation, and efficient energy transfer to the battery. This functional separation enables independent optimization of each stage for efficiency, power density, and control performance across wide operating conditions.

In single-phase OBCs, the twice-line-frequency power ripple is unavoidable. A conventional approach employs bulky passive capacitors at the DC link [3]–[5], which substantially increases volume. To reduce the required DC-link capacitance, active power decoupling (APD) techniques have emerged as a prominent focus. Among these, capacitor-based APD methods are widely adopted [6]–[8], enabling higher power density. However, the additional decoupling circuit must process nearly one-third of the system energy, all of which is reactive. This leads to a noticeable efficiency penalty.

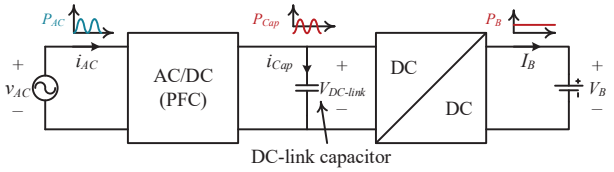

Fig. 1. Two-stage on-board charger architecture.

Beyond the PFC stage, the isolated DC/DC stage is another critical element. Dual-active-bridge (DAB) converters [9]–[11] and LLC/CLLC resonant converters [12]–[15] are strong candidates. The DAB exhibits relatively large turn-off current—significantly higher than that of CLLC—resulting in higher turn-off losses and lower efficiency, a drawback exacerbated at high switching frequencies. Resonant converters deliver superior performance at resonance but degrade noticeably away from resonance. A variable DC-link approach allows near-resonant operation under most conditions [16]–[18], enabling optimal performance. Nevertheless, it imposes stricter requirements on the PFC stage and DC-link capacitor, which must both absorb twice-line-frequency ripple at low DC-link voltage and withstand high voltage stress, often necessitating many electrolytic capacitors in series-parallel.

To address these issues, this work tightly integrates the APD function into the isolated DC/DC stage: a Buck-type APD simultaneously performs twice-line-frequency ripple compensation and output voltage regulation. This arrangement fixes the isolated stage voltage gain, enabling high efficiency and high power density. A 3.3 kW two-stage OBC prototype is constructed to validate the concept, and experimental results confirm its superior performance.

II. Analysis of Two-Stage OBC

A. Twice-Line-Frequency Power Ripple

Under steady-state operation with unity power factor at the AC input, the input voltage v_{AC}, current i_{AC}, and instanta-

This work was partially supported by the Natural Science Foundation of Shanghai under Grant 25ZR1401255.

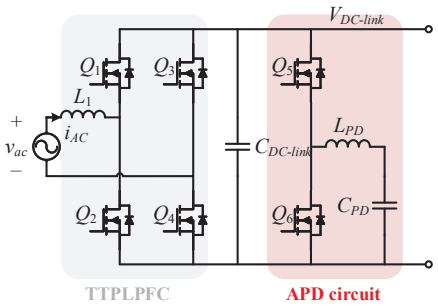

Fig. 2. Totem-pole PFC with active power decoupling circuit.

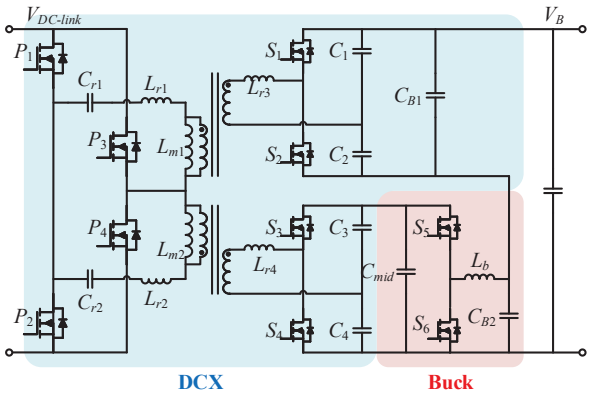

Fig. 3. Isolated DC/DC stage with PPP circuit.

neous power P_{AC} are

$$\begin{aligned} v_{AC}(t) &= \sqrt{2}\, V_{AC,\mathrm{RMS}} \sin(\omega t), \\ i_{AC}(t) &= \sqrt{2}\, I_{AC,\mathrm{RMS}} \sin(\omega t), \\ P_{AC}(t) &= v_{AC}(t)\, i_{AC}(t) = 2 V_{AC,\mathrm{RMS}} I_{AC,\mathrm{RMS}} \sin^2(\omega t) \\ &= V_{AC,\mathrm{RMS}} I_{AC,\mathrm{RMS}} \left[1 - \cos(2\omega t)\right], \end{aligned} \tag{1}$$

where $V_{AC,\mathrm{RMS}}$, $I_{AC,\mathrm{RMS}}$, and ω denote the RMS input voltage, RMS input current, and angular line frequency, respectively. Thus, the input power comprises a DC component and a second-harmonic component at twice the line frequency. Ideally, the DC component equals the battery charging power P_B, while the second-harmonic component represents the power ripple P_{PD} absorbed by the energy buffer:

$$\begin{aligned} P_B &= V_B I_B = V_{AC,\mathrm{RMS}} I_{AC,\mathrm{RMS}}, \\ P_{PD} &= -V_{AC,\mathrm{RMS}} I_{AC,\mathrm{RMS}} \cos(2\omega t) = -P_B \cos(2\omega t). \end{aligned} \tag{2}$$

The twice-line-frequency ripple P_{PD} has an amplitude equal to P_B and a relatively low frequency. Consequently, electrolytic capacitors with high energy density are typically paralleled at the DC link to buffer energy. However, maintaining a sufficiently small DC-link voltage ripple requires very large capacitance.

B. Conventional APD Method

APD techniques substantially reduce the required energy-buffer capacitance. The core idea is to introduce a third port, in addition to the input and output ports, and impose a large twice-line-frequency voltage ripple across its output capacitor to absorb the corresponding power ripple. As illustrated in Fig. 2, a buck converter is paralleled at the DC link and serves as the APD circuit, where the buck's output port acts as the third port. The twice-line-frequency power ripple is controlled to be absorbed by the decoupling capacitor C_{PD}, thereby avoiding the need for a large $C_{DC-link}$ to suppress low-frequency ripple. Moreover, due to the large permissible voltage ripple, the required capacitance of C_{PD} can be significantly reduced.

When P_{PD} is positive, C_{PD} is charged; when negative, it is discharged. A considerable portion of energy is therefore processed twice by the APD path, which reduces overall efficiency. Meanwhile, although the capacitor volume can be lowered, the added half-bridge and inductor increase the total volume. As a result, the system's power density cannot be effectively improved.

C. Isolated DC/DC Stage

LLC/CLLC resonant converters are widely used for the isolated DC/DC stage. A key function of this stage is to accommodate battery voltage variation. Under wide voltage ranges, conventional pulse-frequency-modulated (PFM) LLC/CLLC converters must sweep the switching frequency broadly. Below resonance, circulating current increases, raising conduction losses; above resonance, turn-off current rises, increasing switching and magnetic losses. Consequently, resonant converters suffer notable efficiency degradation over wide voltage ranges. In addition, frequency modulation introduces design challenges:

1) Ensuring zero-voltage switching (ZVS) at high switching frequencies often requires a small magnetizing inductance L_m, which increases circulating current for soft switching.
2) Achieving a wide gain range under heavy load demands a small ratio $L_n = L_m/L_r$, necessitating a large resonant inductance L_r, complicating magnetic integration with the transformer.
3) Transformer design must cover a wide frequency span, hindering optimal performance.
4) Further increasing the switching frequency is limited, constraining power-density improvement.

Partial power processing (PPP) offers an effective solution. As shown in Fig. 3, the PPP-based stage comprises a DC transformer (DCX) and a buck converter. The DCX is implemented as an open-loop CLLC resonant converter operating at its resonant frequency, ensuring galvanic isolation and excellent performance even up to 1 MHz. Output-voltage regulation is achieved by the buck converter, which processes only a fraction of the total power. When the buck handles a large portion of power, its duty cycle is high and efficiency can exceed 99%; when its operating point yields lower efficiency (low output voltage and small duty cycle), the proportion of processed

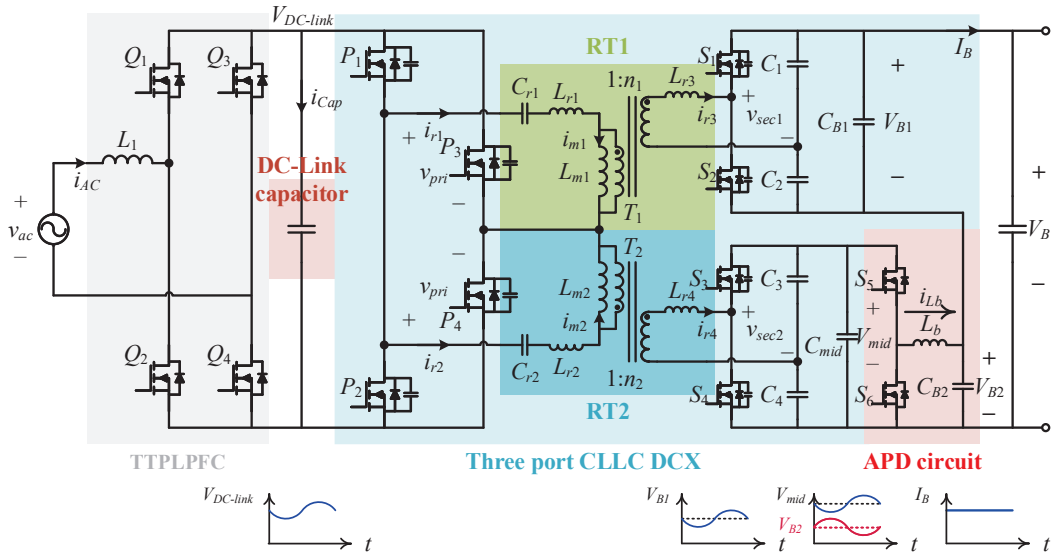

Fig. 4. Schematic of proposed two-stage on-board charger.

power is correspondingly small. This characteristic enables the PPP-based isolated stage to maintain high efficiency across a wide battery voltage range.

III. Proposed OBC with Integrated APD and PPP

A. Topology and Reduced DC-Link Capacitance

For the converters in Fig. 2 and Fig. 3, the buck circuit in the PFC stage is dedicated solely to APD, whereas the buck circuit in the isolated DC/DC stage is used exclusively for output-voltage regulation. This separation yields a redundant hardware structure. To address this, we propose an integrated two-stage OBC architecture with embedded APD, as illustrated in Fig. 4. In the proposed scheme, a single buck converter simultaneously performs twice-line-frequency ripple compensation and output-voltage regulation. In this integrated configuration, V_{B2} carries a significant ripple component, while V_{B1} must exhibit an opposing ripple to ensure a ripple-free output V_B. Owing to the fixed voltage-conversion ratio of the DCX, both $V_{DC-link}$ and V_{mid} inherently exhibit considerable voltage ripple. Consequently, the capacitors $C_{DC-link}$, C_{B1}, C_{mid}, and C_{B2} all serve as distributed energy buffers to decouple the twice-line-frequency power ripple.

If, as in conventional APD implementations, the output capacitor C_{B2} is designated as the primary energy buffer, approximately one-third of the ripple energy still undergoes repeated bidirectional processing within the APD path. More critically, in the integrated structure the twice-line-frequency ripple must propagate through the DCX stage, which significantly increases current stress on the isolated converter and degrades overall efficiency. Therefore, output-side filter capacitors of the DC/DC stage should not be used as the main energy buffer. Instead, $C_{DC-link}$ should be assigned this role, and its capacitance should satisfy

$$C_{B1},\ C_{mid},\ C_{B2} \ll C_{DC-link}. \tag{3}$$

Under this design, the energy buffered by $C_{DC-link}$ is directly absorbed or released without additional circuit-level processing.

The total energy stored in the capacitors can be approximated by

$$\sum_{k\in\{DC-link,\,B1,\,mid,\,B2\}} \frac{1}{2}C_k V_k^2(t) \;\approx\; \frac{1}{2}C_{DC-link}V_{DC-link}^2(t). \tag{4}$$

Since the twice-line-frequency ripple is absorbed by these capacitors,

$$\begin{aligned} &\frac{1}{2}C_{DC-link}V_{DC-link}^2(t) \\ &= \frac{1}{2}C_{DC-link}V_{DC-link}^2(0) + \int_0^t P_{PD}(\tau)\,d\tau \\ &= \frac{1}{2}C_{DC-link}V_{DC-link}^2(0) - \frac{P_B}{2\omega}\sin(2\omega t), \end{aligned} \tag{5}$$

which yields

$$V_{DC-link}(t) = \sqrt{V_{DC-link}^2(0) - \frac{P_B}{\omega C_{DC-link}}\sin(2\omega t)}. \tag{6}$$

Over one line half-period, the RMS value of the DC-link voltage is

$$V_{DC-link,\mathrm{RMS}} = \sqrt{\frac{\int_0^{\pi/\omega} V_{DC-link}^2(t)\,dt}{\pi/\omega}} = V_{DC-link}(0), \tag{7}$$

so (6) can be reformulated as

$$V_{DC-link}(t) = \sqrt{V_{DC-link,\mathrm{RMS}}^2 - \frac{P_B}{\omega C_{DC-link}}\sin(2\omega t)}. \tag{8}$$

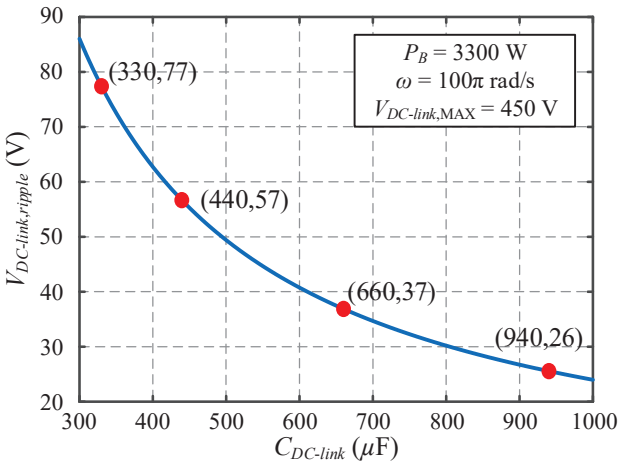

Fig. 5. Relationship between DC-link voltage ripple and $C_{DC-link}$ with $V_{DC-link,\mathrm{MAX}} = 450$ V.

To determine the voltage ratings of the DC-link capacitor and switching devices, the peak DC-link voltage is

$$V_{DC-link,\mathrm{MAX}} = \sqrt{V_{DC-link,\mathrm{RMS}}^2 + \frac{P_B}{\omega C_{DC-link}}}, \tag{9}$$

and the minimum DC-link voltage, which dictates the maximum gain required of the DC/DC stage during charging, is

$$\begin{aligned} V_{DC-link,\mathrm{MIN}} &= \sqrt{V_{DC-link,\mathrm{RMS}}^2 - \frac{P_B}{\omega C_{DC-link}}} \\ &= \sqrt{V_{DC-link,\mathrm{MAX}}^2 - \frac{2P_B}{\omega C_{DC-link}}}. \end{aligned} \tag{10}$$

Thus, the DC-link voltage ripple is

$$\begin{aligned} V_{\text{DC-link,ripple}} &= V_{DC-link,\mathrm{MAX}} - V_{DC-link,\mathrm{MIN}} \\ &= V_{DC-link,\mathrm{MAX}} - \sqrt{V_{DC-link,\mathrm{MAX}}^2 - \frac{2P_B}{\omega C_{DC-link}}} \end{aligned} \tag{11}$$

Considering typical electrolytic-capacitor voltage ratings (below 500 V) and the use of 650 V-rated switching devices, $V_{DC-link,\mathrm{MAX}}$ is set to 450 V. Under this condition, Fig. 5 illustrates the relationship between the DC-link ripple and the capacitance $C_{DC-link}$. By allowing a large twice-line-frequency voltage ripple on the primary energy buffer, the required capacitance can be significantly reduced.

B. Control Strategy

Building on the preceding analysis, the proposed topology integrates APD functionality and output-voltage regulation into a single buck converter. By allowing large voltage ripple across the primary energy-buffer capacitors, the required capacitance is significantly reduced. Achieving a ripple-free output under these conditions, however, demands a tailored control architecture. As shown in Fig. 6, the control system comprises two main loops: (1) a dual-loop PFC controller to ensure unity power factor on the AC side, and (2) a ripple-cancellation loop to guarantee a ripple-free output.

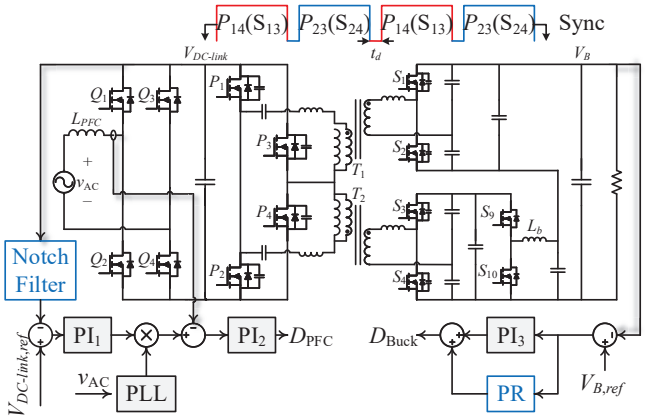

Fig. 6. Control structure.

TABLE I
KEY PARAMETERS AND COMPONENT SPECIFICATIONS

Symbol	Parameter
AC input	220 V_{rms}, 50 Hz
$V_{DC-link,\mathrm{MAX}}$	450 V
PFC switching frequency	100 kHz
CLLC (DCX) resonant frequency	1 MHz
APD buck switching frequency	100 kHz
T_1 turns ratio	15:9
T_2 turns ratio	15:9
$C_{DC-link}$	2×220 μF, 500 V electrolytic
C_{B1}	18×470 nF, 630 V X7R MLCC
C_{mid}	1×10 μF, 600 V film
C_{B2}	1×10 μF, 600 V film
V_B range	600–900 V

To prevent the twice-line-frequency ripple at the DC link from injecting third-harmonic distortion into the input current i_{AC}, a notch filter tuned at 2ω is placed in the DC-link voltage feedback path. In laboratory validation, a resistive load is used instead of a battery; under this condition, ripple-free power delivery requires ripple-free output voltage. Accordingly, proportional–integral (PI) and proportional–resonant (PR) compensators are implemented in parallel for output-voltage regulation. The PI compensator sets the DC operating point, while the PR compensator suppresses the twice-line-frequency component. Coordinated active-power control at the input and output ports ensures that the twice-line-frequency power ripple is absorbed by the circuit capacitors rather than appearing at the output.

IV. Experimental Verification

A 3.3 kW prototype based on the proposed integrated OBC architecture with embedded APD was implemented; key parameters are listed in Table I. The PFC-stage prototype and its steady-state waveforms at full load are shown in Fig. 7. The DC-link voltage exhibits a pronounced 100 Hz ripple, with a peak of 450 V and a valley near 390 V. The isolated DC/DC-stage prototype and its steady-state waveforms under

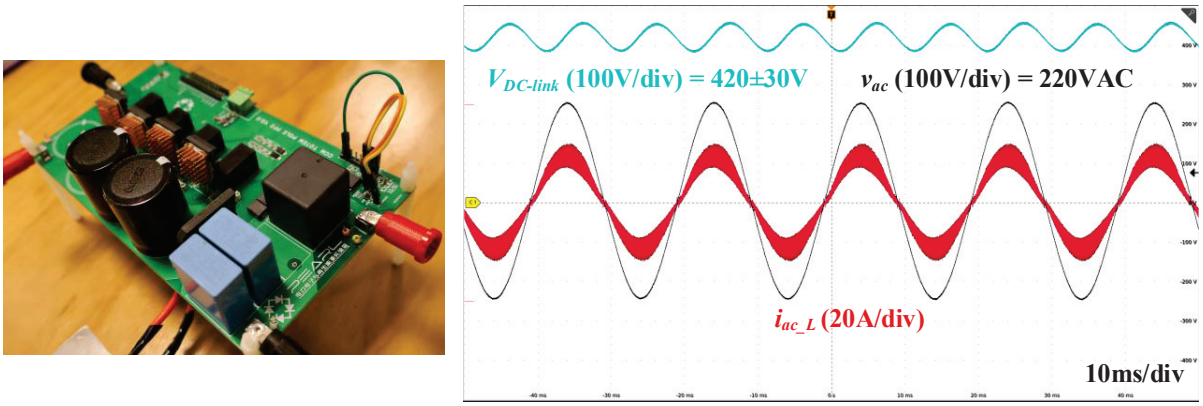

Fig. 7. Prototype and steady-state waveforms of the PFC stage under full load.

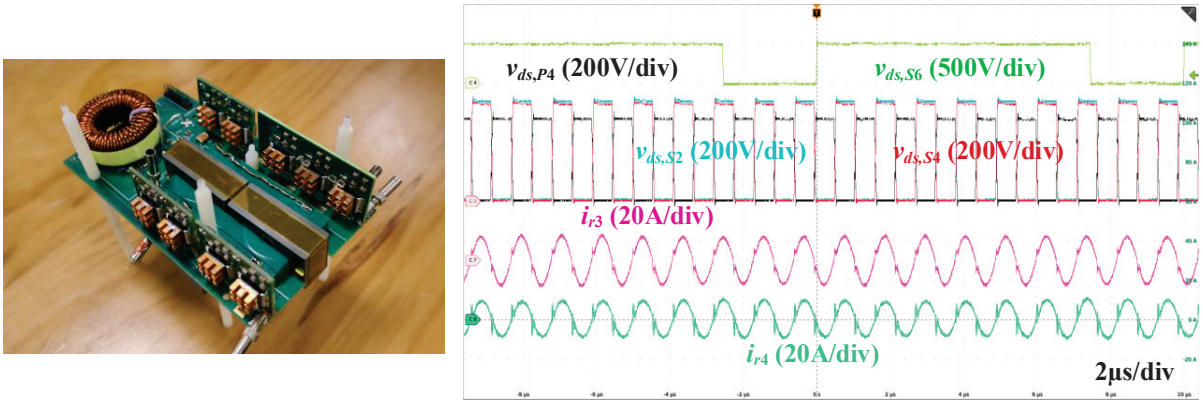

Fig. 8. Prototype and steady-state waveforms of the isolated DC/DC stage at $V_{DC-link} = 420\,\text{V}$, $V_B = 850\,\text{V}$, $P_B = 3.3\,\text{kW}$.

$V_{DC-link} = 420\,\text{V}$, $V_B = 850\,\text{V}$, and $P_B = 3.3\,\text{kW}$ are shown in Fig. 8.

Joint testing of both stages was performed. The steady-state key waveforms of the complete OBC for 220 V input with $V_B = 600\,\text{V}$ and $V_B = 900\,\text{V}$ are presented in Fig. 9a and Fig. 9b, respectively. Consistent with the analysis, $V_{DC-link}$, V_{B1}, and V_{B2} all exhibit significant 100 Hz ripple. The ripple components on V_{B1} and V_{B2} are opposite in phase, yielding a ripple-free net output V_B. As V_B increases, the DC bias of V_{B2} rises while V_{B1} remains essentially unchanged.

The measured full-load charging efficiency across the battery-voltage range is plotted in Fig. 10. With the DCX operating near 1 MHz, the prototype achieves efficiencies above 95.7% over the entire tested range, reaching a peak of 95.96%. These results confirm the proposed two-stage architecture delivers high efficiency and validates its performance across a wide voltage span.

V. Conclusions

This paper analyzed the limitations of APD circuits and proposed a novel two-stage OBC architecture that integrates APD with PPP. The proposed architecture reduces the required capacitance for absorbing twice-line-frequency power ripple by over 50% compared with conventional solutions. By enabling the isolated DC/DC stage to operate the CLLC resonant converter in DCX mode, the design achieves high efficiency and improved power density at resonant frequencies up to 1 MHz. The architecture leverages both power-decoupling capacitors and the isolated transformer to enhance overall power density. A 3.3 kW prototype (220 V input, 600–900 V output) was implemented; it uses only 440 μF of electrolytic capacitance for 100 Hz ripple absorption and maintains high efficiency across the tested voltage range, experimentally validating the proposed concept.

Acknowledgment

The authors thank Hengdian Group DMEGC Magnetics Co., Ltd. for providing high-frequency magnetic core samples and Infineon Technologies for supplying 650 V GaN HEMT devices.

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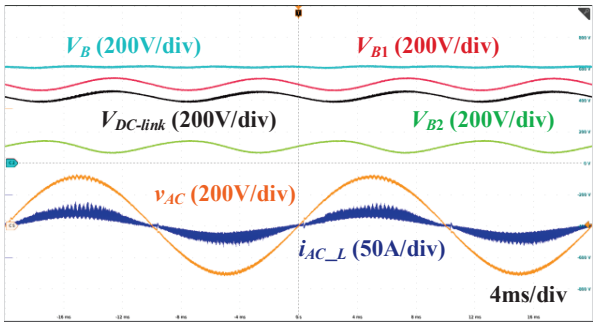
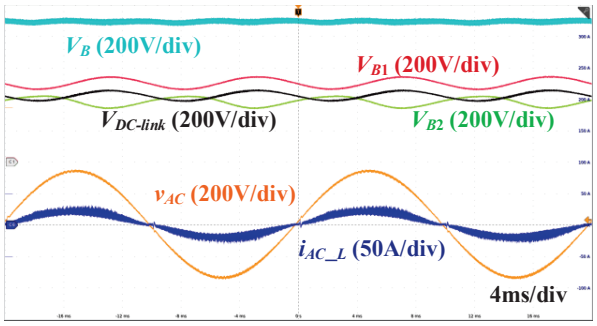


(a) $V_{AC} = 220\,\text{VAC},\ V_B = 600\,\text{V},\ P_B = 3.3\,\text{kW}$



(b) $V_{AC} = 220\,\text{VAC},\ V_B = 900\,\text{V},\ P_B = 3.3\,\text{kW}$

Fig. 9. Steady-state waveforms of the integrated OBC under two representative operating points.

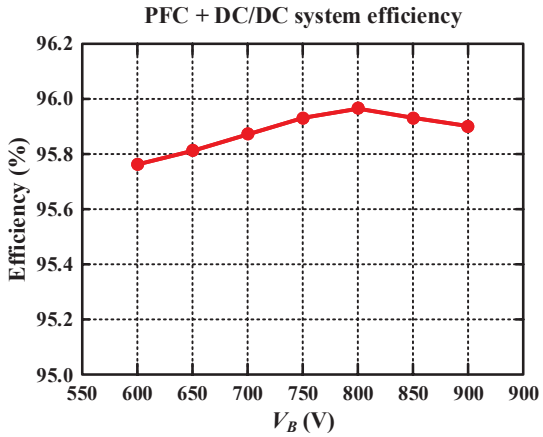


Fig. 10. Measured efficiency with different battery voltage under 3.3 kW charging power.

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