Adaptive Virtual Bus Strategy for Electrolytic Capacitorless DAB Microinverters

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***Abstract*—In residential photovoltaic (PV) systems, microinverters link the PV panels to the ac bus. Conventionally, these microinverters incorporate a stable dc bus that relies on bulky and unreliable electrolytic capacitors. To improve, we propose an adaptive virtual bus strategy for DAB microinverter, which removes the electrolytic capacitors. The microinverter features a quasi-single-stage design interconnected by a virtual bus, which exhibits a notable double-line-frequency voltage ripple. The front-end employs a boost converter to elevate the low PV voltage and regulate the voltage of the virtual bus. The back-end utilizes a dual-active-bridge (DAB) inverter to transform the oscillating virtual bus voltage into the desired ac output. This architecture facilitates active power decoupling (APD) for enhanced power density by buffering mismatched power on the minimized bus capacitors and dynamically adjusting the operational state of the DAB inverter. Furthermore, by decoupling the control algorithms of the two parts, we reduce the number of required voltage and current sensors, thereby simplifying the overall control system. To validate the concept, a GaN-based prototype rated at 200 W and 600 kHz maximum is designed and tested. This prototype achieved a peak efficiency of 92.67%.**

***Index Terms*—Active power decoupling (APD), dual-active-bridge (DAB), gallium nitride (GaN), microinverter, virtual bus.**

I. Introduction

As global demand for clean energy continues to grow, distributed photovoltaic (PV) systems are gaining increasing attention due to their adaptability and scalability in residential power systems [1]. In residential PV systems shown in Fig. 1, the microinverter is the key module as it enhances efficiency and reduces the cost of installation and maintenance [2]. Given the requirements of residential PV systems, the microinverter is desired to maintain continuous stable PV current, galvanic isolation, high power density, high reliability, low control complexity, and low component count simultaneously.

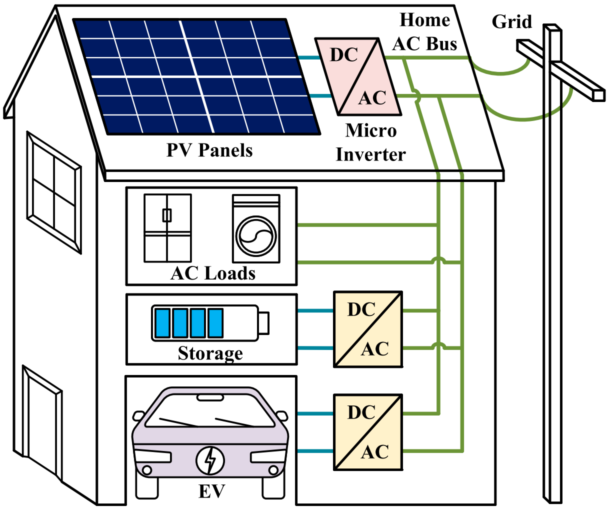

Fig. 1. Structure diagram of a residential PV system.

For grid-connected microinverters, galvanic isolation is essential for safety, due to the common-mode leakage currents [3], [4]. Conventional microinverters employ a two-stage architecture: a front-end dc–dc converter stage boosts the low PV voltage to a high dc bus voltage, while the back-end inverter stage ensures high-quality ac power output. Large electrolytic capacitor bank at dc bus maintains a stable dc input for the inverter [5]. In contrast, single-stage solutions directly transform low PV voltage into line-frequency ac voltage with reduced component count. However, it necessitates more sophisticated control [6].

Among the classical isolated topologies, flyback-based inverter stands out due to its simple structure and reliability [7]. For zero-voltage switching (ZVS), an active-clamping circuit can be employed to absorb the leakage energy and improve efficiency [8]. However, the power capability is limited, resulting in lower power density. LLC-based inverters are widely studied [9]. However, small magnetizing inductance is necessary to

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adapt to the wide operating range. This leads to high circulating current and degraded efficiency [10]. Dual-active-bridge (DAB) based solutions offer better transformer utilization [11], [12]. However, the control algorithm is complex due to the nonlinear gain characteristics [13]. Basic DAB inverters utilize single-phase shift (SPS) modulation, but this comes at the cost of limited soft-switching range and high reactive power when the port voltage varies [14]. In [15], variable-frequency extended-phase shift (EPS) modulation is used to suppress the reactive power and to linearize the relationship between the output current and phase shift.

Beyond topology innovations, single-phase inverters inherently face power mismatch between the dc and ac ports, which enforces an energy storage unit to buffer the double line-frequency instantaneous power [16]. Most solutions use a large electrolytic capacitor bank as the dc bus [17]. However, electrolytic capacitor faces challenges due to its limited lifespan, large equivalent series resistance (ESR), and poor reliability [18], [19]. In addition, the double line-frequency dc-link ripple generates heat on the buffer capacitor bank, further shortening its lifespan and raising the system cost [20]. Besides, the electrolytic capacitor bank is always bulky, increasing the system volume and decreasing the power density significantly [21]. An alternative solution is to use the active power decoupling (APD) circuits, which transfer the mismatch power through an active switching circuit to other buffer capacitors that are away from the dc-link [22]. With a larger double line-frequency voltage ripple for the decoupling capacitors, the capacitance can be reduced, making it feasible to use longer-life film or ceramic capacitors, thereby extending the system lifetime with squeezed volume [23].

To achieve APD, research focuses on both topologies and control strategies. Common APD circuits are often in series or parallel with the PV port. Commonly used topologies include boost, buck, and H-bridge, with differential inverter or split-capacitor designs [24], [25], [26], [27], [28], [29]. On the other hand, research on control strategies focuses on achieving precise regulation of decoupling capacitor voltage and enhancing the efficiency of decoupling circuits. To this end, various control strategies—including proportional-integral (PI), proportional-resonant (PR), bang-bang, and model predictive control-have been employed. These approaches are designed to ensure accurate voltage regulation within decoupling circuits and boost overall performance [30], [31], [32], [33], [34]. These typical APD solutions use decoupling circuits to replace the bus capacitors, requiring a nearly constant bus voltage, which results in the need for complex control methods and precise sampling of voltage and current to enhance performance, posing challenges for control system design.

In contrast to the fixed bus voltage solutions, operating with a modulated bus can also reduce bus capacitance requirements. This method of intentionally increasing bus voltage ripple to reduce the bus capacitance significantly has been previously applied in LED and fuel cell applications [35], [36]. Nevertheless, few studies have explored this method for power decoupling. In [37], a novel approach using a simple pulse-width modulation (PWM) method is proposed in an H-bridge inverter to reduce double line-frequency harmonic, effectively lowering bus capacitance. This method maintains the quality of the ac output while intentionally introducing significant ripple in the dc bus voltage. However, it only verifies the feasibility of using modulated bus voltage to reduce double line-frequency power ripple, while power oscillation elimination at the dc port is not addressed. In [38], an ultra-fast maximum power point tracking (MPPT) algorithm is implemented under modulated bus operation on a differential power processing flyback-based inverter. Still, high dc-link voltage requirements and limited bus voltage oscillation range make it unsuitable for microinverters in residential PV systems. Moreover, accurately controlling the current flowing into the decoupling capacitors remains a significant challenge, further complicating its practical implementation.

In this article, we propose a novel adaptive virtual bus strategy for electrolytic capacitorless quasisingle-stage DAB microinverter. The proposed strategy exhibits the following key contributions.

1) The virtual bus features an adaptive voltage ripple at double line frequency, enabling power decoupling functionality, a substantial reduction in bus capacitance, and elimination of the requirement for electrolytic capacitors.
2) Control algorithms between the two parts are decoupled, which significantly reduces the number of sensors required and simplifies the overall control system. Compared with conventional APD circuits, the proposed method notably decreases control complexity.

The system employs a front-end boost converter to step up the PV voltage, thereby reducing current stress. It maintains continuous current flow and regulates the dc bias of the virtual bus. Operating in critical conduction mode (CRM), the boost converter achieves zero-voltage switching (ZVS) for GaN HEMTs through current zero-crossing prediction (ZCP) technology, eliminating the need for additional high-frequency current sensors. The back-end DAB inverter, with a wide gain range, adapts seamlessly to the voltage oscillation of the virtual bus, achieving adaptive energy buffering. Consequently, by implementing the solution, the mismatched power is efficiently buffered on the adaptive virtual bus, ensuring stable dc power and maintaining high ac power quality. This approach offers a streamlined and efficient solution for residential PV systems.

The rest of the article is organized as follows. Section II presents the operating principles of the microinverter. Section III introduces the system's control strategy. In Section IV, design considerations are presented. Experimental results are provided to verify the proposed solution in Section V. Finally, Section VI concludes this article.

II. OPERATING PRINCIPLES

Fig. 2 illustrates the schematic of the quasi-single-stage DAB microinverter. It consists of a front-end boost converter and a back-end DAB inverter connected by a virtual bus. For the boost converter, a synchronous rectifier (SR) replaces the conventional diode to realize CRM with reduced switching loss. Since the PV input voltage is relatively low, the boost

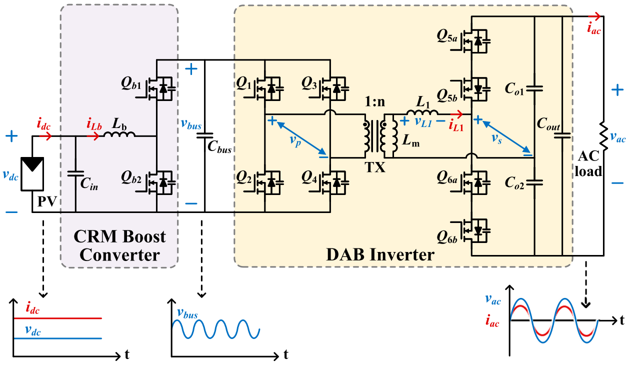


Fig. 2. Schematic of the adopted quasi-single-stage DAB microinverter.

converter can step up the voltage to simplify the design of the back-end DAB inverter and reduce the current stress. The main purpose of the boost converter is to control the dc bias bus voltage and filter double line-frequency power. The DAB inverter consists of a full bridge on the primary side and a secondary side voltage doubler rectifier composed of switches and capacitors, linked by a high-frequency transformer TX. The transformer turns ratio is $1:n$, and L_1 is the equivalent value of transformer leakage inductance on the secondary side. Because the magnetizing inductance L_m is much larger than the leakage inductance, it can be considered as an open circuit during analysis. This DAB inverter converts the oscillating bus voltage into a controlled ac output.

A. Adaptive Virtual Bus

The power flow diagram is shown in Fig. 3. The transmission power plays an important role in determining the switching actions of the boost converter and DAB inverter. In the boost converter, the transmission power P_{Boost} determines the average inductor current i_{avg}, which affects the switching instants. As for the DAB inverter, the transmission power P_{DAB} determines the root-mean-square (rms) value of output ac current i_o, thereby determining the phase shifts. Therefore, by controlling their transmission powers, the working state of the entire microinverter is determined.

Assuming the expected transmission power of the microinverter is P, and considering the power at both dc and ac ports, the instantaneous dc power p_{dc} equals the transmission power since it remains constant. In contrast, the instantaneous ac power p_{ac} oscillates with the ac port voltage and current. Suppose the instantaneous voltage and current at the ac port are as follows:

$$\begin{aligned} v_{\text{ac}}(t) &= \sqrt{2}V_{\text{rms}}\sin(\omega t) \\ i_{\text{ac}}(t) &= \sqrt{2}I_{\text{rms}}\sin(\omega t+\varphi) \end{aligned} \tag{1}$$

where V_{rms} and I_{rms} represent the rms value of ac voltage and current, respectively.

Then the instantaneous ac port transmission power p_{ac} can be derived as

$$\begin{aligned} p_{\text{ac}}(t) &= v_{\text{ac}}(t)i_{\text{ac}}(t) \\ &= V_{\text{rms}}I_{\text{rms}}\cos(\varphi) - V_{\text{rms}}I_{\text{rms}}\cos(2\omega t+\varphi). \end{aligned} \tag{2}$$

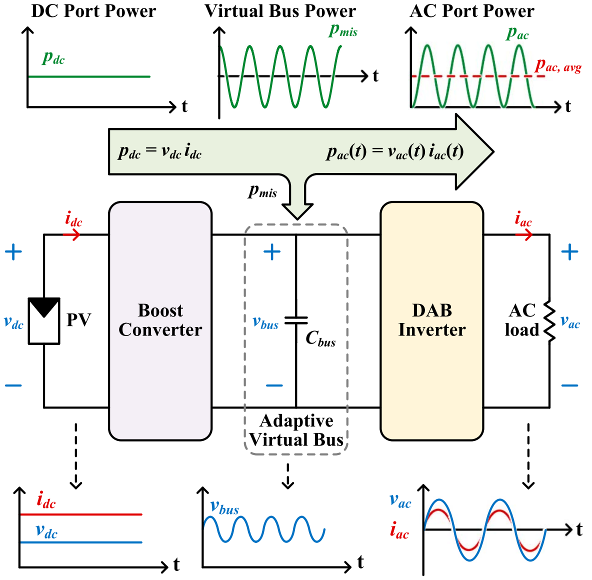


Fig. 3. Power flow diagram illustrating the concept of the virtual bus.

In (2), the former term is a constant, representing the dc bias of the ac port power, while the latter represents the double line-frequency oscillating power. For simplicity, the ac load is assumed resistive. In that case, the former term equals P, and the latter term, representing the mismatch power, should be buffered by C_{bus}. The following equation about v_{bus} can be obtained:

$$p_{\text{mis}} = \frac{1}{2}C_{\text{bus}}\frac{dv_{\text{bus}}^2}{dt} = V_{\text{rms}}I_{\text{rms}}\cos(2\omega t) \tag{3}$$

where $p_{\text{mis}} = p_{\text{dc}} - p_{\text{ac}}$ represents the mismatch power flowing into the virtual bus capacitors.

When the current flows into capacitors, the voltage rises, and the power direction is positive. In this process, it can be regarded as the dc input power, which equals the transmission power of the microinverter P, being shared by the bus capacitors and back-end DAB inverter. The voltage at the bus capacitors includes a dc bias component, denoted as V_{bias}. Based on the energy balance, the v_{bus} can be derived as

$$v_{\text{bus}} = \sqrt{\frac{P}{\omega C_{\text{bus}}}\sin(2\omega t) + V_{\text{bias}}^2}. \tag{4}$$

Therefore, based on (4), the oscillating virtual bus voltage is derived. Based on these analyses, the driving pattern and key waveforms at the line frequency scale are shown in Fig. 4.

B. CRM ZCP Boost Converter

The front-end boost converter operates in the current ZCP-based CRM to achieve ZVS at high switching frequency. The adopted ZCP method eliminates the usage of high-frequency current sensor.

The working waveforms of the CRM ZCP boost converter are shown in Fig. 5. The typical CRM operation can be divided into several stages. During the $Q_{b1,2}$ conduction stages T_{on} and T_{SR}, the inductor current can be calculated by inductor charging equation, while in deadtime stages T_{df} and T_{dr} it needs to be

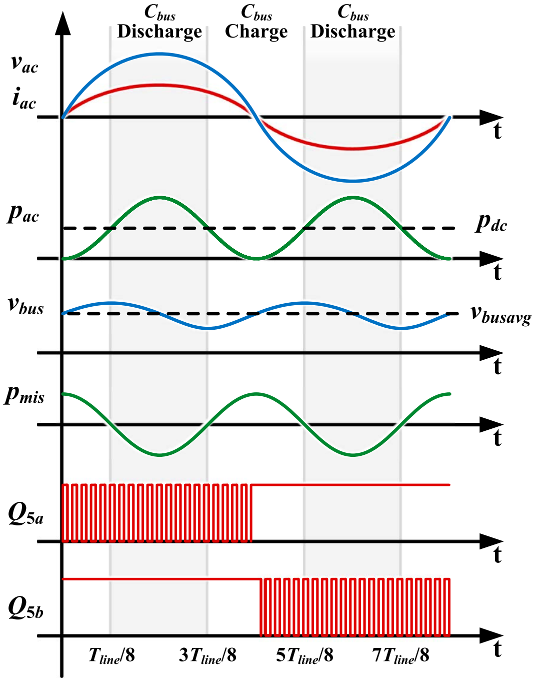
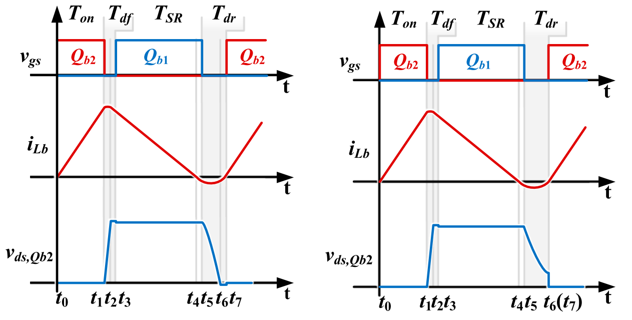


Fig. 4. Driving pattern and key waveforms at line frequency scale.



(a) (b)

Fig. 5. Working waveform of CRM ZCP boost converter: (a) ZVS case; and (b) valley switching case.

calculated by resonant equations. In T_{dr}, whether the ZVS of Q_{b2} can be realized is determined by the v_{dc} and v_{bus}. When $v_{\text{dc}} \leq 0.5v_{\text{bus}}$, ZVS can be realized. Otherwise, only valley switching is possible.

By calculating the energy storage and the energy flow between the source and the load at the beginning and end of the resonant period, the inductor current can be estimated at the start and end of the resonant period. Take t_1 to t_2 as an example

$$\frac{1}{2}L_b i_{Lb}^2(t_1) + 2Q_{\text{tot}}v_{\text{dc}} = \frac{1}{2}L_b i_{Lb}^2(t_2) + Q_{\text{tot}}v_{\text{bus}}. \tag{5}$$

In (5), Q_{tot} represents the amount of charge flowing through the switch during the resonant period. Using (5), the inductor current after the resonant period can be estimated from the inductor current before the resonant period.

Therefore, as shown in Fig. 6, the control strategy of the ZCP can be analyzed as follows. First, the average inductor current

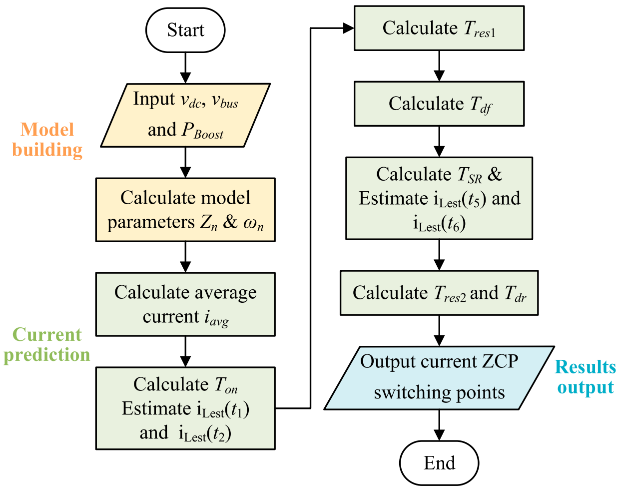


Fig. 6. Flowchart of zero current prediction of the boost converter.

I_{avg} should be calculated. With the average inductor current established, as the current waveform approximates a triangular shape, the inductor charging time T_{on} can be calculated, which directly affects the transmission power. I_{avg} and T_{on} can be expressed as

$$\frac{P}{v_{\text{dc}}} = i_{\text{avg}} = \frac{v_{\text{dc}}T_{\text{on}}Z_n - L_b(v_{\text{bus}} - v_{\text{dc}})}{2Z_nL_b} \tag{6}$$

$$T_{\text{on}} = \frac{2Z_nL_bi_{\text{avg}} + L_b(v_{\text{bus}} - v_{\text{dc}})}{Z_nv_{\text{dc}}} \tag{7}$$

where $Z_n = \sqrt{L_b/2C_{\text{oss}}}$ is the characteristic impedance, with C_{oss} denoting the parasitic capacitance.

In T_{df}, because the inductor current i_{Lb} is sufficiently large, allowing for rapid realization of ZVS for Q_{b1}. The resonance can be approximated using trapezoidal approximation. The deadtime T_{df} should be greater than resonant time T_{res1}. $i_{\text{Lest}}(t_x)$ represents the estimated inductor current at time t_x

$$T_{df} \geq T_{\text{res1}} = \frac{4Q_{\text{tot}}}{i_{\text{Lest}}(t_1) + i_{\text{Lest}}(t_2)}. \tag{8}$$

In the inductor discharging period, to simplify the analysis, we consider the SR to be ideal, which implies $i_{\text{Lest}}(t_5) = 0$. Then, the T_{SR} is shown as

$$T_{\text{SR}} = \frac{i_{\text{Lest}}(t_2)L_b}{v_{\text{bus}} - v_{\text{dc}}}. \tag{9}$$

Moving on, in T_{dr}, an equivalent approximation cannot be made due to the small average current. Therefore, the calculation of the resonant period needs to be performed using first-order LC response calculations as

$$T_{dr} = \begin{cases} T_{\text{res2}} - \dfrac{i_{\text{Lest}}(t_6)L_b}{V_D + v_{\text{dc}}}, & v_{\text{dc}} \leq 0.5v_{\text{bus}} \\ \dfrac{\pi}{\omega_n}, & v_{\text{dc}} > 0.5v_{\text{bus}} \end{cases} \tag{10}$$

where $\omega_n = 1/\sqrt{2C_{\text{oss}}L_b}$ is the resonant frequency and V_D denotes the source-drain forward voltage. T_{res2} represents the resonant time in T_{dr}, which is calculated through trajectory

$$T_{\text{res2}} = \frac{\pi + \arctan(i_{\text{Lest}}(t_6)Z_n/v_{\text{dc}})}{\omega_n}. \tag{11}$$

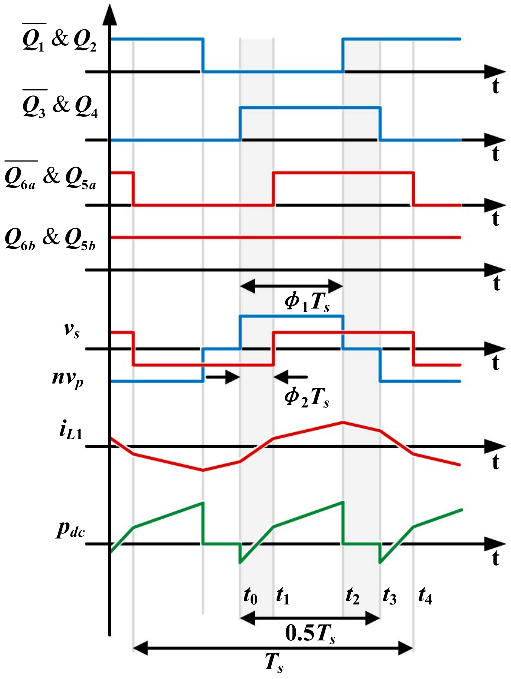


Fig. 7. DAB steady-state waveforms in EPS mode.

Based on the method, the conduction times of switches can be estimated using the input and output voltages and the expected transmission power of the boost converter.

C. DAB Inverter

EPS modulation is adopted in the DAB inverter. Its working waveforms during the positive ac half cycle are shown in Fig. 7. Since the switching frequency is much higher than the line frequency, the ac voltage can be considered constant at the switching frequency scale. Under EPS, primary switches operate at 50% duty cycle. As for secondary switches Q_5 and Q_6, Q_{5b} and Q_{6b} remain on during the positive half cycle, while Q_{5a} and Q_{6a} operate at 50% duty cycle to match the primary side switches. In the negative half cycle, this relationship reverses to adapt to the reverse ac voltage.

In Fig. 7, Q_3&Q_4 leg acts as the master phase, with other legs as slave phases. The phase shift between Q_3&Q_4 leg and Q_1&Q_2 leg is noted as ϕ_1, while phase shift between Q_3&Q_4 leg and Q_5&Q_6 leg is noted as ϕ_2.

To derive the output current, first calculate the slopes using the inductor charging equation $L_1 di_{L1}/dt = v_{L1}$

$$\frac{di_{L1}}{dt} = \begin{cases} (nv_{\text{bus}} + 0.5v_{\text{ac}})/L_1, (t_0 - t_1) \\ (nv_{\text{bus}} - 0.5v_{\text{ac}})/L_1, (t_1 - t_2) \\ (-0.5v_{\text{ac}})/L_1, \qquad (t_2 - t_3). \end{cases} \tag{12}$$

Accordingly, the currents at t_1, t_2 and t_3 can be calculated by the symmetry of the inductor current waveform about the x-axis, which means $i_{L1}(t_0) = -i_{L1}(t_3)$

$$\begin{cases} i_{L1}(t_1) = \frac{T_s}{2L_1}(2nv_{\text{bus}}\phi_2 - nv_{\text{bus}}\phi_1 + 0.25v_{\text{ac}}) \\ i_{L1}(t_2) = \frac{T_s}{2L_1}(v_{\text{ac}}\phi_2 + (nv_{\text{bus}} - v_{\text{ac}})\phi_1 + 0.25v_{\text{ac}}) \\ i_{L1}(t_3) = \frac{T_s}{2L_1}(v_{\text{ac}}\phi_2 + nv_{\text{bus}}\phi_1 - 0.25v_{\text{ac}}). \end{cases} \tag{13}$$

Therefore, the output current can be calculated by integrating i_{L1}. The t_1 to t_4 period represents a complete power output interval because of constant positive v_s voltage during the period

$$\begin{aligned} i_o &= \frac{1}{T_s}\int_{t_1}^{t_4} i_{L1}(t)\,dt \\ &= \frac{nv_{\text{bus}}}{2L_1 f_s}\left(-\phi_1^2 - 2\phi_2^2 + 2\phi_1\phi_2 + \frac{\phi_1}{2}\right). \end{aligned} \tag{14}$$

Considering (14), there are three variables in the equation: two phase shifts and the switching frequency. These free variables make the control algorithm design complex. Therefore, the relationship between the two phase shifts can be considered linear. Besides, $nv_{\text{bus}}/2L_1$ is a constant coefficient. By making the switching frequency f_s relate to the phase shifts rather than fixed, variable terms are eliminated in the equation, thereby simplifying the output current equation. The relationships between variables are

$$\begin{aligned} \phi_2 &= k\phi_1 \\ f_s &= (1 - 2(2k^2 - 2k + 1)\phi_1)f_{\text{smax}} \end{aligned} \tag{15}$$

where k is the coefficient to adjust phase shifts and f_{smax} is the frequency upper limit, determined by set working conditions.

Thus, (14) can be simplified as

$$i_o = \frac{nv_{\text{bus}}}{4L_1 f_{\text{smax}}}\phi_1 \tag{16}$$

where $nv_{\text{bus}}/4L_1 f_{\text{smax}}$ is the constant coefficient throughout an entire cycle.

In (16), the output current is linearly related to ϕ_1, greatly simplifying control.

However, to ensure the DAB inverter operates in the mode shown in Fig. 7, the range of ϕ_1 is limited to 0–0.5. Otherwise, the working waveform would change. But there is still a possibility that ϕ_1 may exceed the range. Therefore, a control method is needed to regulate the output current when ϕ_1 exceeds the range.

Based on (14), when ϕ_1 reaches the upper limit, it can be fixed and no longer considered to have a linear relationship with i_o. In that case, f_s becomes the controlled variable, while both ϕ_1 and ϕ_2 are set as constants. f_s can be derived as follows:

$$f_s = \frac{nv_{\text{bus}}\phi_1}{4L_1 i_o}(1 - 2\phi_1(2k^2 - 2k + 1)). \tag{17}$$

Thus, for the DAB inverter, when ϕ_1 is within the range, the ac output is controlled by regulating ϕ_1, while ϕ_1 exceeds the range, the ac output is controlled by controlling f_s instead. The expected ac output current is determined by the expected transmission power.

III. CONTROL STRATEGY

A. Virtual Bus Voltage Regulation

For the proposed adaptive virtual bus strategy, the front-end and back-end controls are separated. The boost converter and DAB inverter can work independently by utilizing sampled voltages. Unlike the conventional modulated bus solutions, the adaptive virtual bus solution is power-controlled by controlling the boost input current and DAB output current, while bus voltage oscillation is not directly controlled. With this approach, the virtual bus capacitors can buffer not only the double line-frequency mismatch power but also the higher-order harmonic mismatch power. However, the voltage of the virtual bus is not completely uncontrolled, the bus dc bias voltage needs to be regulated, otherwise the system would lose stability.

To regulate the virtual bus dc bias voltage, the difference in transmission power between the front-end and back-end can be modulated. When the dc bias voltage is lower than the expected value, the front-end transmission power increases, allowing higher power to be injected into the bus capacitors, while the back-end still transmits the fixed power. This raises the dc bias voltage and vice versa. The dc bias voltage controlling equation is shown as

$$\Delta P = \frac{1}{2} C_{\text{bus}} (V_{\text{busset}}^2 - v_{\text{bus}}^2) \times 2 f_{\text{line}} \tag{18}$$

where V_{busset} is the expected dc bias voltage, and P represents the expected transmission power. The relationship between the expected transmission power of the microinverter and the two parts' powers is $P_{\text{DAB}} = P, P_{\text{Boost}} = P + \Delta P$.

However, due to the oscillating bus voltage, it is not always possible to accurately sample the dc bias voltage. As shown in Fig. 4, when the ac voltage crosses zero, the bus voltage is exactly equal to its dc bias voltage. Therefore, sampling the bus voltage at this instant can directly represent the dc bias voltage. This relationship can also be derived from (4).

B. Control Algorithm

The flowchart of the control algorithm is shown in Fig. 8. It can be seen that the controls of the boost converter and DAB inverter are separate. For the DAB inverter, only v_{bus} needs to be sampled to regulate the output current, while in the boost converter, v_{bus} and v_{dc} need to be sampled. Their transmission powers can be determined by expected transmission power and the virtual bus dc bias voltage control method to keep the system stable.

Another noticeable thing is the ac output direction, which can be determined by reference to the sinusoidal waveform. As shown in Fig. 4, during the positive half-cycle of ac output voltage, Q_{5b} and Q_{6b} are constantly on to reduce switching loss, while Q_{5a} and Q_{6a} are the high frequency switches. During the negative half-cycle, their roles are exchanged, $Q_{5\text{b}}$ and $Q_{6\text{b}}$ function as the high frequency switches.

C. Master/Slave Phase Exchanging Control

The ZVS condition of each half-bridge can be derived by i_{L1} at the switching point, that is, the currents in (13) should be greater than 0. According to these conditions, it is found that under all operating conditions of the DAB inverter, the master phase cannot achieve ZVS, while the slave phases can achieve ZVS in most cases. This results in unbalanced heating of the two half-bridges in the DAB primary side, due to additional heat generated by the switching loss.

To address the uneven heating caused by different ZVS conditions, and given that the ZVS condition of a half-bridge depends on whether it is the master phase, the heating of the two primary side half-bridges can be balanced by exchanging the master phase.

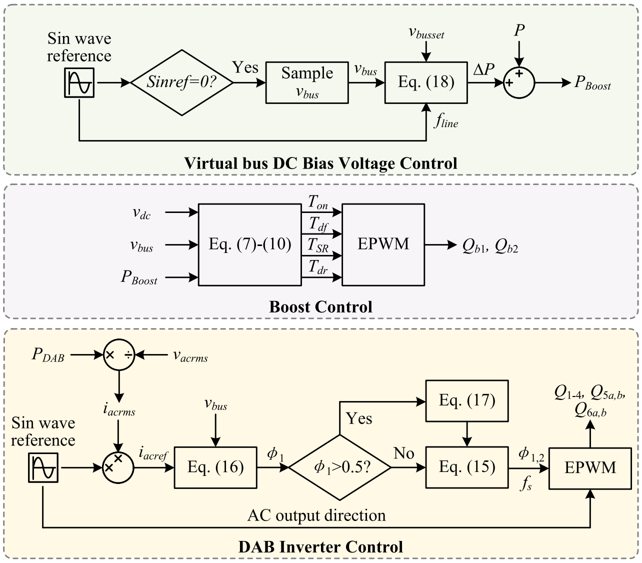


Fig. 8. Control algorithm flowchart.

Since the master phase of the DAB inverter is not fixed, the two primary half-bridges can alternate as the master phase to balance heating. In this case, to maintain a consistent output, the operating states of the two slave phases should also change. To ensure that the switching process does not affect the operation of the microinverter, the exchange occurs at the zero-crossing point of the ac voltage. In the actual control algorithm, when the ac output is positive, the Q_3 and Q_4 half-bridge acts as the master phase, and when the ac output is negative, the Q_1 and Q_2 half-bridge becomes the master phase.

IV. DESIGN CONSIDERATIONS

A. Virtual Bus Capacitor C_{bus}

The virtual bus capacitors C_{bus} are used to buffer the mismatched power p_{mis}. Based on Fig. 4, the proportion of total power mismatch during a charge period to total power can be derived. Considering the power mismatch from $T_{\text{line}}/8$ to $3T_{\text{line}}/8$

$$\frac{\left| \int_{T_{\text{line}}/8}^{3T_{\text{line}}/8} p_{\text{mis}}\, dt \right|}{\int_0^{T_{\text{line}}/2} p_{\text{dc}}\, dt} = \frac{1}{\pi} \approx 32\%. \tag{19}$$

We can conclude from (19) and Fig. 4 that the energy buffer capacitors need to handle 32% of the transmission power.

In the microinverter, to accommodate household applications, gallium nitride (GaN) devices EPC2215 are selected as the switches for the boost converter and primary side of the DAB inverter, and GS66508T is selected as the secondary side switches. EPC2215 has a voltage rating of 200 V. The maximum virtual bus voltage is set at 160 V, corresponding to 80% of the GaN HEMT voltage rating. As for minimum virtual bus voltage, considering typical residential PV panel rating power and output voltage, $50V$ is the lower boundary. This is because the virtual bus voltage should not be lower than the input voltage.

Then, based on (3) and (19), the minimum value of the bus capacitors can be calculated

$$\frac{1}{2}C_{\text{bus}}(v_{\text{busmax}}^2 - v_{\text{busmin}}^2) \times 2f_{\text{line}} \geq 0.32P. \tag{20}$$

After the capacitance is determined, the type of capacitors also needs to be selected. Ceramic capacitors, rather than film capacitors, are selected as bus capacitors to improve the power density. However, for ceramic capacitors, the dc bias characteristic is noteworthy. As the dc bias voltage increases, the equivalent capacitance decreases, significantly reducing the available capacitance. For the common ceramic capacitor, when the dc bias voltage reaches half of its rated voltage, its capacitor charge rate drops to around 25%. This problem directly results in the energy stored in the virtual bus capacitors no longer being proportional to the square of its voltage. Consequently, in (18) and (20), adjusting the dc bias of bus voltage becomes less accurate, and it becomes difficult to calculate the required minimum capacitance. However, in the proposed APD solution based on adaptive bus operation, obtaining the accurate bus capacitance is not necessary. Indeed, the inaccurate bus capacitance would only result in a certain deviation of the bus voltage dc bias from the expected value. As for the required minimum capacitance, it is only necessary to ensure that the bus maintains sufficient capacitance when the capacitor charge rate drops.

B. Boost Inductor L_b

The boost inductor L_b is designed based on the switching frequency of the boost converter. For the boost converter working in CRM, after the input and output voltages are determined, L_b directly influences the working frequency by the following equation:

$$f_{s,\text{boost}} \approx \frac{v_{\text{dc}}^2(v_{\text{bus}} - v_{\text{dc}})}{2P_{\text{Boost}}L_b v_{\text{bus}}}. \tag{21}$$

Besides, not only the required inductance needs to be considered, but also the selection of magnetic core size and its feasibility of implementation. Given the demand for higher frequency to reduce volume, litz wire is utilized to suppress the ac losses in the inductor, significantly reducing copper losses caused by the skin effect. Therefore, the core volume, window area, and operating frequency need to be considered.

C. High Frequency Transformer

The transformer is one of the key components in the DAB inverter. To achieve higher power density, the transformer leakage inductance is considered as the inductor L_1 in DAB. However, this increases the complexity of transformer design, as it not only requires achieving the desired turn ratio but also means optimizing the required leakage inductance. The expected leakage inductance can be determined by (16).

Considering the very light loads case, the phase shifts become trivial. Due to the controller's internal time delay, an excessively small phase shift may not be accurately output, leading to erroneous switching signals. To avoid such errors, the output signals of the controller are cut off during this period, which is called controller deadtime. However, the deadtime would introduce harmonic distortion and efficiency degradation. Based on (16), a larger leakage inductance can result in larger phase shifts, thereby effectively reducing the deadtime during which the controller cannot output due to the small phase shift.

TABLE I
DESIGN PARAMETERS

Symbols	Description	Value
v_{dc}	DC input voltage	10–25 V
v_{acrms}	AC output voltage rms	110 V
v_{bus}	Virtual bus voltage	50–100 V
f_{line}	AC output freq.	50 Hz
P	Rated power	200 W
f_{smax}	DAB max sw. freq.	600 kHz
$f_{s,\text{boost}}$	Boost sw. freq. range	192 kHz–1.13 MHz
$C_{o1,2}$	Voltage-doubling cap.	2.8 uF 1206B104K251NT×6 + FS55X225K251EGG
C_{out}	Output cap.	2.2 uF C322J225J20L230A60
C_{bus}	Bus cap.	210 uF@100 V GRM32EC72A106KE05×336
L_m	Magnetizing ind.	6.1 mH DMR51H, RM12, 20:24 turns
L_1	Leakage ind.	6.875 uH
n	Transformer turns ratio	1.2
L_b	Boost ind.	1.04 uH DMR51W, RM8, 4 turns

To ensure the transformer meets the turns ratio and leakage inductance requirements, the winding configuration is important, considering the window area. Besides, a high-frequency magnetic core and proper litz wire need to be selected from limited options to reduce losses.

V. EXPERIMENTAL RESULTS

To validate the proposed method, a 200 W prototype is built, with its parameters detailed in Table I. The bus capacitors are ceramic capacitors from muRata rated at 100 V. To achieve a higher voltage rating in the experiment, these capacitors are connected in series to achieve 200 V withstand voltage, and a capacitor bank is formed by stacking six soldered layers. TMS320F280049C from Texas Instruments is used as the controller. Both the inductor and transformer cores are sourced from DMEGC, with the inductor using an RM8 core made of DMR51W material, and the transformer utilizing an RM12 core made of DMR51H material. The system control diagram is shown in Fig. 9 and the GaN-based microinverter prototype is presented in Fig. 10.

Fig. 11 presents the steady-state experimental waveforms at line-frequency scale. During the operation, the input dc voltage remains constant, with the dc port current i_{dc} exhibiting small

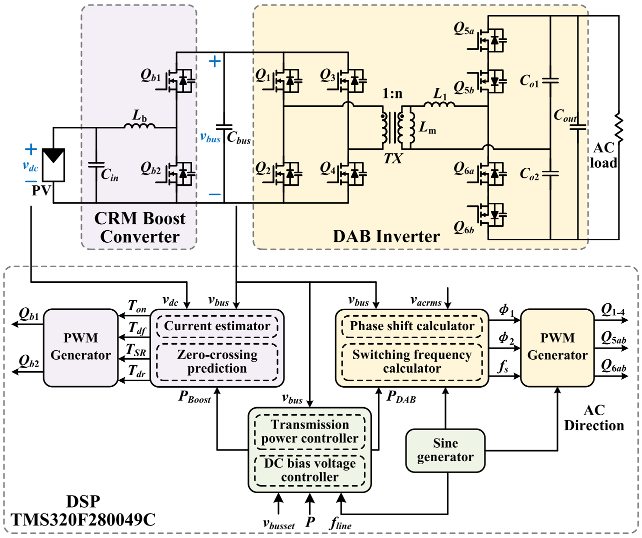


Fig. 9. System control diagram.

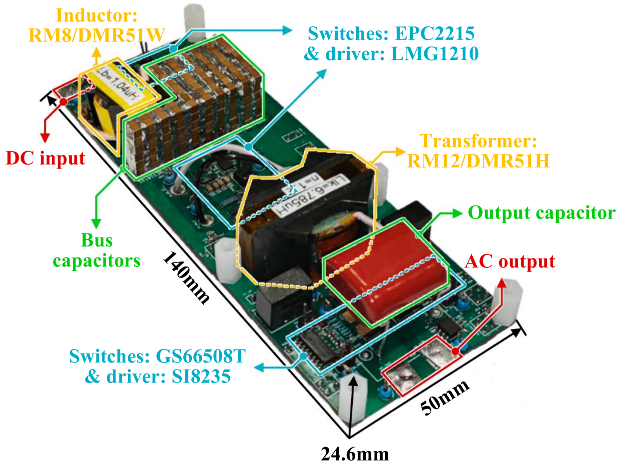


Fig. 10. Picture of the designed GaN-based microinverter prototype.

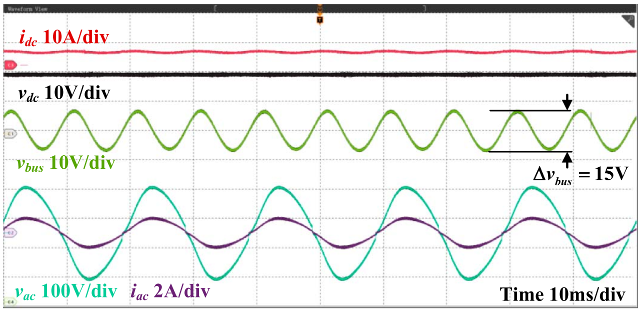
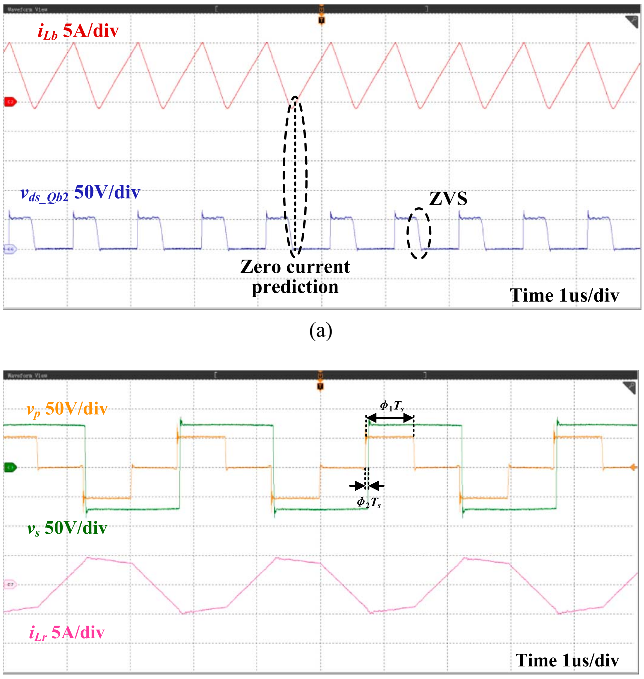


Fig. 11. Experimental steady-state waveforms at line-frequency scale under 80 W output power.



(a)

(b)

Fig. 12. Experimental steady-state waveforms at switching frequency scale: (a) boost converter; and (b) DAB inverter.

double line-frequency harmonics, featuring the oscillating amplitude of 0.39 A. Simultaneously, the virtual bus voltage has significant oscillation, ranging from 51 to 66 V. The output voltage exhibits a well-formed sinusoidal waveform. The experimental results validate the feasibility of the proposed concept of the adaptive virtual bus.

Fig. 12 shows the key steady-state waveforms of the front-end boost converter and the back-end DAB inverter at their switching frequencies. In Fig. 12(a), the boost inductor current i_{Lb} and the drain-source voltage of the bottom GaN HEMT v_{ds_Qb2} are captured. When i_{Lb} crosses zero from negative to positive, the bottom GaN HEMT Q_2 would turn ON promptly, while the v_{ds_Qb2} reaches zero at every cycle, which validates a clear ZVS turn-ON. These experimental results validate the effectiveness of the current ZCP method in the quasi-single-stage DAB inverter. Besides, Fig. 12(b) presents the primary-side voltage v_p, secondary-side voltage v_s of the transformer, and the DAB inductor current i_{L1} waveforms. Due to the adopted EPS modulation, the primary side exhibits a three-level voltage waveform.

Fig. 13 shows the measured conversion efficiency under different output powers. The maximum efficiency is 92.67% at 170 W with 600 kHz peak switching frequency. When the output power is low, switching loss and transformer core loss dominate, resulting in lower efficiency. As the power increases, the proportion of fixed loss gradually decreases, and the overall efficiency increases until the conduction loss dominates, at which point the efficiency will decrease again.

Fig. 14 shows the thermal image of the microinverter under full rating power. The maximum temperature point of the system is 64.6 °C, located at the boost converter. The temperature rise is within an acceptable range, indicating that the thermal design is reasonable.

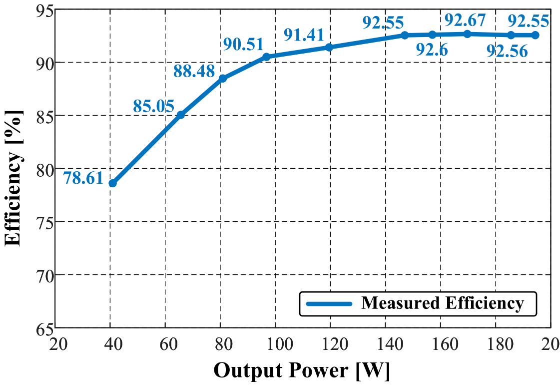


Fig. 13. Measured efficiency versus output power.

Fig. 14. Full rating thermal image.

VI. CONCLUSION

This article introduces a novel adaptive virtual bus strategy for electrolytic capacitorless quasi-single-stage DAB microinverter in residential scenarios. The virtual bus has a significant double line-frequency adaptive voltage ripple, making bus capacitance significantly reduce. Therefore, the bulky electrolytic capacitor can be removed, thus reducing the volume and improving the reliability of the microinverter. By placing a boost converter before the DAB inverter, the PV voltage can be stepped up while maintaining continuous current flow. Meanwhile, the front-end boost converter operates in CRM, using current ZCP for ZVS realization without the necessity for any current sensor. The back-end DAB has wide gain range to adapt to the oscillating virtual bus voltage. Therefore, the mismatch power would be buffered on the adaptive virtual bus, while the dc power remains stable and ac power quality is unaffected. Besides, the approach decouples the controls of two parts, significantly reducing the number of required voltage and current sensors. Compared with conventional APD circuits, the proposed method significantly reduces the control complexity. The efficacy of the microinverter is demonstrated through experiments with a 200 W-rated prototype. The results demonstrate that this method can achieve the desired power decoupling effect.

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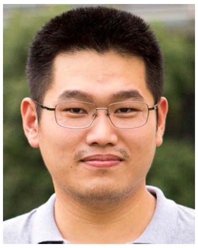

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