Synchronous Bridge Rectifier for MHz Resonant Converter Based on Digital Control

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***Abstract*—This article presents the development of a general MHz synchronous rectifier (SR) designed for resonant converters. It examines the potential losses in a nonideal SR, encompassing driving losses, conduction losses, switching losses, and body-diode losses. When employing the drain–source voltage for synchronization, it investigates the signal delay and mismatch introduced by detector, driver, and transistor parasitic to elucidate the challenges faced by a digital controller. To address these issues, this article proposes a fast synchronous phase control coupled with a slow adaptive dead-time control to dynamically modulate the driving signal. Experimentally, it implemented and tested a 60-W, 6.78-MHz rectifier in a wireless charger. The SR achieved a peak efficiency of 97.7%, ensuring at least a 5.0% efficiency improvement compared to a passive rectifier.**

***Index Terms*—Adaptive control, MHz resonant converter, synchronous rectifier (SR).**

I. Introduction

RESONANT converters have shown great promise due to their soft-switching capabilities, leading to widespread use in high-frequency applications [1], [2]. Synchronous rectifiers (SRs) are typically employed to minimize conduction losses, particularly in low-voltage, high-current situations [3], [4], [5]. Another major demand for MHz SR arises from wireless chargers [6], [7], which have selected 6.78 MHz as the standard resonant frequency due to constraints in the industrial, scientific, and medical bands [8]. Considering the shift toward high-frequency conversion and the significant demand from MHz wireless chargers, the development of a MHz SR has become especially crucial.

SRs have been extensively explored in recent decades [9], [10], [11]. In conventional isolated resonant converters, a central controller typically generates a synchronization signal for the secondary rectifier by referencing the primary driving signal [12]. However, this method becomes impractical for MHz wireless chargers due to the physical separation between the transmitter (TX) and receiver (RX). To address this challenge, synchronization signals need to be generated based on the voltage or current of RX components [13], [14]. Considering the limited bandwidth and the large size of current-sensing circuits, the most attractive solution is to directly use the SR's drain–source voltage to produce the synchronization signal [15]. By utilizing the drain–source voltage, it becomes feasible to integrate the sensing circuit, driving circuit, and the transistor itself into an SR integrated circuit (IC), effectively mimicking a diode from the perspective of the package [16], [17].

There is a growing demand for MHz SR through sensing the drain–source voltage [18], [19]. A common challenge lies in compensating for signal delay and mismatch. For instance, a self-synchronizing delay compensation method has been introduced in [20] to address delay for MHz resonant converters. The delay caused by parasitic parameters is examined and digitally compensated in [21], enhancing the load range of SR. However, most existing solutions focus on compensating a fixed delay, which is insufficient for variable delays or uncertain mismatch. Such variable factors and their mechanism are briefly discussed for a 13.56 MHz converter in an open-loop manner [22]. To tackle this issue, a Class E SR has been proposed in [23] to achieve dynamic compensation in a closed-loop manner. Nevertheless, this approach relies on high-performance field-programmable gate array (FPGA) and a smooth drain–source voltage. For MHz bridge rectifiers, the high dv/dt makes it challenging to accurately sense the zero-crossing point when the voltage is compared with a reference. Thus, managing the uncertain delay and mismatch becomes difficult when the drain–source voltage experiences high dv/dt.

This article details the development of a 6.78 MHz bridge SR employing digital control. To manage uncertainties in signal delay and mismatch, the timing for switching the SR ON and OFF is identified as a critical factor in the analysis of loss models. This approach reveals that how these timing variables interact to minimize losses. By utilizing the straightforward drain–source voltage, synchronized phase control and adaptive dead-time

Received 24 December 2024; revised 30 April 2025; accepted 10 June 2025. Date of publication 16 June 2025; date of current version 27 August 2025. This work was supported in part by the National Natural Science Foundation of China under Grant 52477013 and in part by Lingang Laboratory under Grant LG-GG 202402-06-10. Recommended for publication by Associate Editor T. Long. *(Corresponding author: Minfan Fu.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2025.3580095.

Digital Object Identifier 10.1109/TPEL.2025.3580095

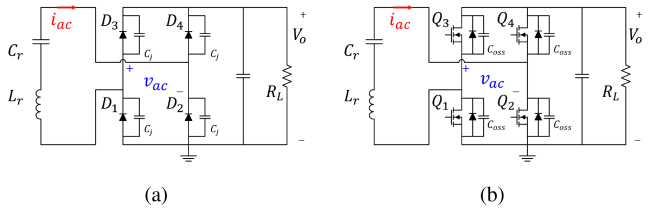


Fig. 1. Bridge rectifier. (a) Passive rectifier. (b) Active rectifier.

control are proposed, which allow for rapid optimization of turn-ON timing and gradual adjustment of dead time. This method relies solely on a universal controller and standard analog circuits, facilitating the implementation of a highly efficient SR across a wide range of load conditions.

II. MHz Bridge Rectifier

A. Challenges of High-Frequency Rectifier

In Fig. 1(a), a voltage-type rectifier can be seen as the inverse configuration of a voltage-source inverter. The dc output is smoothed by a single capacitor, and assuming that a small ripple in the output voltage results in a square voltage v_{ac} at the ac terminal. When this rectifier is paired with the resonant tank, resonance ensures a sinusoidal excitation i_{ac}. The change in polarity of i_{ac} causes diode current commutation. Replacing each diode with a MOSFET, as shown in Fig. 1(b), is well-known for significantly reducing conduction losses, a topic widely explored in the context of kHz rectification. Consequently, the goal of using active devices is to ideally replicate the behavior of passive ones.

The passive bridge naturally commutates based on the polarity of i_{ac}. In the absence of junction capacitance, this commutation would occur instantaneously. However, due to the nonlinear characteristics of junction capacitance C_j, the transition time during diode commutation becomes significant. Fig. 2(a) depicts the waveforms of a passive rectifier operating at MHz frequencies. The dc output voltage remains constant, while variations in i_{ac} correspond to changes in power levels. Different power levels result in noticeable variations in transition time, resembling the dead-time concept found in active inverters. The actual conduction time of the diode is represented by the duty cycle D, where a longer transition time leads to a smaller D. During the transition period, the load current must fully charge or discharge the junction capacitance, which requires more time for lighter loads. As the operating frequency increases, this effect becomes more pronounced, significantly influencing the rectifier's mode of operation. Therefore, an active bridge must account for this transition time and aim to emulate the behavior of a diode.

The challenge in designing an active rectifier is not only to account for the transition time caused by the junction capacitance but also to determine the appropriate turn-ON instance and duty cycle based on the sensed state of the circuit. Assuming that the gate signal is applied at the correct moment without any delay, the waveform of an ideal active rectifier is depicted in Fig. 2(b). It is important to note that this waveform serves as a target reference rather than a practical representation. When i_{ac} crosses

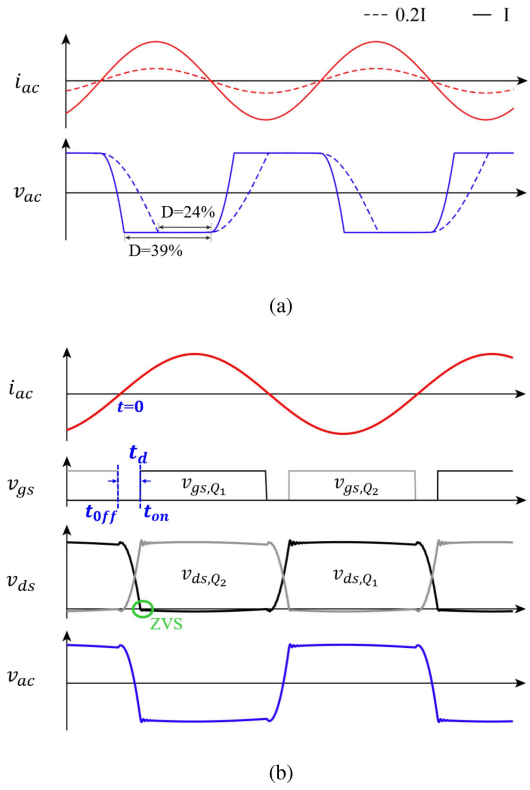


Fig. 2. Simulation waveforms. (a) Passive rectifier. (b) Active rectifier.

zero and becomes positive at $t = 0$ (denoting this as the time reference), the rectifier should promptly detect this transition and deactivate Q_2 and Q_3 at $t = 0$. Ideally, this requires ensuring that $t_{\text{off}} = 0$. During the transition period, or dead time, the junction capacitance of Q_2 is charged from zero to V_o at t_{on}. In summary, the two critical pieces of information for switching are the current-related t_{off} and the voltage-related t_{on}. For fixed frequency operation, such as in a 6.78 MHz wireless charger, the switching period is predetermined, making precise action at t_{on} and t_{off} essential for minimizing device losses. The optimal driving scheme should detect the triggering events, specifically v_{ds}, and execute the appropriate actions promptly.

B. Loss Analysis of SR

In high-frequency SR, the timing of turning ON and OFF is highly dependent on the accuracy of signal detector and the response time of gate driver. These factors critically impact system performance, making it essential to develop an accurate loss model for optimizing SR efficiency. This article uses a full-bridge rectification system as an example, operating at a nominal frequency of 6.78 MHz. This fixed-frequency rectifier is typically used in the RX of a wireless charger that adheres to the Airfuel standard. The output voltage and power are 24 V and 60 W, respectively. The additional SR parameters are listed in Table II.

When an SR achieves its optimal operating conditions as depicted in Fig. 2(b), the predominant sources of device losses are gate driving losses and conduction losses. The driving losses

TABLE I
SR PARAMETERS

Symbol	Value	Symbol	Value	Symbol	Value
f_s	6.78 MHZ	V_o	24 V	P_o	60 W
Q_g	4 nC	V_{gs}	5 V	I_{ac}	2.75 A
$r_{ds,on}$	16 mOhm	C_{gd}	10 pF	C_{oss}	120 pF

TABLE II
PARAMETERS OF THE VALIDATION SYSTEM

Symbol	Value	Symbol	Value	Symbol	Value
L_{tx}	850 nH	r_{tx}	0.20 Ω	C_{tx}	660 pF
L_{rx}	860 nH	r_{rx}	0.21 Ω	C_{rx}	665 pF
k	0.18	V_{in}	20 V	R_l	4∼12 Ω

can be expressed by

$$P_{\text{dri}} = Q_g V_{\text{gs}} f_s. \tag{1}$$

This type of loss is mainly influenced by the switching frequency f_s, the gate–source voltage V_{gs}, and the gate charge Q_g. Notably, it remains unaffected by the specific turn-ON and turn-OFF times, t_{on} and t_{off}. Assuming that the input current is defined as

$$i_{\text{ac}}(t) = I_{\text{ac}} \sin \omega_s t \tag{2}$$

the conduction losses caused by the device's on-resistance, $r_{\text{ds,on}}$, can be calculated as follows:

$$P_{\text{cond}} = f_s \int_{t_{\text{on}}}^{t_{\text{off}}+T_s/2} i_{\text{ac}}^2(t) r_{\text{ds,on}}\, dt$$
$$= I_{\text{ac}}^2 r_{\text{ds,on}} f_s \left(\frac{(T_s/2 - t_d)}{2} - \frac{\sin 2\omega t_{\text{off}} - \sin 2\omega t_{\text{on}}}{4(T_s/2 - t_d)} \right). \tag{3}$$

Therefore, the minimal device loss in optimal conditions can be described by

$$P_{\text{loss,opt}} = P_{\text{dri}} + P_{\text{cond}}. \tag{4}$$

The rectifier input voltage v_{ac} is approximated as a trapezoidal wave and can be expressed as a piecewise function

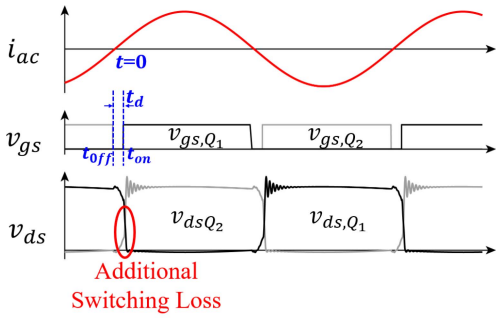
$$v_{\text{ac}} = \begin{cases} \frac{2V_o}{t_{\text{off}} - t_{\text{on}}}(t - t_{\text{on}}) + V_o, & t_{\text{off}} < t < t_{\text{on}} \\ -V_o, & t_{\text{on}} < t < \frac{T_s}{2} + t_{\text{off}}. \end{cases} \tag{5}$$

The output power is further derived as

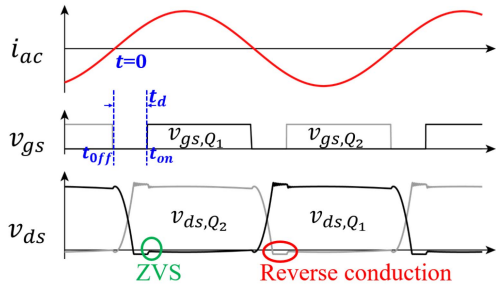
$$P_o = f_s \int_o^{T_s} v_{\text{ac}} i_{\text{ac}}\, dt$$
$$\approx \frac{1}{\pi} V_o I_{\text{ac}} (\cos \omega t_{\text{on}} + \cos \omega t_{\text{off}}). \tag{6}$$

This reveals that the output power decreases with the increasing t_{on} and t_{off}. In a low-frequency rectifier, it is approximately true that $t_{\text{on}} = t_{\text{off}} = 0$, and the output power capability is maximized. Considering that P_{cond} increases with the increasing t_{on} and t_{off}, and P_{dri} is independent of t_{on} and t_{off}, achieving higher rectification efficiency requires minimizing both t_{on} and t_{off}.

To achieve optimal operation, the driving circuit must sense the current information and immediately turn OFF the device.



(a)



(b)

Fig. 3. Simulation waveforms. (a) Case A: $t_d < t_c$. (b) Case B: $t_d > t_c$.

This is accomplished through the circuit's detection and driving logic. Any signal delay and mismatch in the circuit or control would lead to a positive t_{on}, thereby reducing efficiency. In Fig. 2(b), the length of the transient time is t_d

$$t_d = t_{\text{on}} - t_{\text{off}}. \tag{7}$$

The optimal t_d ensures that the driving circuit maintains the exact dead time required for the junction capacitance (C_{oss}) charging and discharging process. This critical dead time, denoted as t_c, can be calculated such that it guarantees

$$2C_{oss}V_o = \int_{t_{\text{off}}}^{t_{\text{off}}+t_c} i_{\text{ac}}\, dt. \tag{8}$$

Solving the above equation yields

$$t_c = \frac{1}{\omega} \cos^{-1} \left(\cos \omega t_{\text{off}} - \frac{2\omega C_{oss} V_o}{I_{\text{ac}}} \right) - t_{\text{off}}. \tag{9}$$

Under steady-state conditions, if the SR can ensure $t_{\text{off}} = 0$ and $t_d = t_c$, the efficiency will be maximized.

C. Loss Analysis of a Nonideal Active Rectifier

Due to the nonideal rectifier, it typically holds that $t_{\text{off}} > 0$ and $t_d < t_c$, which is classified as Case A. The rectifier's waveforms are shown in Fig. 3(a). Due to the insufficient dead time, the drain–source voltage is forced down to zero at the turn-ON instance t_{on}. The state transition cannot be completed instantaneously due to device's gate–source capacitor C_{gd}, leading to voltage ringing and additional switching losses. Considering

the rise time t_r caused by the miller platform, and the switching losses are derived as follows:

$$t_r = \frac{C_{\text{gd}} v_{\text{ds}}(t_{\text{off}})}{I_{\text{drive}}}$$

$$v_{\text{ds}}(t_{\text{off}}) = V_o - \frac{I_{\text{ac}}(\cos\omega t_{\text{on}} - \cos\omega t_{\text{off}})}{C_{\text{oss}}}$$

$$P_{\text{sw}} = f_s \int_{t_{\text{on}}}^{t_{\text{on}}+t_r} v_{\text{ds}} i_{\text{ds}}\, dt$$

$$\approx \frac{1}{2} f_s v_{\text{ds}}(t_{\text{off}}) i_{\text{rec}}(t_{\text{off}}) t_r. \tag{10}$$

Combining P_{sw} with P_{dri} and P_{cond}, the overall device loss for Case A is

$$P_{\text{loss,A}} = P_{\text{dri}} + P_{\text{cond}} + P_{\text{sw}}. \tag{11}$$

Another type of nonideal condition occurs when $t_{\text{off}} > 0$ and $t_d > t_c$, which is defined as Case B. The rectifier circuit's operating waveforms are shown in Fig. 3(b). During the dead time, the device's junction capacitance fully charges and discharges. At the turn-ON instance t_{on}, the drain–source voltage is clamped near zero, making the switching loss negligible. However, due to the extended dead time, the proportion of diode conduction loss increases due to the forward voltage drop V_F. This additional body diode loss is derived as follows:

$$P_{\text{dio}} = f_s \int_{t_{\text{off}}+t_c}^{t_{\text{on}}} V_F i_{\text{ac}}\, dt$$

$$= V_F I_{\text{ac}} \left(\cos\omega t_{\text{off}} - \frac{2C_{oss} V_o}{I_{\text{ac}}} - \cos\omega t_{\text{on}} \right). \tag{12}$$

Combining P_{dio} with P_{dri} from (1) and P_{cond} from (3), the overall device loss for Case B is derived as

$$P_{\text{loss,B}} = P_{\text{dri}} + P_{\text{cond}} + P_{\text{dio}}. \tag{13}$$

D. Influence of t_{off} and t_d

Considering the nonideal t_{off} and t_d, the overall loss can be derived based on (1), (3), (10), and (12)

$$P_{\text{loss}} = P_{\text{dri}} + P_{\text{cond}} + P_{\text{sw}} + P_{\text{dio}}. \tag{14}$$

Note that the above loss model is defined for model unification in different cases. Based on this model, the influence of t_{off} and t_d is illustrated in Fig. 4. The minimum-loss point (i.e., $t_{\text{off}} = 0$ and $t_d = t_c$) is shown as the green triangular mark. The blue surface represents additional switching losses of Case A due to the insufficient dead time, and the red surface represents the additional diode losses of Case B due to the forward voltage drop. Although any shift from the minimum-loss point would cause additional losses, it is clear that there still exists a valley curve in the loss surface. The projection of this valley is the black solid line in the bottom plane, indicating that t_d should be controlled dynamically instead of being fixed when t_{off} deviates from 0. In practice, the driving scheme should consider the coupling between t_{off} and t_d to improve rectifier efficiency dynamically and adaptively.

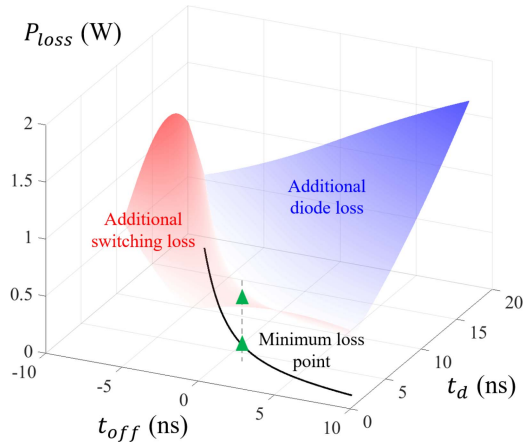


Fig. 4. Loss of the example SR.

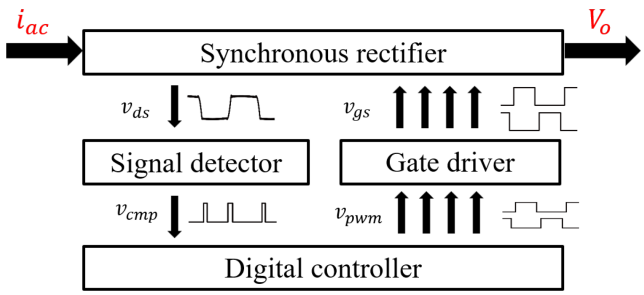


Fig. 5. Control configuration of the proposed SR.

III. SR With Adaptive Control

A. SR Configuration

Fig. 5 illustrates the control configuration of the proposed SR, which includes a signal detector, a digital controller, and a gate driver. In the signal detector, the drain–source voltage v_{ds} of the low-side device passes through a voltage clamping circuit and a comparator. This detector needs to generate a square wave voltage v_{cmp} that contains the zero-crossing information of v_{ds}. This information is further processed by the digital controller, which is responsible for producing the desired pulse-width modulation (PWM) signal v_{pwm} for the subsequent gate driver. The final gate driver is a commercial driving IC. Ideally, the resulting v_{gs} should almost align with i_{ac}. In sum, the proposed rectifier needs one drain–source voltage to generate four PWM signals based on the known driving logic.

Given the mature techniques available for signal detectors and gate drivers, the primary challenge and innovation lie in the design of the digital controller. It must compensate for circuit delays when generating the turn-OFF signal at t_{off}, and then produce the turn-ON signal based on the optimal t_d. Considering the limited computational capacity of the digital controller, the SR operates in an adaptive manner instead of a real-time manner. The subsequent subsections will initially explore the potential signal delays and mismatches induced by the external circuitry of the digital controller. Following this, the discussion will focus

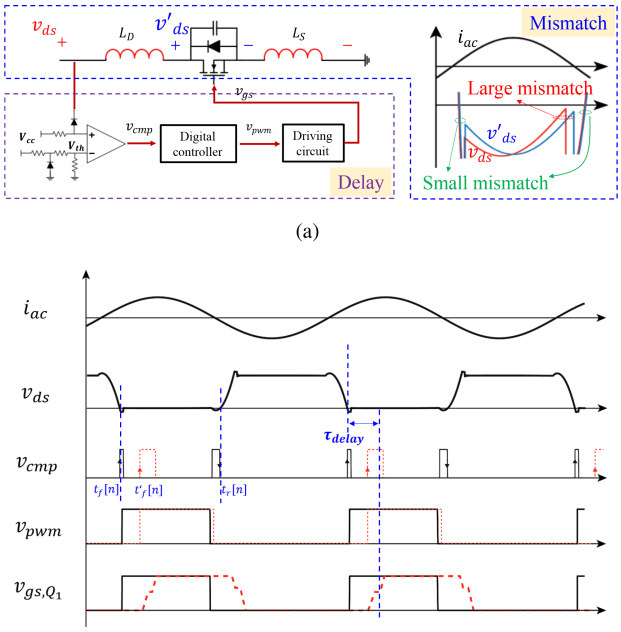


Fig. 6. Mechanism and influence of delay. (a) Circuit caused delay and mismatch delay. (b) Influence of a fixed delay.

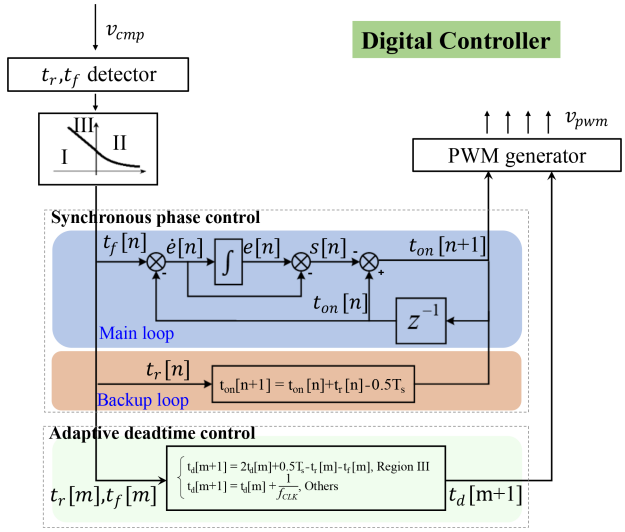


Fig. 7. Proposed digital controller.

on the computation and adaptive generation of $t_{\rm on}$ and t_d via the digital controller.

B. Signal Delay and Mismatch

Fig. 6(a) illustrates the potential delays introduced by the signal and power circuits. At the signal level, it is well-established that there is a relatively constant delay from $v_{\rm ds}$ to $v_{\rm gs}$, arising from components, such as the signal detector, digital controller, and gate driver. Furthermore, parasitic inductance within the transistor leads to uncertain mismatch, which are influenced by operating conditions, such as power level and switching frequency. Consequently, it is crucial to assess how these uncertainties affect SR performance.

Fig. 6(b) depicts the impact of delays on critical signals. In the absence of any delay in the signal circuit, the black solid line would represent the gradual progression of signal processing in an open-loop format for several key signals: $v_{\rm ds}$, $v_{\rm cmp}$, $v_{\rm pwm}$, and $v_{\rm gs}$, with the zero-crossing of $i_{\rm ac}$ serving as the reference point. Within the signal detector shown in Fig. 6(a), the high-level $v_{\rm ds}$ is clamped to V_{cc} by a diode before being input into a high-frequency comparator. The nonlinearity of the diode and the inherent delay of the comparator contribute to a total delay before reaching the digital controller, denoted as $\tau_{\rm in}$. Similarly, post the digital controller, delays exist between the signals $v_{\rm pwm}$ and $v_{\rm gs}$ due to the gate driver, and between $v_{\rm gs}$ and $v_{\rm ds}$ as a result of the transistor. These delays collectively define the total delay after the digital controller, labeled $\tau_{\rm out}$. In comparison to the black solid waveform, the red dotted waveform in Fig. 6(b) illustrates the effect of these delays. Given the operating frequency, these relatively fixed delays can be quantified and treated as constants, allowing for compensation within the digital controller.

Signal mismatches arise due to device parasitic inductance, specifically L_D and L_S, as depicted in Fig. 6(a). The sensed drain–source voltage can be expressed as

$$v_{\rm ds} = -\left(i_{\rm ac} r_{\rm ds,ON} + (L_D + L_S)\frac{di_{\rm ac}}{dt}\right) \tag{15}$$

where $r_{\rm ds,ON}$ represents the transistor's on-resistance. As illustrated in Fig. 6(a), the mismatch between $v_{\rm ds}^{'}$ (calculated without considering the inductance) and $v_{\rm ds}$ varies at the turn-ON and turn-OFF instances. Typically, commercial SRs require the magnitude information of $v_{\rm ds}$ for PWM generation, which can result in significant mismatches at the turn-OFF instance, particularly in high-frequency SRs. Consequently, leveraging the zero-crossing information of $v_{\rm ds}$, due to its smaller mismatch compared to $v_{\rm ds}^{'}$, is more advantageous.

C. Synchronous Phase Control

The proposed digital controller is depicted in Fig. 7(a). This controller requires two events from $v_{\rm cmp}$ as its input, corresponding to t_r and t_f in Fig. 6(b). It employs a synchronous phase control (SPC) to rapidly generate $t_{\rm on}$, updating the output every two switching periods. This control loop effectively addresses large and relatively fixed delays or mismatches. Concurrently, a slow adaptive dead-time control (ADC) is used to adjust t_d every eight switching periods. This control loop effectively manages uncertainties, ensuring that the SR operates at the minimum-loss point of Fig. 4.

The SPC of Fig. 7 includes a main loop and a backup loop. As shown in Fig. 6(b), the solid waveform (indicating no delay) illustrates the alignment between t_f and the rising edge of $v_{\rm pwm}$. Consequently, t_f is utilized in the main loop of Fig. 7, serving as the reference for generating $t_{\rm on}$. The main loop employs the widely recognized sliding mode control.

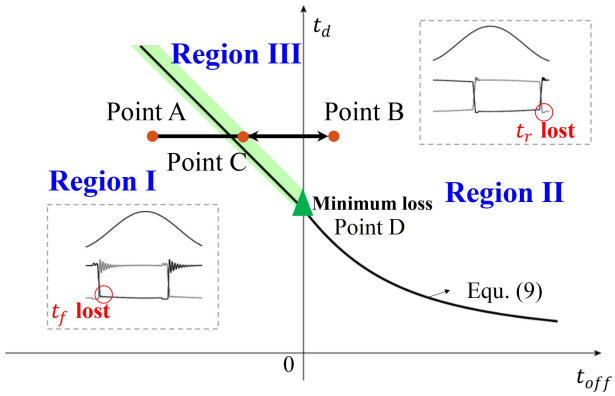


Fig. 8. Rectifier operating regions and sliding mode surface of the proposed method.

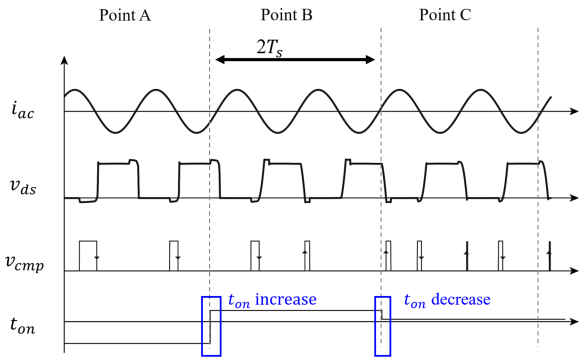


Fig. 9. SPC process.

The effectiveness of the main loop depends on the presence of t_f, which cannot be guaranteed under all operating conditions. Fig. 4 is simplified to a 2-D representation as shown in Fig. 8. The proposed control strategy aims to eventually converge to the solid black line. Based on the typical waveform of $v_{\rm ds}$, the detector circuit may fail to capture the $v_{\rm ds}$-induced t_f within Region I of Fig. 8. When t_d is insufficient for ensuring zero-voltage switching, t_f is lost because the transistor's body diode does not conduct. Under this scenario, the backup loop captures t_r and incrementally increases $t_{\rm off}$ to ensure the SR functions outside Region I.

Fig. 9 illustrates a typical control process to demonstrate the transition of operating points A, B, and C, as referenced in Fig. 8. Initially, the SR operates at Point A within Region I. The absence of t_f immediately activates the backup loop, which adjusts $t_{\rm on}$ to move the SR to Point B. It is important to note that within the SPC, t_d remains constant, and $t_{\rm on} = t_{\rm off} + t_d$. Subsequently, the main loop engages to reduce $t_{\rm on}$ toward reducing loss, identified as Point C. This control strategy gradually stabilizes the SR around the black solid line illustrated in Fig. 8, within the green bold-shaded area.

D. Adaptive Dead-time Control

The proposed SPC facilitates rapid adjustment of $t_{\rm on}$ every two switching periods. During this process, the dead time t_d is treated as a constant, ensuring the SR operates within the green-shaded area. Consequently, a slow ADC is necessary to finely tune t_d, as shown in Fig. 7. The ultimate goal is to reach Point D in Fig. 8, which is the minimum-loss point illustrated in Fig. 4.

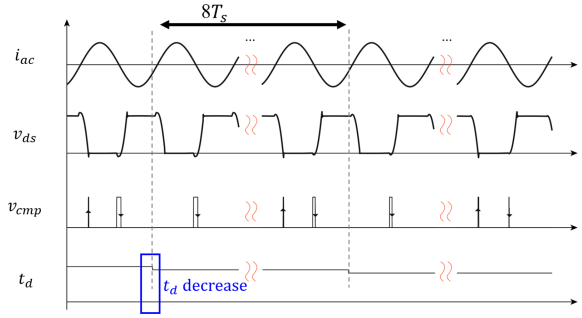


Fig. 10. ADC process.

At Point D, the target state is depicted by the black waveform in Fig. 6, characterized by $t_r = 0.5T_s$ and $t_f = t_d$. This implies the following relationship:

$$t_r + t_f = 0.5T_s + t_d. \tag{16}$$

The ADC loop functions by sensing and summing t_r and t_f. With a simple proportional control method, t_d is updated digitally as follows:

$$t_d[m+1] = t_d[m] + (t_d[m] - t_f[m]) + (0.5T_s - t_f[m]). \tag{17}$$

A typical ADC process is presented in Fig. 10, where t_d adaptively decreases over every eight switching periods.

Similar to the challenges faced in SPC, the sensed $v_{\rm ds}$ cannot guarantee the capture of t_r and t_f under all operating conditions. In Fig. 8, Region I results in the loss of t_f, Region II results in the loss of t_r, only Region III ensures the necessary input for (17), and $t_{\rm off} = 0$ is the dividing line of Region II and Region III. Consequently, when t_r or t_f is lost outside of Region III, the ADC slightly increases t_d to return the SR to Region III, as shown

$$t_d[m+1] = t_d[m] + \frac{1}{f_{\rm CLK}} \tag{18}$$

where $f_{\rm CLK}$ represents the clock frequency of the digital controller and can be considered as the minimum increment for t_d. The proposed ADC mechanism is illustrated in Fig. 7.

IV. Experimental Verification

An SS-compensated wireless charger is built in Fig. 11 for verification purposes. An SR-based system is compared with a benchmark using passive rectifier. The whole system consists of a full bridge inverter, coupling coils, and a full bridge rectifier. GaN HEMTs (EPC2014 C) are used in proposed SR and inverter. The digital controller is a commercial MCU (STM32H743). For the benchmark system, four Schottky diodes (NRVTS5100E) were used for the passive rectifier. All the other parameters are the same for both systems and given in Table II.

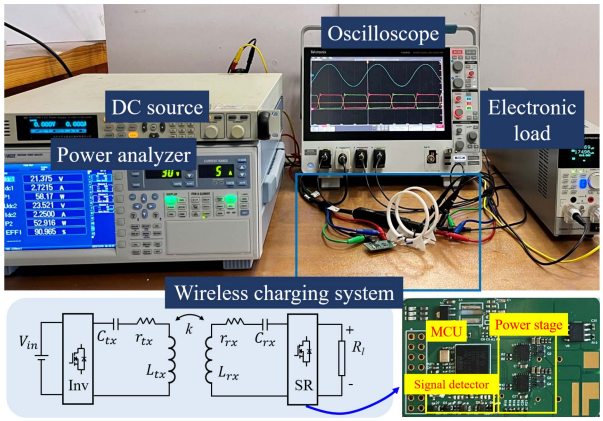
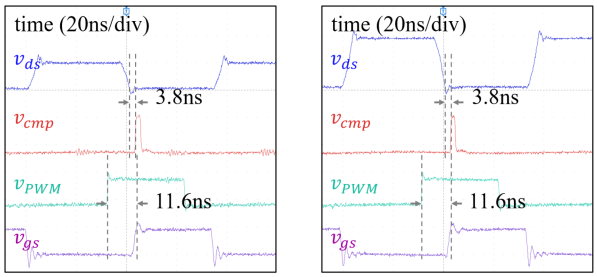


Fig. 11. Experimental setup of the 6.78-MHz wireless charger.



(a) (b)

Fig. 12. Influence of signal delay. (a) $V_o = 10V$. (b) $V_o = 20V$.

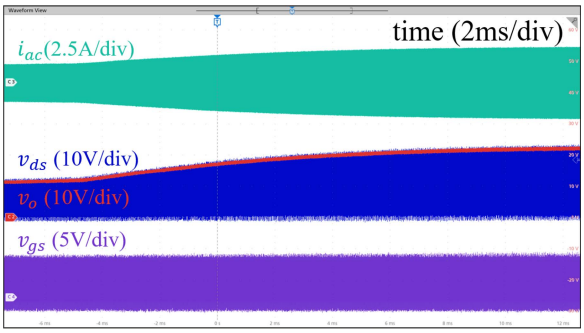
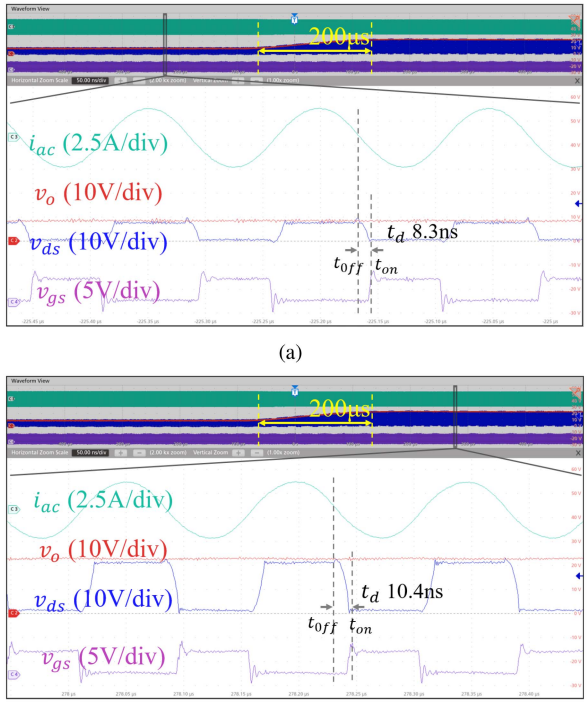


Fig. 13. Input transient waveforms of the system.

Fig. 12(a) and (b) shows the signal delay at different output voltage, which helps justified the analysis of Fig. 6. The delays of the comparator and gate driver are evident and occupy a substantial portion of the switching period in MHz systems, significantly impacting SR synchronization. Notably, the delay remains nearly constant across different operating conditions, indicating that it is determined by device characteristics rather than system states.

Fig. 13 shows the dynamic response of the SR-based system when the input voltage steps from 10 to 20 V. The rectifier input current (i_{ac}), output dc voltage (v_o), drain–source voltage (v_{gs}), and gate–source voltage (v_{ds}) are depicted. The output voltage rises smoothly as the system transitions between operating



(a)

(b)

Fig. 14. Load transient waveforms of the system. (a) $R_L = 4\Omega$. (b) $R_L = 12\Omega$.

conditions, demonstrating the dynamic stability and effective regulation of the proposed SR control.

Fig. 14(a) and (b) presents the system response during a dynamic load transition from 4 to 12 Ω. The upper part shows the long-term dynamic behavior, while the lower part zoom into the switching-cycle waveforms. Fig. 14(a) corresponds to the 4 Ω condition before the transition, and Fig. 14(b) to the 12 Ω condition after. Throughout the transition, the input ac current remains nearly constant due to the system's current regulation characteristics, while the output voltage increases and stabilizes. The source-drain voltages and gate-driving waveforms confirm the successful operation of the SR under varying conditions, with the dead time adaptively adjusting according to load variations, further verifying the robustness of the proposed method.

Fig. 15 compares the system efficiencies of the SR-based system ($\eta_{\text{sys,SR}}$) and the benchmark system ($\eta_{\text{sys,dio}}$) over various power levels. Efficiencies were primarily measured by a power analyzer, while single-stage efficiencies of the resonant tank (η_{tank}) and rectifier (η_{SR}) were further estimated based on Table II and the corresponding operating conditions. Note that the measurement of ac power is not accurate. The results show a clear efficiency improvement attributed to the SR, underscoring its necessity for MHz rectification. The SR achieves a peak efficiency of 98.1% (excluding driving loss) and 97.7% (including driving loss), while the overall system efficiency reaches a maximum of 91.4%. As shown in Fig. 15(b), the rectifier's maximum temperature is 52.8°C, with GaN device's temperature remaining below 50°C. Table III further benchmarks the design

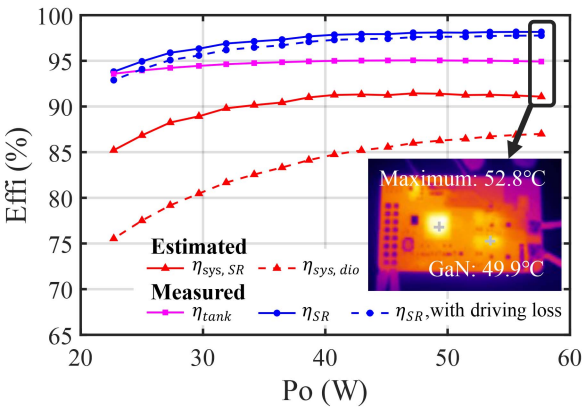


Fig. 15. Rectifier efficiency and system efficiency.

TABLE III
COMPARISON WITH PRIOR RESEARCH

Ref.	f_s (MHz)	Topology	t_d control	V_o (V)	P_o (W)	η_{SR} (%)
[24]	10	Class Φ2	NO	5	10	82.0
[13]	6.78	Class E	NO	48	194	94.6
[20]	6.78	Class E	NO	120	228	93.1
[25]	13.56	Class E	NO	40	300	93.0
[16]	13.56	Full-bridge	NO	2.5	0.248	94.8
[26]	6.78	Full-bridge	NO	5	6	91.5
[23]	6.78	Class E	Yes	24	120	97.0
[15]	6.78	Full-bridge	Yes	40	44.9	N/A
This	6.78	Full-bridge	Yes	24	60	97.7

against state-of-the-art MHz rectifiers, confirming the highest reported efficiency at 6.78 MHz.

V. CONCLUSION

This article presents the development of a bridge SR for MHz resonant power conversion. The typical operation mode of an active rectifier is analyzed, leading to the derivation of the SR loss model. The effects of two control variables are examined in depth, revealing their coupling in the context of loss minimization. Utilizing a simple signal detector and driver, the analysis of signal delay and mismatch explores the challenges faced by the digital controller. A fast SPC is combined with a slow ADC to dynamically adjust the turn-ON instance and dead time. Experimental results demonstrate that a 60-W 6.78-MHz system can achieve a peak SR efficiency of 97.7%.

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