A Hybrid Switched-Capacitor CDR 48 V/1 V Voltage Regulator

Ziyao Wang, *Student Member, IEEE*, Zehui Li, *Member, IEEE*, Xufeng Kou, *Senior Member, IEEE*, Minfan Fu, *Senior Member, IEEE*, and Haoyu Wang, *Senior Member, IEEE*

***Abstract*—In 48 V data center voltage-regulation applications, current-doubler rectifier (CDR) topology is a promising solution due to its high step-down ratio and structural simplicity. However, the hard-switching operation of its primary-side switches compromises conversion efficiency, increases voltage stress as load current rises, and generates voltage spikes. To address these limitations, this article proposes a single-stage hybrid switched-capacitor CDR 48-V/1-V voltage regulator. It features a stacked switched-capacitor primary structure. The capacitive voltage division reduces voltage stress on active switches. This enables low-voltage MOSFETs while maintaining zero-voltage switching (ZVS). A 1-MHz prototype converts 48–1 V and delivers a 100-A output current. Experimental results confirm reduced stress and robust ZVS with 93.4% peak efficiency.**

***Index Terms*—Current-doubler rectifier (CDR), high step-down ratio, switched-capacitor, zero-voltage switching (ZVS).**

I. Introduction

MODERN data centers employ a 48 V power bus to cut resistive power losses, elevate power delivery efficiency, reduce conductor sizing and cost, and deliver superior thermal management & power density versus the legacy 12 V bus [1], [2], as illustrated by the typical data-center power architecture in Fig. 1. However, this transition poses significant challenges for voltage regulator modules (VRMs). Achieving a 48:1 step-down ratio necessitates efficient mitigation of the large voltage gap and conversion losses [3]. To address the 48 V to 1 V conversion challenge, the conventional two-stage architecture typically cascades a fixed-ratio intermediate bus converter with multiphase buck regulators [4], [5]. Although this approach leverages compatibility with 12 V legacy systems, it suffers from low total efficiency and high component count [6].

Correspondingly, single-stage architectures have garnered significant research interest [7]. *LLC* topology is widely adopted due to its soft-switching capability [8]. However, it relies on frequency modulation, and system performance degrades in voltage regulation scenarios. The Sigma architecture [9], [10] addresses this challenge. Its partial power processing achieves a favorable efficiency–regulation tradeoff but increases system complexity and component stress.

To circumvent the control complexity while maintaining high current delivery, current-doubler rectifier (CDR) topology has emerged as a strong candidate. Operating as a transformer-isolated buck converter, it supports fixed-frequency PWM control—simplifying loop compensation and voltage regulation. This topology is commonly realized as the half-bridge CDR (HB-CDR) [11], [12]. Leveraging two interleaved inductors, the HB-CDR inherits the current-sharing capability of the multiphase buck converter, inherent ripple cancellation, and improved thermal performance for high-density applications.

However, the conventional HB-CDR requires structural refinement for efficient 48 V conversion [13]. Under standard PWM operation, the primary switches experience hard switching. Abrupt interruption of the leakage current generates severe voltage spikes, demanding high-voltage-rated devices. The phase-shifted full-bridge CDR converter [14] leverages leakage inductance to achieve primary-side zero-voltage switching (ZVS). Nevertheless, its switches endure the full input voltage, and the ZVS tends to fail at light load. A stacked primary structure [15] halves the static blocking voltage but retains hard switching. Active auxiliary circuits enable soft switching [16]. However, they induce excessive secondary-side circulating current, which increases conduction loss. Quasi-resonant techniques [17], [18] offer load-independent soft switching and high efficiency but require variable-frequency control, complicating regulation. Active clamping [19] suppresses voltage spikes and achieves zero-current switching (ZCS) but adds components, reducing power density and increasing cost.

To address voltage stress and switching losses without sacrificing simplicity, integrating flying capacitors into the primary structure offers a promising solution [20], [21]. These capacitors act as passive clamping cells, clamping switch voltage stress to a fraction of the input voltage while absorbing leakage energy and eliminating voltage spikes. The capacitive voltage-reduction mechanism has been demonstrated in hybrid switched-capacitor architectures. For instance, the series-capacitor buck [22], [23] utilizes a flying capacitor to halve voltage stress, thereby reducing switching losses. Similarly, high-order topologies such as the Dickson [24], [25] and modular LEGO architectures [26], [27] leverage capacitive stacking for higher step-down ratios,

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The authors are with the School of Information Science and Technology, ShanghaiTech University, Shanghai 201210, China (e-mail: wangzy22024@shanghaitech.edu.cn; lizh2@shanghaitech.edu.cn; kouxf@shanghaitech.edu.cn; fumf@shanghaitech.edu.cn; wanghy@shanghaitech.edu.cn).

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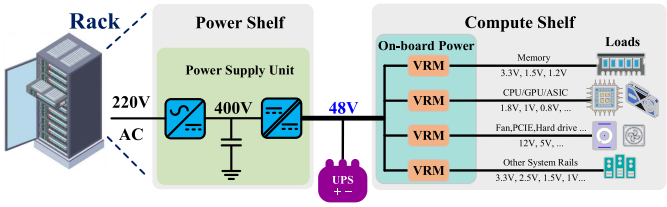


Fig. 1. 48 V data center power conversion architecture.

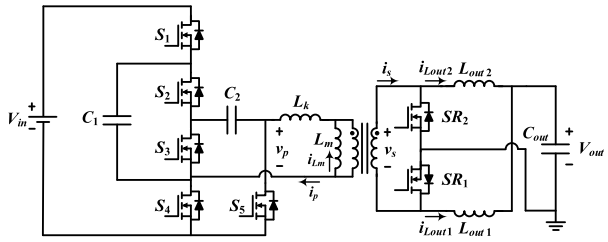


Fig. 2. Schematic of the proposed hybrid switched-capacitor CDR topology.

extending operational duty cycles. Moreover, capacitive voltage sharing reduces switch voltage stress, enabling lower-voltage MOSFETs with improved figure-of-merit (FOM), minimizing conduction and switching losses.

Inspired by this concept, we propose a hybrid switched-capacitor CDR 48-V/1-V converter in this article. By combining a stacked primary structure with CDR, the topology integrates the voltage-step-down feature of the switched-capacitor network and the current-doubling advantage of CDR. Key contributions include the following.

1) *Reduced voltage stress:* A 3:1 capacitive division in the stacked primary structure enables 40-V-rated MOSFETs with optimized FOM, minimizing conduction and switching losses.
2) *Wide-range ZVS:* Clamping the dynamic switching-voltage swing to $V_{in}/3$ drastically lowers resonant energy requirements. The transformer's leakage inductance alone ensures ZVS across broad load ranges without auxiliary circuits.
3) *High efficiency at high frequency:* Reduced switching energy enables 1 MHz operation. A 48–1 V prototype with 100 A output achieves 93.4% peak efficiency, validating the design's effectiveness.

The rest of this article is organized as follows. Section II introduces the circuit structure and operation principles. Section III presents the steady-state analysis and ZVS conditions. Section IV details the prototype implementation and experimental results. Finally, Section V concludes this article.

II. Circuit Structure and Operating Principles

The proposed hybrid switched-capacitor CDR topology consists of a stacked switched-capacitor network on the primary side and a CDR on the secondary side, as shown in Fig. 2. The primary structure comprises 5 active switches (S_1–S_5) and two flying capacitors (C_1, C_2). Structurally, the flying capacitors form a stacked capacitive divider. This configuration distributes

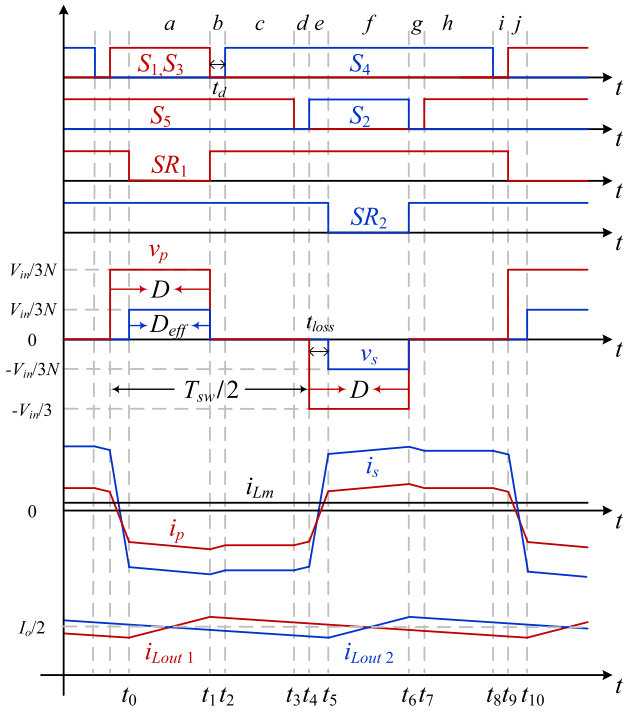


Fig. 3. Key steady-state waveforms.

the high input voltage across the capacitive stack, ensuring that the primary switches operate under reduced voltage stresses. Specifically, the voltage difference between the capacitors naturally clamps the switching nodes, limiting the switching voltage swing during commutation to a fraction of the input voltage. This feature is critical for minimizing switching losses and facilitating ZVS. Furthermore, the transformer leakage inductance L_k is utilized as a resonant element in series with the capacitive loops to achieve soft-charging of capacitors. On the secondary side, a CDR ($SR_1, SR_2, L_{out1}, L_{out2}$) is employed to double the load currents and provide ripple cancellation.

To simplify the analysis, the following assumptions are made.

1) All switches are ideal, except for their parasitic output capacitances (C_{oss}), which are assumed to be identical for the ZVS analysis.
2) The flying capacitors are sufficiently large to be treated as constant voltage sources.
3) The magnetizing inductance L_m is large enough to be neglected during the power transfer interval, whereas the leakage inductance L_k is included as the resonant element.

Based on these assumptions, the steady-state operation is examined over one switching cycle. Fig. 3 depicts the key waveforms over one switching period $T_{\rm sw}$, and the equivalent circuits are shown in Fig. 4.

a) Mode 1 [$t_0 - t_1$]: At t_0, S_1 and S_3 are turned ON. Two current loops are formed on the primary side: the input source charges C_1, while C_2 discharges to the transformer. On the secondary side, SR_2 conducts. Consequently, L_{out1} is charged by the transformer secondary voltage, while L_{out2} freewheels through SR_2. The primary voltage drives the series combination of the leakage inductance and the

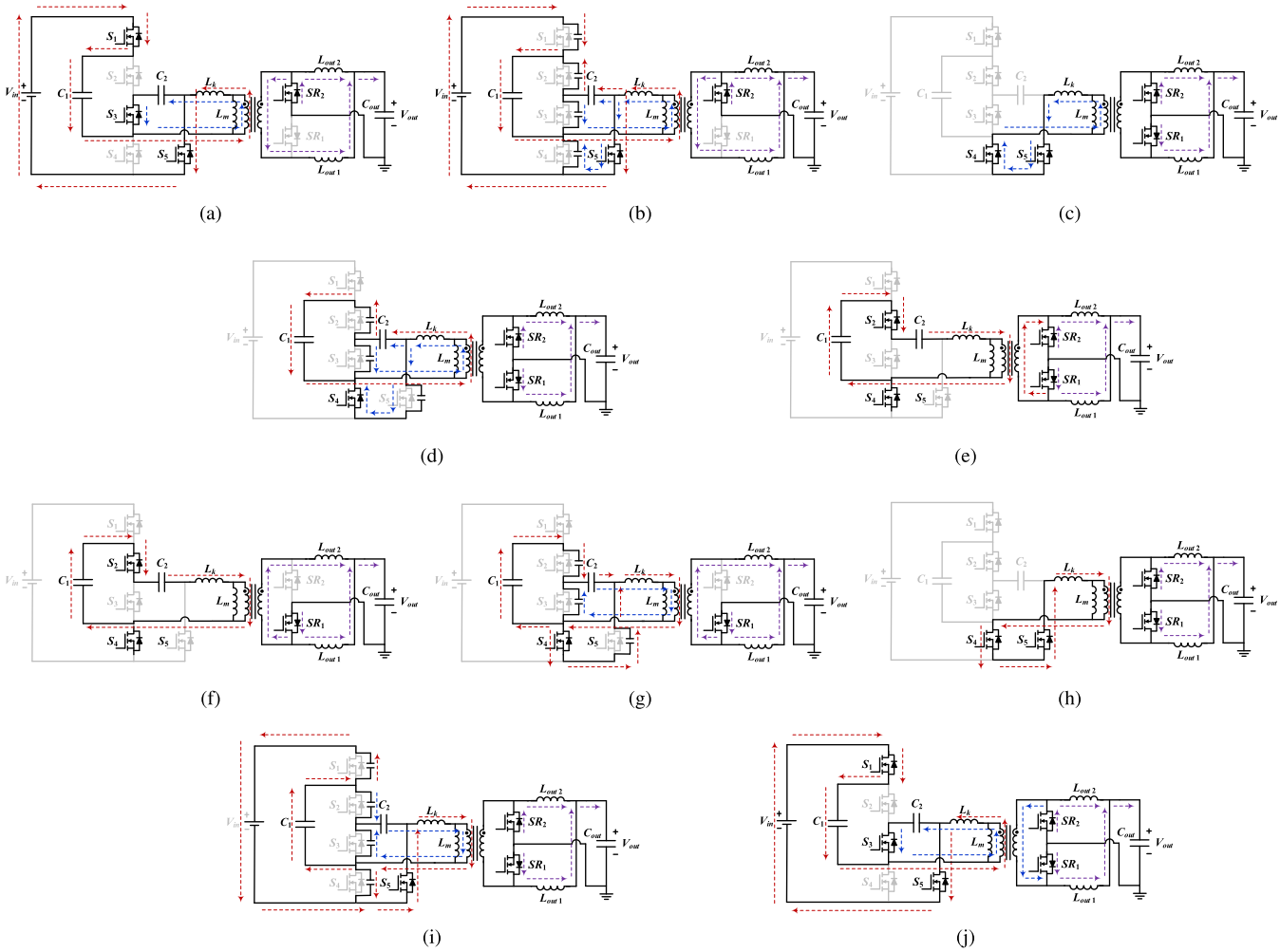


Fig. 4. Equivalent topological stages of the proposed converter over one switching cycle. (a) Mode 1 [t_0–t_1]. (b) Mode 2 [t_1–t_2]. (c) Mode 3 [t_2–t_3]. (d) Mode 4 [t_3–t_4]. (e) Mode 5 [t_4–t_5]. (f) Mode 6 [t_5–t_6]. (g) Mode 7 [t_6–t_7]. (h) Mode 8 [t_7–t_8]. (i) Mode 9 [t_8–t_9]. (j) Mode 10 [t_9–t_{10}].

reflected output inductance. The primary current i_p rises linearly, which ensures soft charging for the flying capacitors. The current is expressed as

$$i_p(t_1) = i_p(t_0) + \frac{v_p(t_0) - NV_{out}}{L_k + N^2 L_{out}}(t_1 - t_0). \quad (1)$$

b) Mode 2 [$t_1 - t_2$]: At t_1, S_1 and S_3 are turned OFF. The primary current charges the C_{oss} of S_1 and S_3, and discharges the C_{oss} of S_2 and S_4. Once the voltages across S_2 and S_4 drop to zero, their body diodes conduct to enable ZVS turn-ON. The energy required to complete this voltage commutation is

$$E_{req} = \sum_{k\in\{1,2,3,4\}} \frac{1}{2} C_{oss,k} (\Delta V_{ds,k})^2. \quad (2)$$

To ensure ZVS for S_4, the energy stored in the leakage inductance must satisfy

$$\frac{1}{2} L_k [i_p(t_1)]^2 \geq E_{req}. \quad (3)$$

c) Mode 3 [$t_2 - t_3$]: At t_2, S_4 is turned ON with ZVS. The primary current freewheels through the loop formed by S_4 and S_5. On the secondary side, both synchronous rectifiers SR_1 and SR_2 conduct, clamping the transformer voltage to zero. L_{out1} and L_{out2} freewheel through the rectifiers, releasing stored energy to the load.

d) Mode 4 [$t_3 - t_4$]: At t_3, S_5 is turned OFF. The primary current charges the C_{oss} of S_3 and S_5, and discharges the C_{oss} of S_2. Once the voltage across S_2 drops to zero, its body diode conducts. The required ZVS energy is

$$E_{req} = \sum_{k\in\{2,3,5\}} \frac{1}{2} C_{oss,k} (\Delta V_{ds,k})^2. \quad (4)$$

To achieve ZVS for S_2, the condition is

$$\frac{1}{2} L_k [i_p(t_3)]^2 \geq E_{req}. \quad (5)$$

e) Mode 5 [$t_4 - t_5$]: At t_4, S_2 is turned ON with ZVS. A primary loop is established where C_1 charges C_2. This applies a positive voltage $v_p(t_4)$ across the transformer leakage inductance L_k. On the secondary side, both synchronous rectifiers remain conducting, clamping the transformer secondary voltage to zero. Consequently, the full potential $v_p(t_4)$ is applied across L_k. The primary current

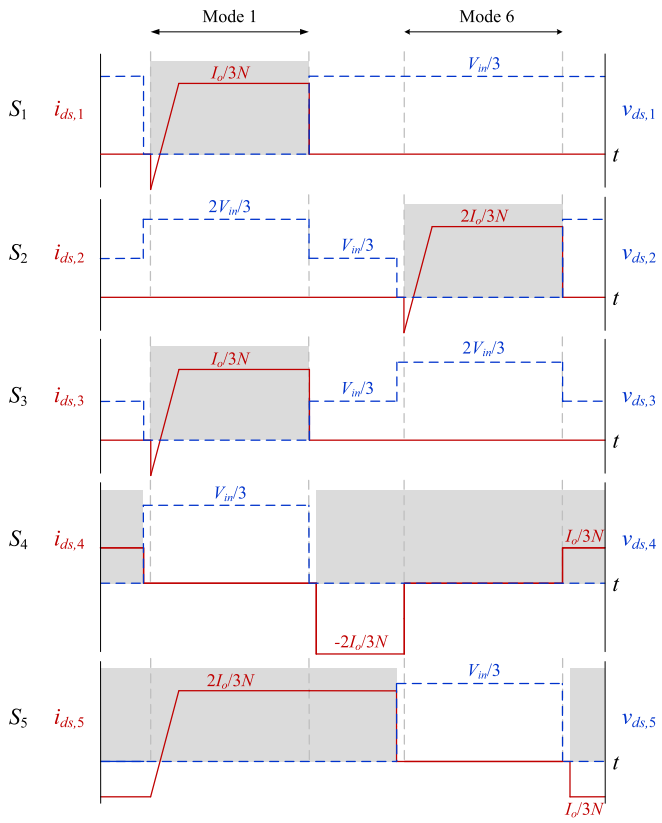


Fig. 5. Theoretical voltage (v_{ds}) and current (i_{ds}) waveforms of the primary active switches (S_1–S_5) over one switching cycle.

i_p, which is initially negative, rises linearly with a positive slope given by

$$\frac{di_p}{dt} = \frac{v_p(t_4)}{L_k}. \tag{6}$$

This commutation interval corresponds to the effective duty cycle loss time (t_{loss}). Since the secondary winding current must swing from $-I_o/2$ to $+I_o/2$ to complete the CDR commutation, the corresponding primary current variation is I_o/N. Therefore, this duty cycle loss time is strictly quantified by

$$t_{loss} = \frac{L_k \cdot I_o}{N \cdot v_p(t_4)}. \tag{7}$$

f) Mode 6 [$t_5 - t_6$]: At t_5, the primary current matches the reflected current of L_{out2}. Consequently, SR_2 turns OFF with ZCS. The transformer delivers energy to charge L_{out2}, while L_{out1} freewheels through SR_1. This interval constitutes the power-transfer phase of the positive half-cycle. The primary current i_p continues to rise linearly, driven by the voltage difference between the source and the reflected output voltage. The current at the end of this interval is expressed as

$$i_p(t_6) = i_p(t_5) + \frac{v_p(t_5) - NV_{out}}{L_k + N^2 L_{out}}(t_6 - t_5). \tag{8}$$

g) Mode 7 [$t_6 - t_7$]: At t_6, S_2 is turned OFF. The primary current charges the C_{oss} of S_2 and discharges the C_{oss} of

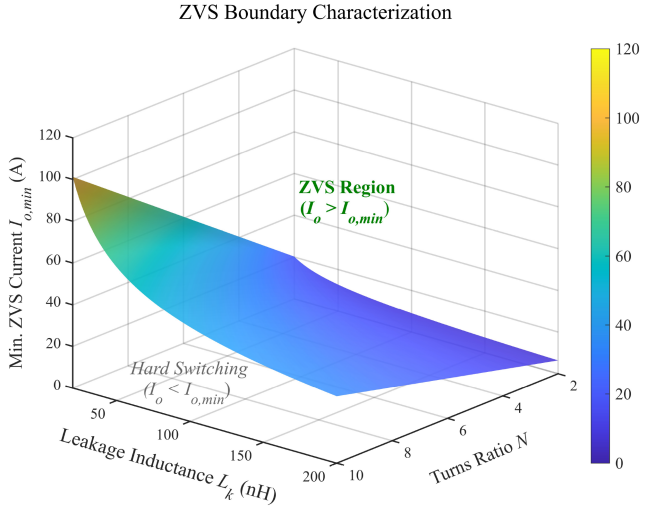


Fig. 6. ZVS boundary characterization based on turns ratio N and leakage inductance L_k. The surface indicates the minimum load current required to overcome the capacitive energy barrier.

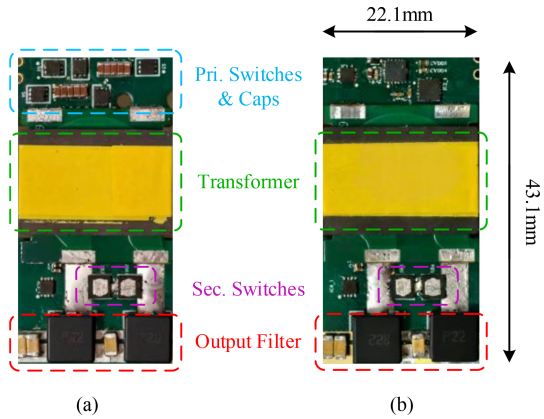


Fig. 7. Photograph of the hardware prototype. (a) Top view. (b) Bottom view.

S_3 and S_5. The ZVS condition for the incoming switches is satisfied when

$$\frac{1}{2}L_k\,[i_p(t_6)]^2 \geq \sum_{k\in\{2,3,5\}} \frac{1}{2}C_{oss,k}(\Delta V_{ds,k})^2. \tag{9}$$

h) Mode 8 [$t_7 - t_8$]: At t_7, S_5 is turned ON with ZVS. The primary current freewheels through S_4 and S_5, while both SR_1 and SR_2 conduct on the secondary side. No power is transferred from the input source during this interval.

i) Mode 9 [$t_8 - t_9$]: At t_8, S_4 is turned OFF. The primary current charges the C_{oss} of S_2 and S_4, and discharges S_1 and S_3. The leakage energy available for this transition must satisfy

$$\frac{1}{2}L_k[i_p(t_8)]^2 \geq \sum_{k\in\{1,2,3,4\}} \frac{1}{2}C_{oss,k}(\Delta V_{ds,k})^2. \tag{10}$$

j) Mode 10 [$t_9 - t_{10}$]: At t_9, S_1 and S_3 are turned ON with ZVS. $v_p(t_9)$ is applied to the leakage inductance while the secondary side remains shorted. The primary current

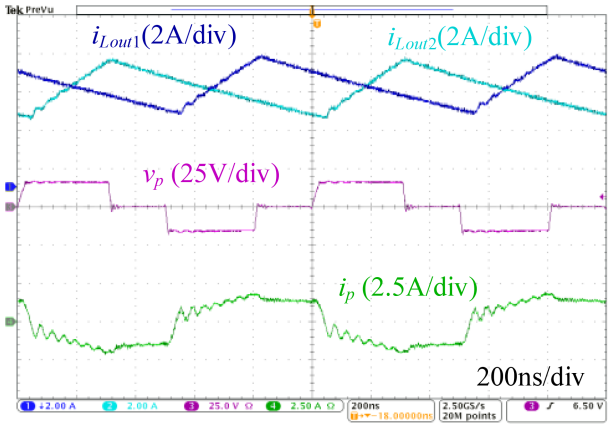


Fig. 8. Measured steady-state waveforms at $V_{in} = 48$ V and $I_o = 20$ A.

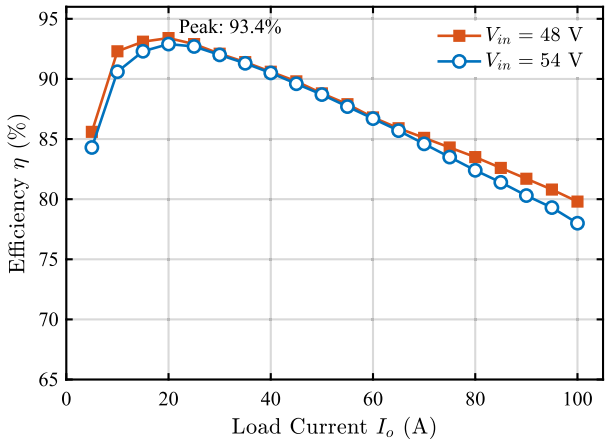


Fig. 9. Measured efficiency curves at 48 and 54 V input.

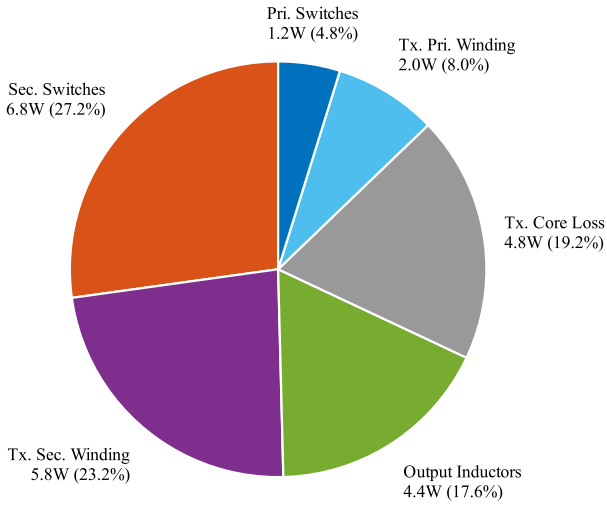


Fig. 10. Calculated power loss breakdown distribution at full load.

decreases linearly with a slope of

$$\frac{di_p}{dt} = \frac{v_p(t_9)}{L_k}. \tag{11}$$

The converter resumes to Mode 1 when the primary current matches the reflected output current.

III. Steady-State Analysis

A. Voltage Gain Derivation

To derive the voltage gain and component stresses, the steady-state operation is analyzed. Assume S_1–S_3 operate with a duty cycle D.

During the negative half-cycle (Mode 1), S_1 and S_3 conduct. The input voltage V_{in} charges C_1, while C_2 discharges through the transformer. The charging current is governed by the loop inductance (including leakage and reflected output inductance), which limits the di/dt and ensures soft-charging of the capacitors. Applying Kirchhoff's voltage law (KVL) to the primary loop yields

$$V_{C1} + V_{C2} = V_{in}. \tag{12}$$

The voltage applied to the transformer primary winding is $|v_p(t_0)| = V_{C2}$.

During the positive half-cycle (Mode 6), S_2 conducts. Capacitor C_1 charges C_2 via the transformer. Similarly, the series inductance in the conduction path enables soft-charging and prevents current spikes. The primary winding voltage is $|v_p(t_5)| = V_{C1} - V_{C2}$.

To satisfy the transformer volt-second balance under symmetric operation, the voltage magnitudes in both half-cycles must be equal

$$V_{C2} = V_{C1} - V_{C2} \Rightarrow V_{C1} = 2V_{C2}. \tag{13}$$

Solving (12) and (13) yields the capacitor voltages

$$V_{C1} = \frac{2}{3}V_{in}, \quad V_{C2} = \frac{1}{3}V_{in}. \tag{14}$$

This indicates a 3:1 voltage division, which clamps the primary-side dynamic switching-voltage swing to $V_{in}/3$.

Considering the transformer turns ratio N and the CDR characteristics, the output voltage is given by

$$V_o = \frac{V_{in}/3}{N} \times D. \tag{15}$$

Consequently, the voltage conversion ratio M is expressed as

$$M = \frac{V_o}{V_{in}} = \frac{D}{3N}. \tag{16}$$

This confirms the high step-down capability suitable for 48 V applications.

B. Current Distribution Analysis

This section analyzes the current distribution and the resulting DC bias in the magnetizing current. The variables $i_{p,pos}$ and $i_{p,neg}$ represent the effective current magnitudes during the power transfer intervals, corresponding to the average values of the instantaneous current ramps $i_p(t_6)$ and $i_p(t_1)$ analyzed in Section II.

The primary current distribution is governed by the charge balance of the flying capacitors. During the positive half-cycle (Mode 6), the current flows through the series path of C_1,

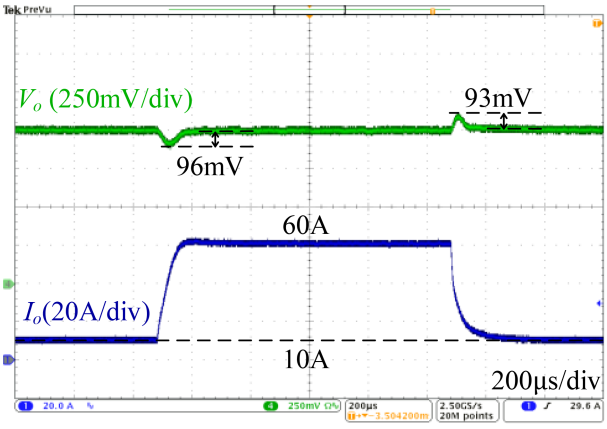


Fig. 11. Closed-loop load transient experimental waveforms.

the transformer, and C_2. Thus, the positive primary current magnitude $i_{p,pos}$ equals the discharging current of C_1 (which equals the charging current of C_2)

$$i_{p,pos} = I_{C1,dis} = I_{C2,ch}. \tag{17}$$

During the negative half-cycle (Mode 1), the input source and capacitor C_2 supply current in parallel. Consequently, the magnitude of the negative primary current $|i_{p,neg}|$ is the sum of the charging current of C_1 and the discharging current of C_2

$$|i_{p,neg}| = I_{C1,ch} + I_{C2,dis}. \tag{18}$$

At steady state, capacitor charge balance requires equal charging and discharging current ($I_{C1,ch} = I_{C1,dis}$ and $I_{C2,ch} = I_{C2,dis}$). Substituting these equalities gives the ratio of negative to positive primary currents

$$|i_{p,neg}| = 2i_{p,pos}. \tag{19}$$

This equation indicates an inherent 2:1 asymmetry in the primary current magnitude.

Conversely, the secondary CDR inherently balances the DC currents of the two output inductors due to parasitic resistance negative feedback. Consequently, the load current reflected to the primary side, denoted as i_{ref}, is symmetric. With a turns ratio of N, the reflected current magnitude is

$$i_{ref} = \frac{I_o}{2N}. \tag{20}$$

The transformer magnetizing current i_{Lm} is the difference between the total primary current i_p and the reflected load current i_{ref}. During the positive half-cycle (low current phase)

$$i_{p,pos} = i_{ref} - I_{Lm,bias}. \tag{21}$$

During the negative half-cycle (high current phase, considering magnitudes)

$$|i_{p,neg}| = i_{ref} + I_{Lm,bias}. \tag{22}$$

Since i_p is asymmetric while i_{ref} is symmetric, a DC bias $I_{Lm,bias}$ is automatically established in the magnetizing current. Solving these equations with the constraint from (19) yields the bias magnitude

$$I_{Lm,bias} = \frac{I_o}{6N} = \frac{1}{3} i_{ref}. \tag{23}$$

Substituting this bias back provides the primary currents

$$i_{p,pos} = \frac{I_o}{3N}, \quad |i_{p,neg}| = \frac{2I_o}{3N}. \tag{24}$$

It should be noted that the transformer core design must consider the DC bias $I_{Lm,bias}$ to avoid saturation.

Structurally, the series configuration of the flying capacitors and the transformer primary winding inherently establishes an auto-balancing mechanism. Suppose parasitic effects introduce a voltage deviation Δv, resulting in $V_{C1} = 2V_{in}/3 + \Delta v$ and $V_{C2} = V_{in}/3 - \Delta v$. According to the steady-state operating modes, this deviation introduces a net DC voltage across the magnetizing inductance over one switching cycle

$$\Delta V_{Lm} = D(V_{C1} - V_{C2}) - DV_{C2} = 3D\Delta v. \tag{25}$$

The resulting volt-second imbalance generates a corrective shift in the magnetizing current (ΔI_{Lm}). Since the forward and reverse primary currents inherently alternate the charging and discharging duties of C_1 and C_2, the induced ΔI_{Lm} acts to counteract the initial voltage deviation. This interaction forms an intrinsic negative feedback loop, governed by $d(\Delta v)/dt \propto -\Delta I_{Lm}$, which autonomously drives the capacitor voltages back to the nominal steady state, thereby eliminating the requirement for active control intervention.

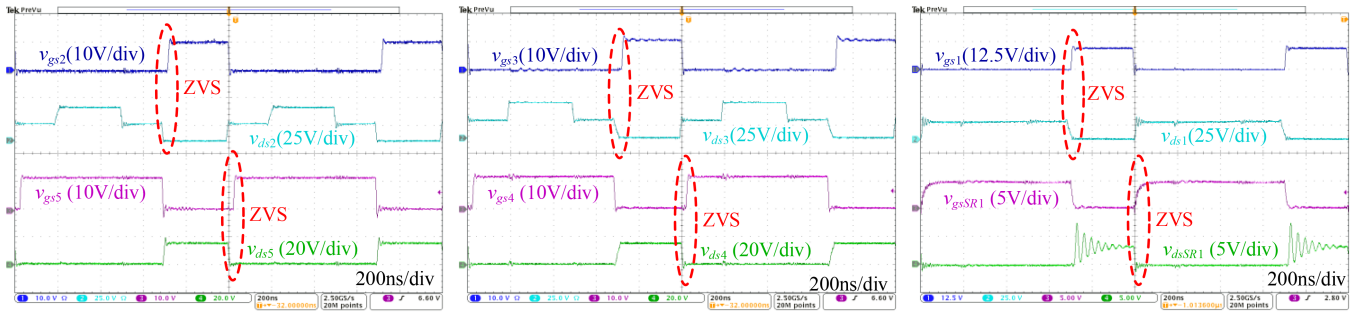
C. Voltage Stress Analysis

The voltage stresses on the active switches are determined by the steady-state capacitor voltages derived in Section III-A ($V_{C1} = 2V_{in}/3, V_{C2} = V_{in}/3$). By applying KVL to the primary loops when the switches are in the blocking state, the maximum voltage stresses are derived as

$$\begin{aligned} V_{S1,block} &= V_{in} - V_{C1} = \frac{1}{3}V_{in} \\ V_{S2,block} &= V_{in} - V_{C2} = \frac{2}{3}V_{in} \\ V_{S3,block} &= V_{C1} = \frac{2}{3}V_{in} \\ V_{S4,block} &= V_{C2} = \frac{1}{3}V_{in} \\ V_{S5,block} &= V_{C1} - V_{C2} = \frac{1}{3}V_{in}. \end{aligned} \tag{26}$$

Equation (26) reveals a nonuniform stress distribution: while S_2 and S_3 block a static voltage of $2V_{in}/3$, the dynamic switching stress for *all* active switches is strictly clamped to $V_{in}/3$. This capacitive clamping mechanism limits the voltage swing during commutation to the potential difference between adjacent flying capacitors. Consequently, the switching losses and dv/dt stress are determined by this reduced step rather than the full input voltage, enabling the use of devices with optimized FOM.

Regarding the current stress, the rms values are derived from the theoretical waveforms illustrated in Fig. 5, where the



(a) (b) (c)

Fig. 12. Zoomed-in soft-switching waveforms ($V_{in} = 48$ V, $I_o = 20$ A). (a) ZVS transitions of S_2 and S_5. (b) ZVS transitions of S_3 and S_4. (c) Waveforms of primary switch S_1 and secondary rectifier SR_1.

TABLE I
SUMMARY OF COMPONENT STRESSES

Switch	Voltage Stress	Current Stress
S_1	$\frac{1}{3}V_{in}$	$\frac{I_o}{3N}\sqrt{D-\frac{9L_kI_of_s}{8NV_{in}}}$
S_2	$\frac{2}{3}V_{in}$	$\frac{2I_o}{3N}\sqrt{D-\frac{9L_kI_of_s}{8NV_{in}}}$
S_3	$\frac{2}{3}V_{in}$	$\frac{2I_o}{3N}\sqrt{D}$
S_4	$\frac{1}{3}V_{in}$	$\frac{I_o}{3N}\sqrt{2.5-5D}$
S_5	$\frac{1}{3}V_{in}$	$\frac{I_o}{3N}\sqrt{2.5-4D-\frac{9L_kI_of_s}{8NV_{in}}}$

* *f_s denotes switching frequency. RMS currents include the impact of t_{loss}.*

shaded regions indicate the MOSFET conduction intervals. These waveforms are reconstructed based on the asymmetric current distribution analysis in Section III-B. The rms calculations summarized in Table I integrate these trapezoidal current profiles over their respective conduction intervals, accounting for the linear rise time t_{loss} during commutation.

D. ZVS Analysis

To maximize efficiency, ZVS is critical for all primary switches. The realization of ZVS relies on the energy stored in the leakage inductance L_k to discharge the C_{oss} of the switches during the dead time. Given that the primary current distribution is asymmetric, the soft-switching difficulty varies between transitions. During the transition from the negative to the positive half-cycle (Mode 4), the commutation current corresponds to the peak of the negative phase ($|i_{p,neg}| = 2I_o/3N$), providing sufficient resonant energy. In contrast, the transition from the positive to the negative half-cycle (Mode 9) relies on the significantly lower positive peak current ($i_{p,pos} = I_o/3N$). Furthermore, this transition involves the charging and discharging of four active switches (S_1, S_2, S_3, S_4). Consequently, Mode 9 represents the worst-case scenario that defines the ZVS boundary.

For this critical transition, two conditions must be satisfied simultaneously: the energy criterion and the timing criterion. Primarily, the inductive energy provided by the leakage inductance must exceed the total capacitive energy required to swing the switch voltages. The primary current available for commutation corresponds to the instantaneous current at turn-OFF, which equals the positive peak current in this mode: $I_{ZVS} = i_{p,pos} = I_o/(3N)$. Considering that the switching voltage swing is clamped to $V_{sw} = V_{in}/3$, the ZVS energy condition is expressed as

$$\frac{1}{2}L_k\left(\frac{I_o}{3N}\right)^2 \geq \sum_{k\in\{1,2,3,4\}}\frac{1}{2}C_{oss,k}\left(\frac{V_{in}}{3}\right)^2. \tag{27}$$

Solving this inequality yields the minimum load current required to overcome the capacitive energy barrier

$$I_{o,min} \geq 2NV_{in}\sqrt{\frac{C_{oss}}{L_k}}. \tag{28}$$

To visualize the design tradeoffs quantitatively, the boundary characterization based on (28) is plotted in Fig. 6. The surface represents the minimum load current threshold ($I_{o,min}$) required to achieve ZVS. The design space above the surface indicates the feasible ZVS region, whereas the area below corresponds to the hard-switching region. As illustrated, the ZVS threshold is governed by the interplay between the turns ratio N and the leakage inductance L_k. Notably, the turns ratio exerts a dominant influence on the ZVS performance. As N decreases, the surface descends rapidly, indicating that the soft-switching condition becomes significantly easier to satisfy. Likewise, increasing the leakage inductance L_k further lowers the ZVS boundary, although its impact becomes less sensitive at higher inductance values.

However, simply minimizing N and maximizing L_k to extend the ZVS range is not the optimal system-level design choice, as their selection requires navigating severe tradeoffs involving the effective duty cycle (D_{eff}), commutation duty cycle loss ($\Delta D = t_{loss} \cdot f_s$), and conduction penalties. A smaller N inherently narrows D_{eff}, which forces the secondary synchronous rectifiers to freewheel longer, thereby exacerbating secondary rms currents and primary conduction losses. Conversely, a larger N necessitates a wider D_{eff}, leaving insufficient margin for

ΔD. Furthermore, while a larger L_k expands the ZVS region toward lighter loads, it directly dictates the secondary commutation time. Under heavy-load conditions and high-frequency operation, an excessively high L_k causes ΔD to occupy a substantial fraction of the switching period, potentially saturating the available duty cycle margin. Therefore, the optimal design strategy targets the ZVS boundary at the expected peak efficiency point (e.g., 20% of the full load). To this end, we selected an intermediate turns ratio and limited leakage inductance to optimize the tradeoff between light-load soft-switching and heavy-load regulation.

Subsequently, the timing criterion imposes constraints on the dead time t_d. Even if the energy condition is met, ZVS fails if the dead time expires before the voltage transition is complete. Assuming a linear charging process, the required discharge time t_{req} is inversely proportional to the load current ($t_{req} \propto 1/I_o$). In a practical implementation with a fixed dead time, t_d must be sufficient to accommodate the discharge duration at the target minimum load

$$t_d \geq \frac{Q_{req}}{I_{ZVS}} = \frac{4C_{oss}(V_{in}/3)}{I_o/(3N)} = \frac{4NC_{oss}V_{in}}{I_o}. \quad (29)$$

Nevertheless, t_d is upper-bounded by the resonant characteristics of the leakage inductance and equivalent capacitance. To prevent current reversal within the resonant tank, t_d must not exceed one-quarter of the resonant period ($t_d \leq \frac{\pi}{2}\sqrt{L_k \cdot 4C_{oss}} = \pi\sqrt{L_k C_{oss}}$).

To benchmark the performance, the proposed converter is compared with the conventional 48 V full-bridge (FB) converter and the three-level (TL) converter. The comparative evaluation focuses on both energy demand and energy supply.

From the perspective of energy demand, the switches in a standard FB converter commutate at the full input voltage V_{in}, whereas the TL converter reduces this stress to $V_{in}/2$. By comparison, the proposed hybrid topology clamps the switching voltage swing to $V_{in}/3$. Since the parasitic capacitive energy is proportional to the square of the voltage swing, the energy barrier is minimized.

From the perspective of energy supply, the transformer turns ratio N plays a pivotal role. To maintain the same conversion ratio, the turns ratio of the proposed converter is one-third that of the FB converter ($N_{prop} = N_{FB}/3$). Consequently, the reflected load current is significantly higher. Even after accounting for the magnetizing bias, the effective commutation current remains double that of the FB benchmark.

Table II presents a comprehensive summary of these parameters. By listing the analytical expressions side-by-side, it is evident that the proposed topology simultaneously minimizes the energy demand and maximizes the energy supply.

TABLE II
COMPARISON OF ZVS PERFORMANCE

Metric	Full-Bridge	Three-Level	This Work
Total Switches	4	4	5
ZVS Commutation Switches	2	2	4
Voltage Swing	V_{in}	$1/2\,V_{in}$	$1/3\,V_{in}$
Required Energy	$C_{oss}V_{in}^2$	$1/4\,C_{oss}V_{in}^2$	$2/9\,C_{oss}V_{in}^2$
Effective Current	I_{base}	$2\,I_{base}$	$(1-1/3)\times 3\,I_{base}$
Available Energy	$1/2\,L_k I_{base}^2$	$2\,L_k I_{base}^2$	$2\,L_k I_{base}^2$

* I_{base} is the primary current of the FB converter. Required energy accounts for the total capacitance involved in the transition.

TABLE III
KEY COMPONENTS AND PARAMETERS

Component	Part Number / Specifications
Primary Switches (S_1–S_5)	ISK057N04LM6 (40 V, 5.75 mΩ)
Synch. Rectifiers (SR_1–SR_4)	IQE004NE1LM7SC (15 V, 0.45 mΩ)
Transformer Core	DMEGC DMR51W, Planar EC-core
Flying Capacitors (C_1, C_2)	2.2 μF × 5 (Murata X7R, 0603)
Output Inductors (L_{out})	220 nH (CODACA CSBX0630)
Gate Drivers	UCC27311A, UCC27614
Signal Isolation	ISO6520-Q1
Isolated Power	MIE1W0505BGLVH

IV. EXPERIMENTAL VERIFICATION

To validate the theoretical analysis and the proposed design methodology, a 1-MHz, 48–1 V prototype is designed and implemented. The converter is rated for a full load current of 100 A. To handle this high output current, the secondary side adopts a parallel structure. Two identical CDR stages are paralleled, resulting in a total of four output phases. This configuration distributes the high current stress and reduces the output voltage ripple through interleaving. The circuit is constructed on a six-layer printed circuit board (PCB) with 2-oz copper thickness to minimize conduction path resistance and optimize thermal performance.

A. Prototype Design and Implementation

The transformer design is critical for high-frequency operation. Leveraging the soft-switching capabilities, the switching frequency is set to $f_s = 1$ MHz. Accordingly, the DMEGC DMR51W ferrite material ($B_{sat} \approx 400$ mT) is selected. For the 48-V/1-V conversion, the transformer turns ratio is determined as $N = 4$. To prevent saturation under the DC magnetizing bias ($I_{Lm,bias}$) derived in Section III-B, a discrete air gap is necessary. In the prototype, four layers of 50-μm heat-resistant tape are applied to the center leg of a planar EC-core (ECW22.1A, $A_e = 43.5$ mm^2), resulting in a fixed air gap of 200 μm. This yields a magnetizing inductance of approximately 4.4 μH, ensuring operation within saturation limits while satisfying the flux swing constraint.

The key circuit components are listed in Table III. Two UCC27311A half-bridge drivers are employed to drive S_1–S_4, while a UCC27614 single-channel driver is used for S_5. To power the floating upper driver without additional isolated power supplies, a cascaded bootstrap technique is adopted. The high-side bias point (HB) of the lower driver serves as the reference potential for the upper driver, and the supply voltage (VDD) of the upper driver is charged through a bootstrap diode.

TABLE IV
PERFORMANCE COMPARISON WITH STATE-OF-THE-ART 48-V VOLTAGE REGULATORS

Reference	Solution	$V_{\text{in}}/V_o, I_o$	f_s (Voltage Regulator)	Peak Efficiency	Power Density
TIE 2020 [10]	Sigma converter	45–55 / 0.8–1.0 V, 80 A	600 kHz	94.0%	420 W/in^3
TPEL 2022 [26]	LEGOPoL	48 / 0.8–1.5 V, 450 A	286 kHz / 1 MHz	91.1%	294 W/in^3
TIE 2024 [11]	Half-bridge CDR	40–60 / 1.3–1.8 V, 120 A	600 kHz	93.1%	1037 W/in^3
TVT 2024 [13]	Series-Capacitor CDR	48–60 / 1.0 V, 30 A	500 kHz	90.6%	52 W/in^3
TPEL 2020 [15]	Stacked-bridge CDR	36–60 / 0.8–1.2 V, 45 A	500 kHz	92.7%	310 W/in^3
TPEL 2022 [18]	Quasi-resonant CDR	48 / 1.8 V, 80 A	168–282 kHz	92.1%	—
TIE 2026 [19]	Active clamp CDR	40–60 / 1.8 V, 40 A	400–600 kHz	92.6%	349 W/in^3
This work	Hybrid SC-CDR	40–60 / 1.0 V, 100 A	1 MHz	93.4%	246 W/in^3

This configuration ensures that the upper driver is powered whenever the lower switch node is clamped to a low potential. Digital isolators (ISO6520-Q1) and isolated DC–DC modules (MIE1W0505BGLVH) are employed to transmit PWM signals and provide bias power, ensuring reliable signal integrity and ground isolation between the control and power stages. Specifically, the gating signals are generated by an external Texas Instruments TMS320F280039C LaunchPad, which utilizes its enhanced PWM (ePWM) modules to digitally manage the primary stepwise ZVS dead-time intervals and compensate for SR propagation delays. A photograph of the hardware prototype is shown in Fig. 7.

B. Steady-State and Transient Performance

The steady-state performance is evaluated at the nominal 48 V input. Fig. 8 shows the key waveforms at 20-A load. The primary winding voltage v_p is effectively clamped at ± 16 V. This confirms the 3:1 capacitive division mechanism and the reduced voltage stress on the switches.

The primary current i_p exhibits a linear slope during the power transfer interval. This slope is governed by the voltage applied across the leakage inductance ($di/dt = v_p/L_k$). Based on the measured slope, the effective leakage inductance is calculated to be 96 nH. According to the energy analysis in Section III-D, this inductance value provides sufficient resonant energy to ensure ZVS for load currents exceeding 18 A. Furthermore, the output inductor currents i_{Lout1} and i_{Lout2} are highly symmetric. This validates the inherent automatic current sharing mechanism.

The measured efficiency curves are plotted in Fig. 9. The converter achieves a peak efficiency of 93.4% at 20 A. The efficiency remains at 80% at full load (100 A). High efficiency is maintained at 54-V input, demonstrating robust performance against voltage variations.

Fig. 10 shows the calculated loss breakdown at full load ($I_o = 100$ A). The total power loss is 25.0 W. Secondary-side losses dominate the distribution due to high current stress. Specifically, the synchronous rectifiers and secondary winding contribute 6.8 W (27.2%) and 5.8 W (23.2%), respectively. In contrast, the total primary-switch loss is only 1.2 W (4.8%). This confirms the effective ZVS operation of the proposed converter.

To validate the dynamic robustness and closed-loop regulation of the proposed topology, load transient experiments are conducted. For load step between 10 and 60 A, the waveforms confirm a maximum voltage undershoot of 96 mV and a peak overshoot of 93 mV, as shown in Fig. 11. By maintaining voltage deviations within 100-mV margin under significant load variations, these results verify the closed-loop transient regulation capability of the proposed converter for 48-V VRM applications.

C. ZVS Evaluation

The ZVS performance is evaluated through gate-source (v_{gs}) and drain-source (v_{ds}) waveforms. Fig. 12 details the switching transitions for critical switch pairs.

Fig. 12(a) illustrates the complementary transitions of S_2 and S_5. The drain-source voltage v_{ds} falls to zero prior to the rising edge of the gate signal v_{gs}. This timing confirms complete ZVS operation. The transitions are smooth, indicating that the leakage inductance provides sufficient resonant energy during this commutation interval.

Fig. 12(b) displays the waveforms for switches S_3 and S_4. The turn-ON of S_3 coincides with the operating phase where the magnetizing bias opposes the load current. This condition yields the minimum primary peak current and represents the worst-case scenario for soft-switching. Despite the limited commutation energy, S_3 achieves a clean ZVS transition without oscillation. This result validates that the reduced voltage swing ($V_{in}/3$) significantly lowers the energy barrier. Consequently, soft-switching is maintained even under the most critical load condition.

Fig. 12(c) presents the synchronization between the primary switch S_1 and the secondary synchronous rectifier SR_1. The waveforms confirm precise timing and effective gate drive operation. The OFF-state voltage of S_1 is clamped at approximately 16 V. This verifies the intended capacitive voltage division mechanism.

D. Performance Comparison

Table IV benchmarks the proposed design against state-of-the-art 48-V voltage regulators. While these solutions offer distinct structural merits, they encounter critical bottlenecks when

scaled to heavy-load, high-frequency applications. For instance, hybrid architectures like the Sigma converter [10] achieve high efficiency but suffer from limited control bandwidth due to their quasi-parallel LLC resonant and buck configuration. Similarly, the LEGO-PoL converter [26] attains a high step-down ratio at the cost of an excessive active switch count. Regarding CDR-based topologies, although the stacked-bridge structure [15] halves the static blocking voltage compared to standard half-bridges [11], both architectures exhibit severe leakage-induced voltage spikes under high load currents. The quasi-resonant CDR [18] effectively mitigates switching losses but is inherently restricted to low switching frequencies. Furthermore, series-capacitor and active-clamp mechanisms [13], [19] enhance soft-switching but incur excessive circulating currents and require redundant auxiliary circuitry for high-current scaling.

In contrast, the proposed hybrid converter provides a different tradeoff by combining a 3:1 capacitive step-down primary structure with a CDR output stage. As analyzed in Sections III-C and III-D and summarized in Table II, the stacked switched-capacitor primary structure redistributes the switch blocking stresses and clamps the dynamic commutation voltage swing to $V_{in}/3$. This reduced voltage swing lowers the C_{oss}-related ZVS energy requirement and enables leakage-assisted primary-side ZVS without an active-clamp or auxiliary resonant circuits. As a result, the prototype operates at 1 MHz and achieves a peak efficiency of 93.4%, as verified by the measured ZVS waveforms and efficiency results. The CDR output stage further retains buck-derived PWM regulation and interleaved high-current delivery, allowing conventional closed-loop voltage regulation and transient-enhancement techniques to be applied. In addition, the 1-MHz switching frequency allows a smaller output inductance and a shorter PWM update interval, which are beneficial for current slew-rate capability and control-bandwidth margin. Therefore, the proposed topology offers a balanced solution for 48-V/1-V VRM applications by combining reduced dynamic voltage swing, leakage-assisted ZVS, high-frequency efficiency, and practical closed-loop regulation capability.

V. Conclusion

This article proposes and demonstrates a single-stage hybrid switched-capacitor CDR voltage regulator for 48 V/1 V data center applications. By integrating a stacked capacitive divider with a CDR, the proposed topology effectively clamps the switching voltage swing to one-third of the input voltage. This mechanism significantly reduces switching losses and enables the utilization of low-voltage MOSFETs with superior FOM. Furthermore, soft-charging operation is achieved by leveraging the intrinsic transformer leakage inductance, which eliminates capacitive current spikes and facilitates ZVS without auxiliary circuits. Experimental results from a 1 MHz, 100 A prototype verify the automatic current sharing capability and robust performance, achieving 93.4% peak efficiency. These results demonstrate that the proposed solution is a viable and effective candidate for high-density power delivery in next-generation data center systems.

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Ziyao Wang (Student Member, IEEE) received the B.S. degree in electronic information engineering from ShanghaiTech University, Shanghai, China, in 2024, where he is currently working toward the Ph.D. degree in electrical engineering with the School of Information Science and Technology.

His current research interests include high-step-down switched-capacitor and point-of-load converters in data-center applications.

Zehui Li (Member, IEEE) received the bachelor's degree in electronic information engineering from Shanghai University, Shanghai, China, in 2021. She received the Ph.D. degree in electrical engineering from the School of Information Science and Technology, ShanghaiTech University, Shanghai, China, in 2026.

Her current research interests include point-of-load converter, light-load efficiency improvement, and magnetic design in data center applications.

Xufeng Kou (Senior Member, IEEE) received the B.S. degree (with honors) in optoelectronic engineering from the Department of Optical Engineering, Chu Kochen Honors College, Zhejiang University, Hangzhou, China, in 2009, and the M.S. and Ph.D. degrees in electrical engineering from the University of California at Los Angeles, Los Angeles, CA, USA, in 2012 and 2015, respectively.

He is currently a Full Professor with the School of Information Science and Technology, ShanghaiTech University, Shanghai, China. His research interests include (magnetic) topological insulators, quantum anomalous Hall effect, and related spin-orbit coupling-enabled spintronic devices.

Minfan Fu (Senior Member, IEEE) received the B.S., M.S., and Ph.D. degrees in electrical and computer engineering from the University of Michigan Shanghai Jiao Tong University Joint Institute, Shanghai Jiao Tong University, Shanghai, China, in 2010, 2013, and 2016, respectively.

From 2016 to 2018, he held a Postdoctoral position with the Center for Power Electronics Systems, Virginia Polytechnic Institute and State University, Blacksburg, VA, USA. He is currently a tenured Associate Professor with the School of Information Science and Technology, ShanghaiTech University, Shanghai. His research interests include megahertz wireless power transfer, high-frequency power conversion, high-frequency magnetic design, and the applications of wide-bandgap devices.

Haoyu Wang (Senior Member, IEEE) received the bachelor's (Distinguished Hons.) degree in electrical engineering from Zhejiang University, Hangzhou, China, in 2009, and the Ph.D. degree in electrical engineering from the University of Maryland, College Park, MD, USA, in 2014.

In 2014, he joined the School of Information Science and Technology, ShanghaiTech University, Shanghai, China, where he is currently a Full Professor with tenure. In 2023, he was a Visiting Academic Fellow with the University of Cambridge, Cambridge, U.K. His research interests include power electronics, electric vehicles, renewable energy systems, and power management integrated circuits.

Dr. Wang is an IET Fellow. He serves as an Associate Editor of IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS, IEEE TRANSACTIONS ON TRANSPORTATION ELECTRIFICATION, and *CPSS Transactions on Power Electronics and Applications*. He was the Guest Editor of *IEEE Journal of Emerging and Selected Topics in Power Electronics* and a Guest Associate Editor for IEEE TRANSACTIONS ON POWER ELECTRONICS.