Reconfigurable H5-bridge Based *LLC*-DAB Sigma Converter for EV Fast Charging Stations

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***Abstract*—In fast charging stations, the electric vehicle (EV) charger needs to adapt to the traction batteries of different models. The ultra-wide voltage range brings significant challenges to the optimal design of the dc/dc converter in the EV charger. To cope with this issue, we propose a Sigma converter based on a reconfigurable H5 bridge. The converter consists of two submodules, the *LLC* submodule and the DAB submodule, with a shared H5 bridge. By reconfiguring the H5 bridge, the *LLC* submodule exhibits a trapezoidal gain characteristic. On this basis, the DAB submodule realizes the residual gain through a hybrid modulation. The *LLC* submodule delivers the majority of power and always operates at the optimal operating point, while the voltage regulation is majorly realized by the DAB submodule. The circulating current of the *LLC* submodule contributes to the zero-voltage switching (ZVS) of the DAB, and the partial power processing structure makes the power path simpler and more efficient. In addition, the modulation method is capable of battery current control, making it suitable for EV charging applications. A 3.3kW prototype that converts 800V input to a 150-900V ultra-wide output is designed, simulated, and experimentally tested to validate the concept.**

***Keywords*—DAB, dc transformer (DCX), H5-bridge, LLC, wide voltage range**

I. Introduction

For the booming EV industries, off-board chargers play an important role in linking the traction batteries to the ac power grid. Due to the coexistence of 400V and 800V electric vehicle (EV) architectures in the current market, the dc/dc stage in the off-board EV charger needs to have an ultra-wide voltage gain range to be compatible with both voltage frameworks as shown in the system diagram in Fig. 1.

The practical application of EV charger usually adopts a two-stage architecture [1] - [5]. The frontend ac/dc stage achieves power factor correction, while the backend dc/dc stage achieves galvanic isolation and charging regulation. The dc/dc converter plays a crucial role in adapting to a wide voltage range on the battery side. DAB and resonant isolated converter are the main candidate topologies for the dc/dc stage due to their electrical isolation capability, soft switching characteristics, bi-directional power transfer capability, simple topology and mature control methods. However, they all have some limitations in terms of performance degradation in wide-gain range applications.

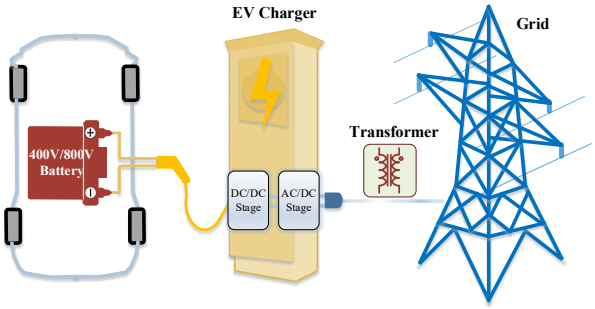


Fig. 1. The system block diagram corresponding to the application in EV charging.

The soft-switching performance of DAB is load and gain range dependent, and ZVS can only be reliably achieved at a heavy load and limited gain range. Under light load and ultra-wide gain range applications, to ensure ZVS, the inductance of DAB must be reduced, which introduces a large amount of reactive circulating current and reactive power, resulting in large circulating current losses in the circuit [6] - [10].

Resonant-isolated converters, such as *LLC* and *CLLC*, have high efficiency and a load-independent gain when the switching frequency is equal to the resonant frequency. However, when the gain of the converter is varied over a wide gain range, the efficiency of the converter will decrease rapidly. In applications with ultra-wide voltage gain ranges, a wider frequency range is required to realize wide-range voltage regulation, and then the problems of efficiency degradation and loss of soft-switching become more and more severe as the switching frequency deviates further from the resonant frequency [11] - [12].

To develop the high-performance dc/dc stage, two-stage solutions are investigated in the literature [13] - [14]. The two-stage converter implements voltage regulation and galvanic isolation separately, which can be optimized respectively. However, the overall system efficiency degrades due to the multiplication effect. To further improve the efficiency, quasi-single-stage topologies combining a DCX and a voltage regulator have been studied [15] - [16]. However, there is still some power flowing through a two-stage channel, which harms the efficiency the system's efficiency.

To achieve a true single-stage structure, this paper replaces the commonly used DCX plus PWM converter in quasi-single-stage structures with a DAB converter. Meanwhile, to further extend the gain range, an H5-bridge structure is introduced. Therefore, an *LLC*-DAB Sigma converter based on the H5 bridge is constructed. Six operating modes adapting to an ultra-wide output voltage range can be realized by changing the configurations of the H5-bridge. The *LLC* submodule always operates at the resonant frequency, which indicates good efficiency performance; the DAB submodule is regulated in a narrow voltage gain range with hybrid modulation to suppress the circulating current and extend the ZVS range. Moreover, the circulating current of the *LLC* submodule aids the DAB's primary switch in achieving ZVS under all load conditions, ameliorating the issue of ZVS loss at light load.

The rest of this paper is organized as follows. Section II introduces the proposed *LLC*-DAB Sigma converter. Section IIIdiscusses parameter design, including gain design and ZVS parameter design. Section IV demonstrated the simulation and experimental simulation verification. Finally, Section V summarizes this paper.

II. Topology Description and Operation Principles

A. Topology Description

The schematic of the proposed converter is illustrated in Fig. 2. The H5 bridge consists of five switches S_1-S_5. The H5 bridge converts the dc voltage V_A to two ac voltages, v_{ab} and v_{bc} [17]. They are fed to two impedance networks RT_1 and RT_2 with different parameters.

The H5-bridge with v_{ab}, RT_1, and the active full-bridge FB_1 forms an *LLC* submodule. The *LLC* converter always operates at the optimal operating point, with a fixed voltage gain as DCX. The H5 bridge with v_{bc}, RT_2, and the active full-bridge FB_2 forms a DAB submodule. Both the primary and secondary bridges of the DAB can operate in half-bridge mode due to the presence of the DC blocking capacitors C_P and C_S.

By configuring the H5-bridge switches among ON state, OFF state, and frequency modulation (FM) state, six configurations can be achieved, namely half bridge *LLC*, half-bridge DAB, half-bridge *LLC* plus half bridge DAB, full bridge *LLC* plus half-bridge DAB, half-bridge *LLC* plus full bridge DAB, and full-bridge *LLC* plus full-bridge DAB, as plotted in Fig. 3. By changing the configuration, the RMS values of v_{ab} and v_{bc} can be adjusted, thus the six-step voltage gain curve can be derived, expanding the entire voltage gain range.

B. DAB Modulation Method

The DAB submodule needs to handle the remaining power and regulate the voltage within a certain range, so the optimization of DAB modulation method plays a decisive role in the performance of the converter. This paper adopts a hybrid modulation method of pulse width modulation (PWM) and phase shift modulation (PFM). The v_{bc} of the DAB

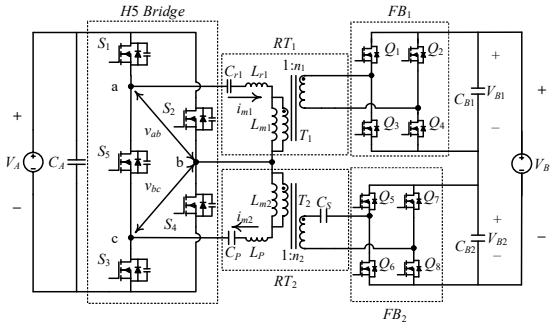


Fig. 2. Schematic of the proposed converter.

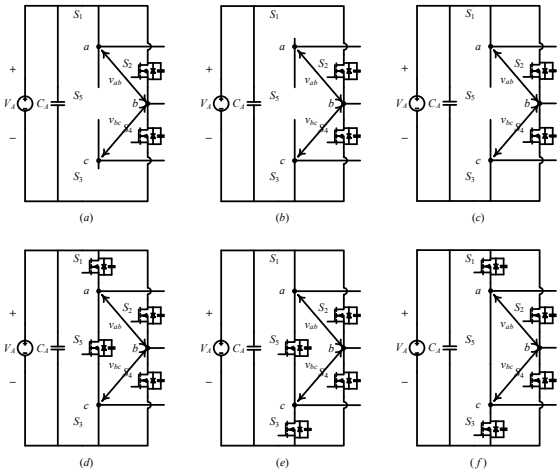


Fig. 3. Six configurations of the H5-bridge: (a) Configuration 1; (b) Configuration 2; (c) Configuration 3; (d) Configuration 4; (e) Configuration 5; (f) Configuration 6.

submodule is controlled by a complementary driving signal with a 50% duty cycle. The FB_2 operates in asymmetric pulse width modulation (APWM) to continuously adjust the dc bias of the dc blocking capacitor, so V_{B2} can be regulated. The output power is adjusted by the phase shift of the H5-bridge side and FB_2 side. Taking the operation mode of a single half-bridge DAB submodule in configuration 2 as an example, the equivalent topology is shown in Fig. 4, and the key waveforms are shown in Fig. 5.

In Fig. 5, S_2 and S_4 are driven in a complementary fashion with a 50% duty cycle, incorporating a defined dead time. The duty cycle of Q_5 and Q_7 varies by the battery side voltage. The duty cycle of Q_8 exceeds 50%. D_1 is the turning-off delay between Q_8 and Q_5. It is between 0 and 0.5.

D_1 is controlled to satisfy the following expression:

$$\frac{V_A}{2} = n_2(1-D_1)V_B \tag{1}$$

The normalized voltage gain is defined as

$$M = \frac{1}{1-D_1} = \frac{2n_2V_B}{V_A} \tag{2}$$

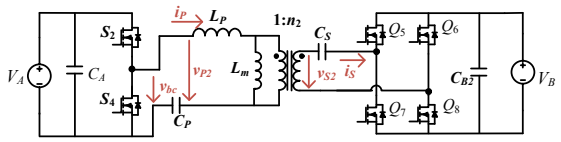


Fig. 4. Equivalent topology of configuration 2.

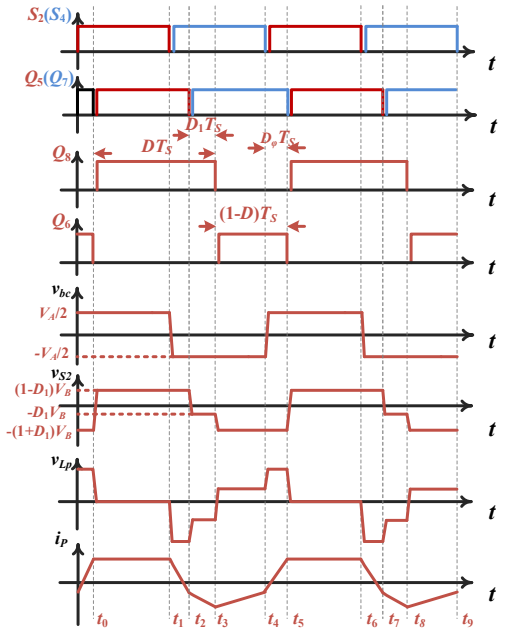


Fig. 5. Key waveform of DAB under hybrid modulation.

For $0.5 < M < 1$, the hybrid modulation realizes a general voltage match with $0 < D_1 < 0.5$. In addition, for M= 0.5 or 1, the highest and lowest gain points of the DAB submodule are completely voltage matched points, with the smallest circulating current, widest ZVS range, and optimal efficiency.

The external phase shift D_φ modulates the power transmitted. The range of D_φ is between 0 and 0.5. The output power of the half-bridge DAB submodule over a switching period is expressed as

$$P_O = \frac{V_A V_B T_S (-2D_1^2 - 4D_1 D_\varphi - 8D_\varphi^2 + 4D_\varphi + D_1)}{8 n_2 L_k} \quad (3)$$

III. Design Considerations

The two submodules of the proposed converter proposed in this paper can be decoupled into two separate parts for design, suitable for traditional DAB and *LLC* design methods. However, partial power processing techniques may pose challenges in gain design, and the ZVS enhancement effect between the two submodules and the H5-bridge configuration may result in differences in ZVS analysis. This section will focus on introducing gain analysis and ZVS analysis.

A. Gain Analysis

Partial power processing technology divides the overall gain of the converter into primary gain and residual gain. Meanwhile, the transmission power is also divided into main power and residual power. In the proposed topology, the main transmitted power is processed through the *LLC* submodule, and the DAB submodule processes the remaining power. By changing the configuration of the H5 bridge, the *LLC* resonant submodule for the main power transmission can be configured with a laddered voltage gain characteristic. The DAB submodule processes the remaining voltage gain.

TABLE I
VOLTAGE GAIN RANGE OF THE CONVERTER

Configuration	$v_{ab,\,RMS}$	$v_{bc,\,RMS}$	Minimum gain	Maximum gain
Configuration 1	$V_A/2$	0	0.5n	0.5n
Configuration 2	0	$V_A/2$	0.5n	n
Configuration 3	$V_A/2$	$V_A/2$	n	1.5n
Configuration 4	V_A	$V_A/2$	1.5n	2n
Configuration 5	$V_A/2$	V_A	1.5n	2.5n
Configuration 6	V_A	V_A	2n	3n

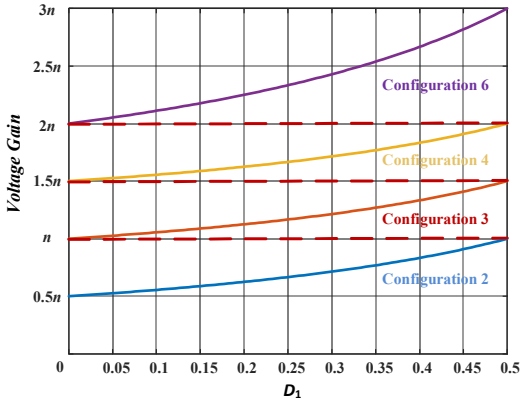


Fig. 6. Voltage gain curves of the proposed topology.

According to the DAB modulation method mentioned earlier, the range of M is between 0.5 and 1. That is $0.5 = M_{\min} \le M \le M_{\max} = 1$.

To ensure continuous gain and minimize the voltage regulation range of DAB, the voltage regulation range of DAB is set to match the voltage gain of *LLC* during gain design. That is

$$n_2 \times (M_{\max} - M_{\min}) = n_2 \times (1 - 0.5) = \frac{1}{2} \times n_1 \quad (4)$$

Therefore, it can be concluded that the transformer turns ratio of DAB and *LLC* is the same, defined as n. That is $n_1 = n_2 = n$. The voltage gain range of the converter under different configurations is shown in Table I.

The converter only operates in four configurations of 2, 3, 4, and 6 to achieve a gain range of 0.5n to 3n, as plotted in Fig. 6, and the turns ratio of two transformers can be derived from this gain range.

Taking the application of EV charging proposed in this article as an example, the output voltage range required for two voltage platforms should be able to cover 250V to 500V and 500V to 900V. So when the input voltage is 800V, n is 0.375, which means the gain range of the converter is 0.375 to 1.125, and the output voltage range is 150V to 900V.

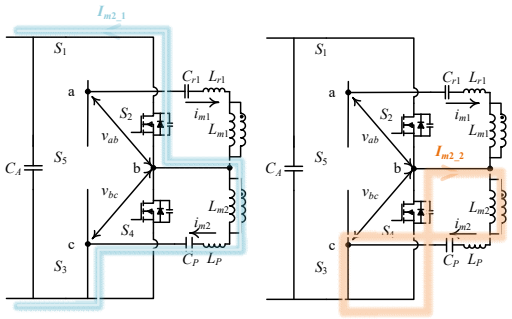


Fig. 7. The flow direction of circulating current in configuration 2 during the dead time.

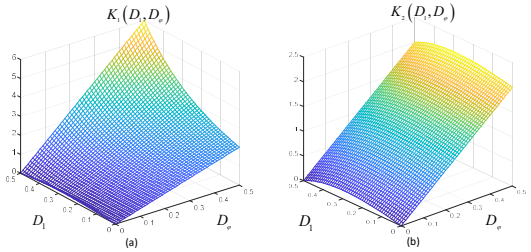


Fig. 8. The impact of D_1 and D_φ on the magnitude of circulating current.

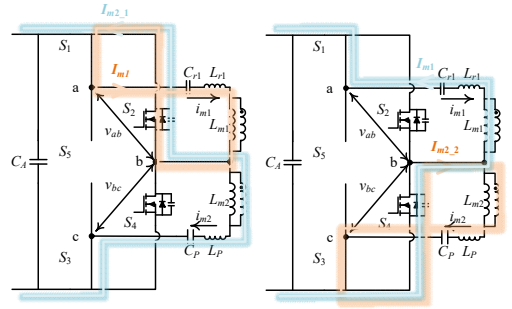


Fig. 9. The flow direction of circulating current in configuration 2 during the dead time.

B. ZVS Analysis of DAB

Based on capacitor charging balance and the waveform diagram as plotted in Fig. 5, it can be deduced that when the DAB submodule works alone, that is, configuration 2, the inductor current expression at different time points is

$$\begin{cases} i_P(t_0) = I_B\left(-2D_1^2 - 4D_1D_\varphi + 4D_\varphi + D_1\right) \\ i_P(t_1) = I_B\left(-2D_1^2 - 4D_1D_\varphi + 4D_\varphi + D_1\right) \\ i_P(t_2) = I_B\left(-2D_1^2 + 4D_1D_\varphi - 4D_\varphi + D_1\right) \\ i_P(t_3) = I_B\left(6D_1^2 + 4D_1D_\varphi - 4D_\varphi - 3D_1\right) \\ i_P(t_4) = I_B\left(-2D_1^2 - 4D_1D_\varphi - 4D_\varphi + D_1\right) \\ I_B = nV_OT_S / 4L_P \end{cases} \tag{5}$$

To simplify the analysis, C_{oss} is neglected. Therefore, when the MOSFET is turned on and the current is negative, it is considered that ZVS has been achieved. If MOSFET wants to achieve ZVS, the inductor current needs to meet the following conditions:

$$\begin{cases} Q_5,\ Q_8:\ -2D_1^2 - 4D_1D_\varphi + 4D_\varphi + D_1 > 0 \\ Q_7:\ -2D_1^2 + 4D_1D_\varphi - 4D_\varphi + D_1 < 0 \\ Q_6:\ 6D_1^2 + 4D_1D_\varphi - 4D_\varphi - 3D_1 < 0 \\ S_2:\ -2D_1^2 - 4D_1D_\varphi - 4D_\varphi + D_1 < 0 \\ S_4:\ -2D_1^2 - 4D_1D_\varphi + 4D_\varphi + D_1 > 0 \\ 0 < D_1,\ D_\varphi < 0.5,\ D_1 + D_\varphi < 0.5 \end{cases} \tag{6}$$

Considering the range of control variables, the ZVS inequalities of Q_5, Q_6, Q_8, and S_4 are always satisfied, that is Q_5, Q_6, Q_8, and S_4 can always achieve ZVS. In addition, ZVS conditions for Q_7 and S_2 can be simplified as

$$\begin{cases} S_2:\ \dfrac{1}{4}\dfrac{D_1(1-2D_1)}{1+D_1} \le D_\varphi \\ Q_7:\ \dfrac{1}{4}\dfrac{D_1(1-2D_1)}{1-D_1} \le D_\varphi \end{cases} \tag{7}$$

According to (7), when D_1 approaches 0.3, ZVS for Q_7 is the most difficult to achieve, and when D_1 approaches 0.225, ZVS for S_2 is the most difficult to achieve. When the transmission power increases, the ZVS range of Q_7 and S_2 expands. Under boundary conditions, DAB operates in single-phase shift modulation (SPS) mode, where ZVS conditions for all MOSFETs become easy to realize.

C. Design of Dead Time

In order to achieve ZVS of the primary MOSFET, the circulating current should be large enough to fully charge and discharge the output capacitor of the MOSFET during the dead zone period [18]. T_d is the duration of the dead zone. C_{oss} is an energy-normalized output capacitor.

$$I_m t_d \ge 2C_{oss}V_A \tag{8}$$

In configuration 2, DAB submodule works alone, where S_2 and S_4 form a half bridge. The circulating current when S_2 S_4 are turned on is I_{m2_1} and I_{m2_2} respectively, and their flow directions are as plotted in Fig. 7. According to (1) and (5), the value of the circulating current can be derived as follows:

$$\begin{cases} \left|I_{m2\_1}\right| = \dfrac{V_AT_S\left|2D_1^2 + 4D_1D_\varphi + 4D_\varphi - D_1\right|}{8L_P(1-D_1)} = \dfrac{V_AT_S}{8L_P} \bullet K_1(D_1, D_\varphi) \\ \left|I_{m2\_2}\right| = \dfrac{V_AT_S\left|-2D_1^2 - 4D_1D_\varphi + 4D_\varphi + D_1\right|}{8L_P(1-D_1)} = \dfrac{V_AT_S}{8L_P} \bullet K_2\left(D_1, D_\varphi\right) \end{cases} \tag{9}$$

where K_1 and K_2 are circulating current factors, whose values are related to D_1 and D_φ. The impact of D_1 and D_φ on the magnitude of circulating current is shown in Fig. 8.

According to (9), it can be concluded that

$$\begin{cases} t_{d\_on} \ge \dfrac{16C_{oss}f_sL_P}{K_1\left(D_1, D_\varphi\right)} \\ t_{d\_off} \ge \dfrac{16C_{oss}f_sL_P}{K_2\left(D_1, D_\varphi\right)} \end{cases} \tag{10}$$

When the phase shift D_φ is small, K_1 and K_2 approach 0, requiring a significant dead time to achieve ZVS. In other words, ZVS is difficult to achieve when DAB is at light load. When the phase shift D_φ is large, K_1 and K_2 are greater than 1, and the circulating current of DAB is greater than that of *LLC*. In other words, when DAB is under heavy load, it is easier to achieve ZVS compared to *LLC*.

In configuration 3, I_m of both submodules charge and discharge C_{oss} of MOSFETs, as plotted in Fig. 9.

$$(I_{m1}+I_{m2})t_d \geq 2C_{oss}V_A \tag{11}$$

The circulating current I_{m1} provided by the *LLC* submodule is expressed as follows

$$I_{m1}=\frac{V_{B1}}{4nL_{m1}f_s}=\frac{V_A}{8L_{m1}f_s} \tag{12}$$

Inserting (10), and (12) into (11), we can obtain

$$\begin{cases}\left(\dfrac{V_A}{8L_{m1}f_s}+\dfrac{V_AK_1}{8L_Pf_s}\right)t_{d\_on}\geq 2C_{oss}V_A\\ \left(\dfrac{V_A}{8L_{m1}f_s}+\dfrac{V_AK_2}{8L_Pf_s}\right)t_{d\_off}\geq 2C_{oss}V_A\end{cases} \tag{13}$$

Therefore, the ZVS conditions of the primary MOSFETs in configuration 3 can be obtained, and the following are given:

$$\begin{cases}t_{d\_on}\geq 16C_{oss}f_s\dfrac{L_{m1}L_P}{K_1L_{m1}+L_P},\ Configuration\ 3\\ t_{d\_off}\geq 16C_{oss}f_s\dfrac{L_{m1}L_P}{K_2L_{m1}+L_P},\ Configuration\ 3\end{cases} \tag{14}$$

The same analysis method is applied to several other configurations, so that the range of dead time values for configurations 4, 5, and 6 can be obtained as follows:

$$\begin{cases}t_{d\_on}\geq 16C_{oss}f_s\dfrac{L_{m1}L_P}{K_1L_{m1}+2L_P},\ Configuration\ 4\\ t_{d\_off}\geq 16C_{oss}f_s\dfrac{L_{m1}L_P}{K_1L_{m1}+2L_P},\ Configuration\ 4\\ t_{d\_on}\geq 16C_{oss}f_s\dfrac{L_{m1}L_P}{2K_1L_{m1}+L_P},\ Configuration\ 5\\ t_{d\_off}\geq 16C_{oss}f_s\dfrac{L_{m1}L_P}{2K_1L_{m1}+1L_P},\ Configuration\ 5\\ t_{d\_on}\geq 8C_{oss}f_s\dfrac{L_{m1}L_P}{K_1L_{m1}+L_P},\ Configuration\ 6\\ t_{d\_off}\geq 8C_{oss}f_s\dfrac{L_{m1}L_P}{K_1L_{m1}+L_P},\ Configuration\ 6\end{cases} \tag{15}$$

D. Design of Inductor L_P

The design of L_P is crucial in the DAB converter as it determines the power transfer capability and the power conversion efficiency. Large L_P leads to a poor power transfer capability. Therefore, L_P should be designed to meet the output power requirements with a 90% design margin as

$$L_P\leq\frac{0.9nT_sV_AV_{B2}}{2P_{rate}} \tag{20}$$

where P_{rate} is the rated power of the DAB submodule [6].

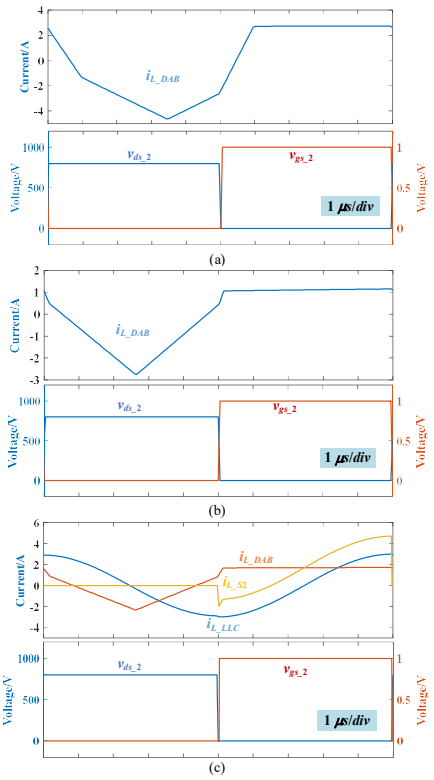


Fig. 10. Simulation result: (a) Primary current and ZVS performance of S_2 in configuration 2 with and D_φ = 0.1 and D_1 = 0.25; (b) Primary current and ZVS performance of S_2 in configuration 2 with D_φ = 0.02 and D_1 = 0.25; (c) Primary current and ZVS performance of S_2 in configuration 3 with D_φ = 0.02 and D_1 = 0.25.

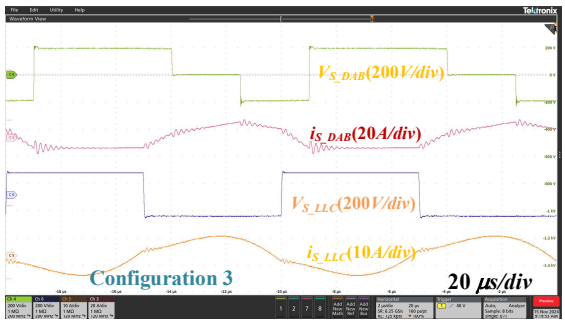
E. Design of the Blocking Capacitor C_P and C_S

Blocking capacitors are utilized to maintain dc voltage bias. Firstly, because the H5 bridge on the primary side can switch configurations, the DAB submodule has two operating modes for the primary side: half bridge and full bridge. Only when the primary side operates in a half bridge, C_P acts as the dc blocking capacitor to maintain dc voltage bias. So the rated voltage of C_P only needs to be greater than $0.25V_A$, equivalent to 200V. Meanwhile, due to the hybrid modulation method of DAB, the secondary side of DAB also has two operating modes: half bridge and full bridge. When the secondary side of DAB operates in half-bridge mode and the primary side operates in full-bridge mode, C_S experiences the maximum voltage stress of $0.5V_{B2}$, equivalent to 300V.

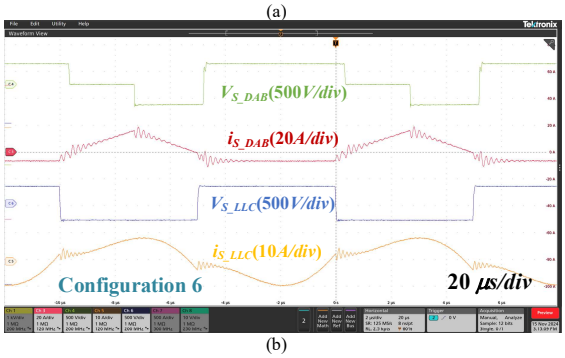
Secondly, blocking capacitors should be large enough to maintain a relatively constant voltage during charging or discharging. C_P and C_S are selected at 5μF to ensure that the voltage change rate is less than 0.01.

IV. Simulation and Experimental Results

To validate the proposed concept, a prototype of a 3.3kW converter was designed, simulated and experimentally tested. The input voltage is 800V and the output voltage is 150 - 900V. The turns n is 3/8. The leakage inductance of *LLC* is 26.6μH, the magnetic inductance is 263.17μH, and the resonant capacitance is 93nF (resonant frequency f_r = 100 kHz). The DAB inductor L_P is 200μH, and the dc blocking capacitors C_P and C_S are both 5μF.



(a)



(b)

Fig. 11. Experimental steady state waveforms: (a) Configuration 3 with V_B = 350V; (b) Configuration 6 with V_B = 700V.

Fig. 10 shows the switching process of S_2 under different working states. Fig. 10 (a) shows that in configuration 2, D_φ = 0.1 and D_1 = 0.25. At this point, meeting the ZVS condition as in (7), S_2 achieves ZVS. And Fig. 10 (b) is also the steady-state waveform under configuration 2, D_1 = 0.25. But at this point, D_φ is too small to meet the ZVS condition proposed in (7), and the circulating current is opposite to discharge direction of the C_{oss} of S_2, making it impossible for S_2 to achieve ZVS. The converter in Fig. 10 (c) operates in configuration 3. Although D_φ = 0.02 and D_1 = 0.25 are the same as (b), the circulating current is equal to the inductor current of the DAB submodule plus the magnetizing current of the *LLC* submodule, which is independent of the load. Therefore, S_2 can still achieve ZVS at this time, which is the ZVS enhancement performance between *LLC* and DAB.

Fig. 11 (a) shows the steady-state waveform of the design prototype in configuration 3 when the output voltage is 350V. Fig. 11 (b) shows the steady-state waveform of the design prototype in configuration 6 when the output voltage is 700V. Both submodules can operate normally regardless of whether the primary side is a full bridge or a half bridge. According to the waveform, it can be observed that the output voltage gains of DAB and *LLC* submodules do not interfere with each other, which is consistent with the gain analysis in the paper. And thanks to the hybrid modulation method, the peak current of the DAB submodule is greatly reduced.

V. Conclusion

This paper introduces an *LLC*-DAB Sigma converter. The topology is thoroughly described, alongside a detailed analysis of its steady-state operation. A hybrid modulation method is employed to enhance the control of the DAB submodule, which is crucial for voltage regulation. The paper derives the converter's gain range and conducts a ZVS analysis. The proposed topology and modulation technique effectively address the challenge of achieving both high efficiency and a wide voltage gain range. To validate the converter's performance and feasibility, a 3.3 kW prototype was developed with an input voltage of 800V and an adjustable output voltage ranging from 150V to 900V.

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