






# Wide Voltage Range Efficiency Enhancement Scheme for Input-Parallel-Output-Series DAB Converters in 800 V DC Microgrids

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**Abstract**—Input-parallel-output-series dual-active-bridge (DAB) converter presents an appealing approach in energy storage integrated high-voltage dc microgrids. The wide voltage range of the energy storage battery introduces significant challenges to the optimal design of the DAB converter. To cope with this issue, this article proposes a hybrid modulation scheme to enhance the wide voltage range efficiency. It combines asymmetrical pulsewidth modulation (APWM), phase-shift modulation, and coupled inductor modulation, aimed at optimizing circulating currents and extending the zero-voltage-switching (ZVS) range across wide voltage and load ranges. APWM ensures that the primary and secondary voltages are aligned through the intermediary dc blocking capacitor. Meanwhile, the coupled inductor modulation achieves an adaptive equivalent series inductance. The operational modes of this modulation scheme are outlined, with a thorough analysis of the relationship between root-mean-square (rms) current, phase shift ratio, voltage gain, and output power. Based on these insights, a control strategy is developed to extend the ZVS range with reduced rms currents. To validate the concept, a 2-kW, 100-kHz prototype is designed and tested. The prototype interfaces a 200–400 V battery port to an 800 V dc bus. Recorded efficiencies peak at 98.3% in forward mode and 98.2% in backward mode, with consistently high performance maintained across wide voltage and load ranges.

**Index Terms**—Bidirectional dc/dc converter, dual-active-bridge (DAB), input-parallel-output-series (IPOS), wide voltage range, zero-voltage-switching (ZVS).

## I. INTRODUCTION

ENERGY storage systems (ESS) are crucial components in dc microgrids, offering flexible power and energy services [1], which require high conversion efficiency. Operating at 800 V, as opposed to 400 V, significantly reduces conduction

losses, positioning the 800 V bus as a promising evolution for dc microgrids. However, the transition to a high-voltage bus introduces new challenges for power electronics converters, necessitating advanced design and control strategy to ensure optimal performance and efficiency.

To satisfy the high-power capability and the high-voltage stress of ESSs in 800 V dc microgrids, a modular structure is introduced to isolated converters to increase the overall current and voltage levels and the conversion efficiency. With multiple modules combined, switches' voltage and current stress can be reduced, compared with conventional single-module converters. [2] Thus, low-rating power semiconductor devices can be employed in high-power applications. Considering the series-parallel connection forms on both sides of the modules, there are four architectures: input-parallel-output-series (IPOS) [3], [4], input-series-output-parallel (ISOP) [5], input-series-output-series [6], input-parallel-output-parallel [7]. The parallel structure can split the current and the series structure can reduce the voltage stress of the power switches. The energy storage battery exhibits a lower voltage compared with the 800 V bus and high current under heavy load, so the IPOS structure is an ideal choice for an ESS in an 800 V microgrid [8].

Galvanically isolated dual-active-bridge (DAB) converter is commonly used as the modular converter [4], [9]. Besides, the bidirectional power flow capability and the relatively wide voltage gain range make it more suitable for battery charging and discharging scenarios [10]. The single-phase-shift (SPS) modulation is the simplest modulation scheme for DAB converters with only one control parameter. [11] The phase shift ratio between two active bridges regulates the power flow between the primary and secondary sides. When the input and output voltages are matched, the DAB converter operates at a trapezoidal inductor current waveform with minimized root-mean-square (rms) current and wide zero-voltage-switching (ZVS) range, giving rise to a high efficiency. However, in wide-range voltage scenarios, such as batteries in ESS, the ZVS feature easily gets lost at light load, and the circulating current increases [12].

To optimize the performance of a DAB converter under unmatched conditions, modulation schemes with multiple control degree-of-freedom (DoFs) and optimized topologies for active bridges have been studied. Modulations based on phase shift, such as extended-phase-shift (EPS) [13], [14], [15], [16],

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dual-phase-shift (DPS) [17], [18], and triple-phase-shift (TPS) [19], [20], have already been widely researched. These modulations introduce inner phase shifts on the primary or secondary sides to modulate the voltages. With these extra control DoFs, the rms current can be reduced [16], [18] and the ZVS range can be expanded. [15] However, these phase-shift modulations (PSMs) still encounter high rms current when the normalized voltage gain is far from the matched point, limiting the efficiency over a wide voltage range.

Besides these PSMs, other different modulations have been investigated for wide voltage range applications, in which the duty cycle of the switches is not restricted to 0.5, which provides another control freedom. In [21], dual asymmetrical pulsewidth modulation (APWM) is proposed. Two independent duty cycles help reduce the control complexity and suppress the circulating current. However, the upper switches still encounter hard-switching owing to the active-clamp-based modulation. In [22], a hybrid modulation combining APWM with PSM is introduced. With an extra dc block capacitor, the voltage match strategy is realized. By controlling the duty cycle, the voltages of two sides can always be matched on the half of a cycle, while the circulating current can be optimized and the control strategy is simple. Meanwhile, the converter has two ideal operation points at the two extreme points of the gain range, where it can operate the same as SPS with matched voltage. However, when the converter operates at the medium gain between the two extreme points, the ZVS range is still limited, which causes low efficiency. In [23], an asymmetric EPS (AEPS) plus TPS modulation is introduced to further optimize rms current and ZVS range, with three control DoFs. However, the analysis and the design of the optimization trajectory are complicated.

Apart from the optimization method for single-module DAB converters above, schemes designed for modular-structure DAB converters are also reported. In [24], an auxiliary coupled inductor connected in a paralleled full-bridge structure is introduced to extend the ZVS range. However, the coupled inductor performs as an extra component besides existing series inductors and transformers, which is essential for DAB converter, and the circuit complexity and magnetic component sizes increase. Besides, in [25], a scheme that substitutes the series independent inductors with coupled inductors connected across modules is introduced. Apart from the advantages of volume, the coupled inductor gives two different inductances under different voltage excitations over the inductor. In [26], a hybrid SPS modulation is introduced to modulate the coupled inductor and achieve optimized rms current at full load range. In [27], the converter is modulated to operate under *LLC* or DAB mode based on modulated the coupled inductor. However, these researches on modular DAB converters with coupled inductors mainly focus on dc transformer applications, where the voltage gains tend to be fixed.

In this manuscript, to achieve enhanced efficiency over a wide voltage range, we propose a hybrid modulation scheme based on the voltage match principle for the coupled-inductor-based IPOS-DAB converter for 800 V microgrids. The circulating current and the ZVS range are optimized within a designed voltage range. At the two extreme points in the voltage range, the

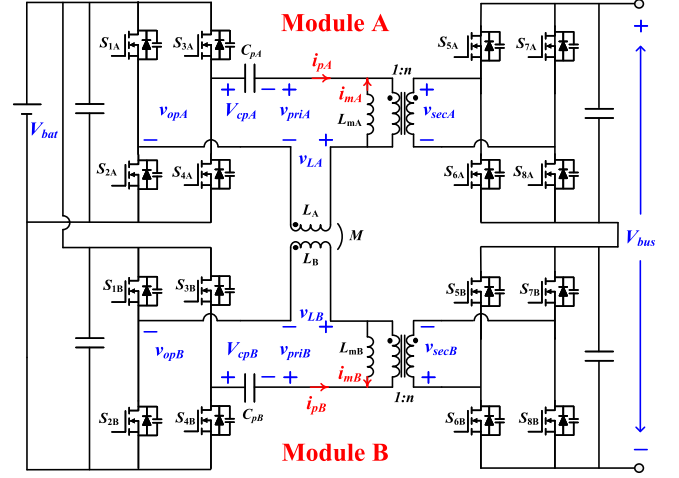


Fig. 1. Schematic of IPOS-DAB converter with coupled inductor.

converter operates with fully matched SPS modulations. With the coupled inductor, two equivalent inductances can be designed at different operating conditions to optimize heavy-load current stress and the light-load ZVS range.

The rest of this article is organized as follows. Section II introduces the working principle of the proposed hybrid modulation for the IPOS-DAB based on the coupled inductor. The detailed control strategy, including ZVS condition and modulation trajectory are analyzed in Section III. Section IV introduces the design consideration of the prototype of the converter. Section V presents the experiment results. Finally, Section VI concludes this article.

## II. OPERATION PRINCIPLES ANALYSIS

### A. Circuit Configuration

The topology of the researched IPOS-DAB converter is plotted in Fig. 1. As shown, the converter consists of two DAB modules with an IPOS structure. A battery module serves as the input, while a high-voltage dc bus is defined as the output. In each module, two full-bridge structures are placed on the primary and secondary sides, with a 1:n transformer linking both sides. A dc block capacitor is placed in series before the transformer. The series inductors of the two modules are coupled together. The parameters of the two DAB modules, including input-output capacitors, self-inductance of the coupled inductor, dc block capacitor, and power switches, are designed symmetrically to achieve power balance.

### B. Hybrid Modulation Scheme

The key steady-state waveforms of the proposed hybrid modulation scheme are plotted in Fig. 2. Basically, the modulation has two modes and the modulation of Module A is identical in both modes. The modulation of Module B is the same as Module A in Mode I, while it is complementary to Module A in Mode II. As a result, the two modes differ in modulating the voltages across the coupled inductor in each module. To simplify the analysis,

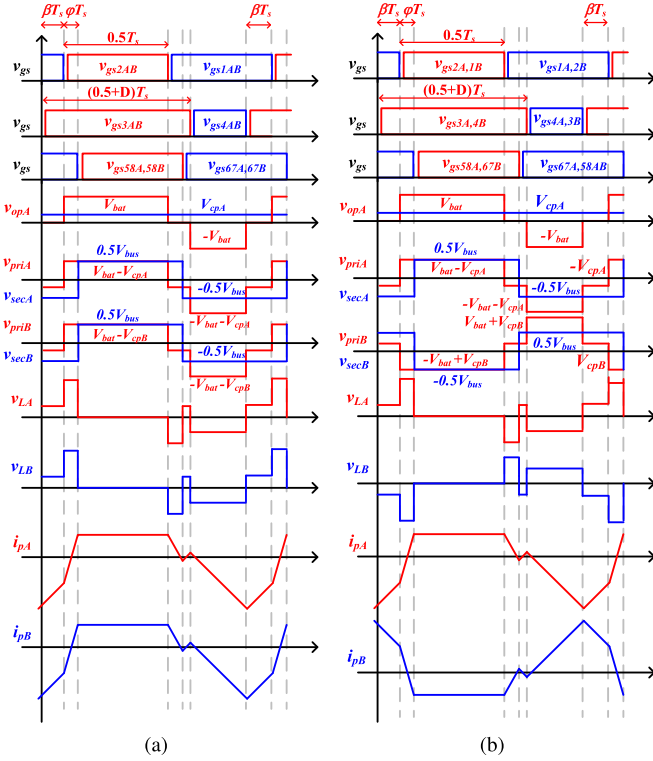


Fig. 2. Key waveforms of the proposed hybrid modulation scheme. (a) Mode I. (b) Mode II.

the modulation in Module A is detailed, and the modulation of Module B of Modes I and II can be derived easily owing to symmetry.

In the full bridge on the primary side, the two pairs of MOSFETs,  $S_{1A,2A}$  and  $S_{3A,4A}$ , are driven complementarily, respectively. The duty cycle of MOSFETs  $S_{1A,2A}$  is set at 50%, while the duty cycle of the other pair,  $S_{3A,4A}$ , is extended over 50%. The redundant duty cycle is defined as the asymmetrical duty cycle  $D$ , which varies between 0 and 0.5. Between the two pairs of MOSFETs, the phase of  $S_{3A}$  leads the phase of  $S_{2A}$  with a phase shift ratio  $\beta$ , varying between 0 and  $D$ . Thus, the output voltage of the primary full bridge,  $v_{opA}$ , consists of four intervals with three voltage levels ( $V_{bat}$ , 0, and  $-V_{bat}$ ). The  $V_{bat}$  interval occupies 0.5 of a period, while the  $-V_{bat}$  one occupies  $0.5 - D$ . The two zero-voltage intervals occupy  $D$  together. The inner phase shift  $\beta$  modulates the phase of the  $-V_{bat}$  interval separating the zero-voltage interval.

On the secondary side, the MOSFETs are driven complementarily with a 50% duty cycle. The phases of  $S_{5A}$  and  $S_{8A}$  are identical. Therefore, a 50% square waveform is generated on the transformer secondary side. Moreover, an outer phase shift ratio  $\varphi$  between the primary and secondary sides modulates the DAB module's power magnitude and direction.  $\varphi$  ranges from 0 to 0.5 and the primary side can lead or lag the secondary side.

Based on the volt-second balance of the transformer magnetizing inductor and the series inductor substituted by the coupled inductor in this design, capacitor  $C_{pA}$  blocks the dc component of  $v_{opA}$ . The dc component of  $v_{opA}$  can be derived by the mean

of the four voltage intervals

$$V_{cpA} = \frac{1}{T_s} [0.5T_s V_{bat} + (0.5 - D)T_s (-V_{bat})] = DV_{bat}. \quad (1)$$

When  $v_{opA}$  is blocked, the voltage across the inductor and transformer,  $v_{priA}$ , can be derived. Thus, the 50% positive level of  $v_{priA}$  is

$$\bar{v}_{priA, pos} = V_{bat} - V_{cpA} = (1 - D)V_{bat} = -\bar{v}_{priA, neg} \quad (2)$$

where  $\bar{v}_{priA, neg}$  is the average value of the negative level of the other 50% intervals, owing to the blocked dc component.

To realize the voltage match, the duty cycle  $D$  is modulated to match the average voltage of  $v_{priA}$  with  $v_{secA}$ , which satisfies the expressions

$$\begin{cases} \bar{v}_{priA, pos} = \bar{v}_{secA, pos} / n \\ \bar{v}_{priA, neg} = \bar{v}_{secA, neg} / n. \end{cases} \quad (3)$$

The voltage match equation is derived

$$(1 - D)V_{bat} = \frac{V_{bus}}{2n}. \quad (4)$$

The normalized voltage gain of a single DAB module is defined as

$$G^* = \frac{V_{bus}}{2nV_{bat}}. \quad (5)$$

Therefore, (4) can be expressed as

$$D = 1 - G^* \quad (6)$$

which indicates that when  $V_{bat}$  varies,  $D$  should be modulated according to  $G^*$  to meet voltage match. For the range of  $D$  is from 0 to 0.5, the general voltage match can be achieved when  $0.5 \leq G^* \leq 1$ , which is the operation gain range of the converter. The rms current and ZVS range can be optimized within the gain range.

Meanwhile, it should be mentioned that when  $D$  is set 0 or 0.5, the primary bridge operates as a full-bridge or a half-bridge with a 50% duty cycle and  $v_{pri}$  and  $v_{sec}$  completely match. The converter operates as the conventional SPS modulation.

### C. Coupled Inductor

The voltages across the coupled inductor can be expressed according to the fundamental circuit theory

$$\begin{cases} v_{LA} = L_A \frac{di_{pA}}{dt} + M \frac{di_{pB}}{dt} \\ v_{LB} = L_B \frac{di_{pB}}{dt} + M \frac{di_{pA}}{dt} \end{cases} \quad (7)$$

where  $L_A$  and  $L_B$  are the self-inductance at modules A and B, and  $M$  is the mutual inductance between the coupled windings. The equations can be rearranged as

$$\begin{cases} \frac{di_{pA}}{dt} = \frac{v_{LA} - k_c v_{LB}}{L_A(1 - k_c^2)} \\ \frac{di_{pB}}{dt} = \frac{v_{LB} - k_c v_{LA}}{L_B(1 - k_c^2)} \end{cases} \quad (8)$$

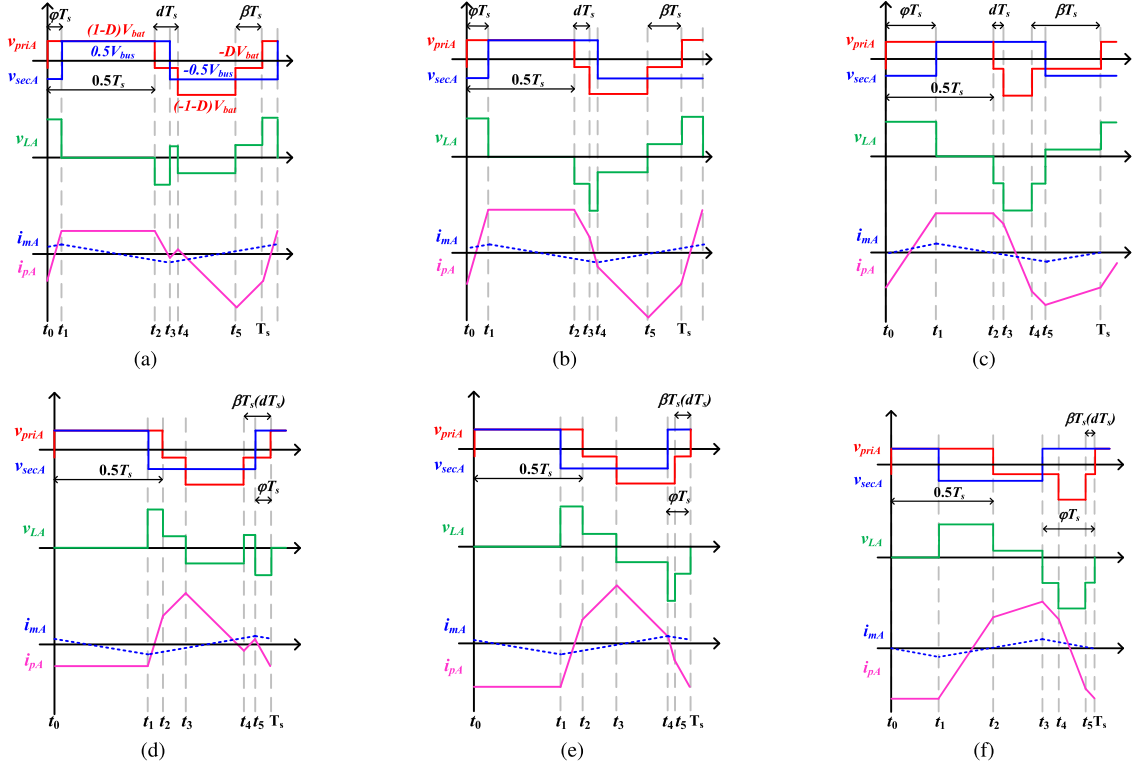


Fig. 3. Steady-state key waveforms of module A. Forward mode: (a) Mode A:  $0 \leq \varphi \leq d$ . (b) Mode B:  $d \leq \varphi \leq 0.5 - D + d$ . (c) Mode C:  $0.5 - D + d \leq \varphi \leq 0.5$ . Backward mode: (d) Mode D:  $0 \leq \varphi \leq d$ . (e) Mode E:  $d \leq \varphi \leq 0.5 - D + d$ . (f) Mode F:  $0.5 - D + d \leq \varphi \leq 0.5$ .

where  $k_c$  is the coupling coefficient, defined as  $M/\sqrt{L_A L_B}$ .

When the converter operates in Mode I, the voltages across the coupled inductor satisfy  $v_{LA} = v_{LB}$ . While  $k_c$  is smaller than 1 generally and the self-inductances  $L_A$  and  $L_B$  are designed the same

$$L_A = L_B = L_k \quad (9)$$

Equation (8) can be simplified as

$$\begin{cases} \frac{di_{pA}}{dt} = \frac{v_{LA}}{L_k(1+k_c)} \\ \frac{di_{pB}}{dt} = \frac{v_{LB}}{L_k(1+k_c)} \end{cases} \quad (10)$$

Then, it can be easily found that each DAB module has an equivalent series inductance

$$L_{eqI} = L_k(1+k_c) = L_k + M. \quad (11)$$

Similarly, when the converter operates in Mode II, where the voltages across the coupled inductor satisfy  $v_{LA} = -v_{LB}$ , (8) can be expressed as

$$\begin{cases} \frac{di_{pA}}{dt} = \frac{v_{LA}}{L_k(1-k_c)} \\ \frac{di_{pB}}{dt} = \frac{v_{LB}}{L_k(1-k_c)} \end{cases} \quad (12)$$

where another equivalent series inductance can be derived as

$$L_{eqII} = L_k(1-k_c) = L_k - M. \quad (13)$$

According to the above analysis, the coupled inductor can be modulated by the driving signals. Thus, each DAB module exhibits an adaptive equivalent series inductance between  $L_{eqI}$  and  $L_{eqII}$ , by switching the operation mode of the two modules in the IPOS-DAB converter.

#### D. Power Transfer Characteristics

As is shown in Fig. 2, the modulations of modules A and B are identical in Mode I, while the drive signals of module B are complementary to module A in Mode II. Thus, only the modulation on module A needs to be analyzed, and the modulation on module B can be derived according to the symmetrical property.

Based on the relationship of outer phase shift ratio  $\varphi$ ,  $\beta$ , and duty cycle  $D$ , six possible operating submodes for module A are plotted in Fig. 3. Fig. 3(a)–(c) shows the three modes, modulating forward power from battery to dc bus, where the primary side leads the secondary side. Fig. 3(d)–(f) shows the other three modes, modulating backward power, where the primary side lags the secondary side. In these waveforms, a variable  $d$  is defined as

$$d = \begin{cases} D - \beta, & \text{(Forward mode)} \\ \beta, & \text{(Backward mode)}. \end{cases} \quad (14)$$

Thus, the variable  $d$  is the ratio of the second interval of  $v_{priA}$  in forward mode, while it is the fourth interval of  $v_{priA}$  in backward mode, as shown in Fig. 3. The inner phase shift  $\beta$  can be represented by  $d$ .



Mode A is taken as a case study. Based on the abovementioned voltage match (VM) principle, the asymmetrical duty cycle  $D$  is always set as  $1 - G^*$ . According to the charge balance of  $C_{pA}$ , the inductor current  $i_{pA}$  at different instants is derived as

$$\begin{aligned} i_{pA}(t_0) &= I_B(D - 2d - 4\varphi + 4Dd + 4D\varphi - 2D^2) \\ i_{pA}(t_1) &= I_B(D - 2d + 4\varphi + 4Dd - 4D\varphi - 2D^2) \\ i_{pA}(t_2) &= I_B(D - 2d + 4\varphi + 4Dd - 4D\varphi - 2D^2) \\ i_{pA}(t_3) &= I_B(D - 2d + 4Dd - 4D\varphi - 2D^2) \\ i_{pA}(t_4) &= I_B(D + 2d - 4\varphi - 4Dd + 4D\varphi - 2D^2) \\ i_{pA}(t_5) &= I_B(2d - 3D - 4\varphi - 4Dd + 4D\varphi + 6D^2) \end{aligned} \quad (15)$$

where  $I_B$  is defined as

$$I_B = \frac{V_{bat}T_s}{4L_{eq}}. \quad (16)$$

$L_{eq}$  is the equivalent inductance of the coupled inductor on each DAB module.

Through the integration of the product of  $v_{secA}$  and  $i_{pA}$ , the output power of the IPOS-DAB converter can be derived

$$\begin{aligned} P_{ModeA} &= \frac{2}{nT_s} \int_0^{T_s} v_{secA}(t)i_{pA}(t)dt \\ &= P_{base}P_{ModeA}^* \end{aligned} \quad (17)$$

where  $P_{base}$  is defined as the base power

$$P_{base} = \frac{V_{bus}^2 T_s}{8n^2 L_{eq}} \quad (18)$$

and  $P_{ModeA}^*$  is the normalized power of Mode A

$$P_{ModeA}^* = \frac{D - 2d + 4\varphi + 4Dd - 4D\varphi - 2D^2 - 4\varphi^2}{1 - D}. \quad (19)$$

The analysis of Modes B–F is similar. The normalized output power expressions of the other modes are listed in (20), shown at the bottom of this page. It can be found that the backward mode is symmetrical with the forward mode in the power and the inductor currents.

### III. CONTROL STRATEGY

For the symmetrical characteristics of forward and backward modes, the analysis in this section also focuses on the forward mode of Module A.

#### A. ZVS Analysis

ZVS condition of the converter should also be analyzed separately according to the different modes. Mode A is taken as an example for analysis. The ZVS condition of Mode A can be derived as

$$\begin{cases} S_2 : i_{pA}(t_0) < -I_{min} \\ S_{5,8} : i_{pA}(t_1) + i_{mA}(t_1) > I_{min} \\ S_1 : i_{pA}(t_2) > I_{min} \\ S_{6,7} : i_{pA}(t_3) + i_{mA}(t_3) < -I_{min} \\ S_4 : i_{pA}(t_4) > I_{min} \\ S_3 : i_{pA}(t_5) < -I_{min} \end{cases} \quad (21)$$

where  $I_{min}$  is the minimum current to charge and discharge the parasitic output capacitor  $C_{oss}$  of MOSFETs on the primary and secondary sides at switching instants, respectively, which can be expressed as

$$I_{min} = \begin{cases} \sqrt{2C_{oss,p}V_{bat}^2/L_{eq}}, (S_{1234}) \\ \sqrt{C_{oss,s}V_{bus}^2/L_{eq}}, (S_{5678}). \end{cases} \quad (22)$$

The current expressions of Mode A are listed in (15), so the ZVS condition of each switch can be expressed

$$\begin{cases} S_2 : \varphi > \frac{(2d - D)(2D - 1)}{4(1 - D)} + \frac{I_{min}}{4I_B(1 - D)} \\ S_{5,8} : \varphi > \frac{(2d - D)(1 - 2D)}{4(1 - D)} + \frac{I_{min} - i_m(t_1)}{4I_B(1 - D)} \\ S_1 : \varphi > \frac{(2d - D)(1 - 2D)}{4(1 - D)} + \frac{I_{min}}{4I_B(1 - D)} \\ S_{6,7} : \varphi > \frac{(2d - D)(2D - 1)}{4(1 - D)} + \frac{I_{min} + i_m(t_3)}{4I_B D} \\ S_4 : \varphi < \frac{(2d + D)(1 - 2D)}{4(1 - D)} - \frac{I_{min}}{4I_B(1 - D)} \\ S_3 : \varphi > \frac{(2d - 3D)(1 - 2D)}{4(1 - D)} + \frac{I_{min}}{4I_B(1 - D)}. \end{cases} \quad (23)$$

ZVS conditions of the other modes can be derived using a similar method. Thus, ZVS condition can be plotted according to  $\varphi$  and  $d$  with a certain  $D$ . The ZVS condition when  $G^* = 0.667$  is plotted in Fig. 4 as an example. Fig. 4(a) shows the ideal ZVS condition when  $C_{oss}$  and the magnetizing inductance are neglected. As shown, there exist continuous full ZVS areas in the plot.

To make the analysis accurate,  $C_{oss}$  and  $L_m$  should be considered and the real ZVS condition is plotted in Fig. 4(b). The regions of each mode are labeled.

$$\begin{aligned} P_{ModeA}^* &= (D - 2d + 4\varphi + 4Dd - 4D\varphi - 2D^2 - 4\varphi^2)/(1 - D) \\ P_{ModeB}^* &= (D - 2d + 4\varphi + 4Dd - 4D\varphi + 8\varphi d - 2D^2 - 4d^2 - 8\varphi^2)/(1 - D) \\ P_{ModeC}^* &= (-3D + 2d - 4Dd + 4D\varphi + 2D^2 - 4\varphi^2 + 1)/(1 - D) \\ P_{ModeD}^* &= (D - 2d + 4\varphi + 4Dd - 4D\varphi - 2D^2 - 4\varphi^2)/(D - 1) \\ P_{ModeE}^* &= (D - 2d + 4\varphi + 4Dd - 4D\varphi + 8\varphi d - 2D^2 - 4d^2 - 8\varphi^2)/(D - 1) \\ P_{ModeF}^* &= (-3D + 2d - 4Dd + 4D\varphi + 2D^2 - 4\varphi^2 + 1)/(D - 1). \end{aligned} \quad (20)$$

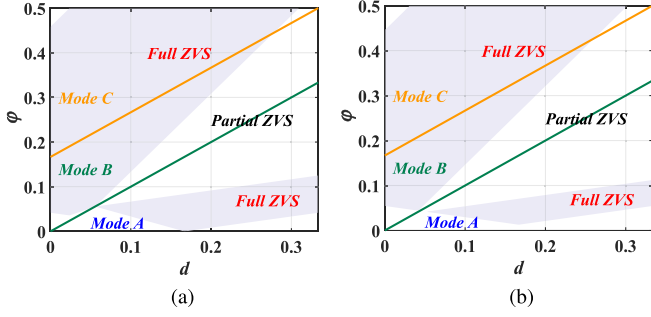


Fig. 4. ZVS condition versus  $\varphi$  and  $d$  when  $G^* = 0.667$ . (a) Ideal ZVS range. (b) ZVS range with  $C_{oss}$  and  $L_m$  considered.

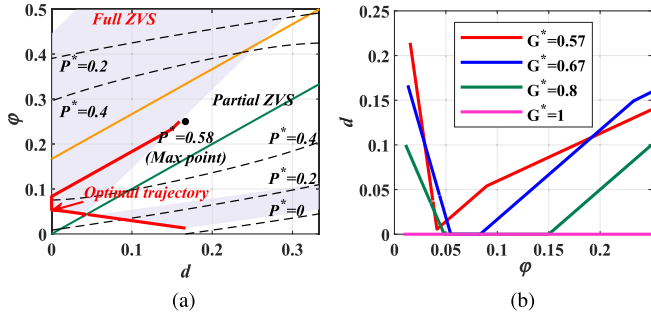


Fig. 5. Optimal modulation trajectory of  $\varphi$  and  $d$ . (a) Real ZVS range with normalized power contour lines. (b) Modulation trajectory under different gains.

### B. Modulation Trajectory

According to (20), the normalized power contour lines are plotted in Fig. 5(a) versus  $\varphi$  and  $d$ . Maximum power point is also labeled, whose coordinates can be derived by

$$\frac{\partial}{\partial d} (P_{\text{ModeB}}^*) = \frac{\partial}{\partial \varphi} (P_{\text{ModeB}}^*) = 0. \quad (24)$$

Maximum power point locates at  $(0.5D, 0.25)$ , where the maximum power can be calculated

$$P_M^* = (0.5 - D^2)/(1 - D). \quad (25)$$

In this design, the rms inductor current is also minimized. Thus, the modulation trajectory for  $d$  and  $\varphi$  should follow the minimum  $\varphi$  point of every normalized power contour line within the ZVS range. According to the ZVS range boundary and (20), when  $0 \leq D < 0.5$ , respectively,  $0.5 < G^* \leq 1$ , the modulation trajectory for  $d$  and  $\varphi$  under a certain  $D$  can be derived as

$$d(\varphi) = \max [\min (F_1, F_2), F_3, 0] \quad (26)$$

where  $F_1$  is the minimum  $\varphi$  point of contour lines in the Mode B region. It can be derived by

$$(P_{\text{modeB}}^*)'_d \Big|_{\frac{d\varphi}{dd}=0} = 0 \quad (27)$$

so

$$F_1(\varphi) = \varphi + 0.5D - 0.25 \quad (28)$$

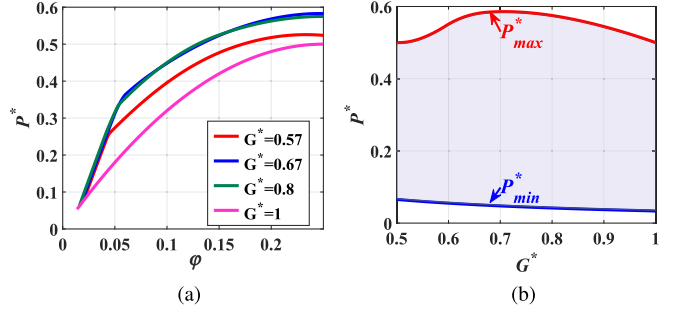


Fig. 6. Power characteristics of the designed modulation trajectory. (a) Transfer power versus  $\varphi$ . (b) Operation range versus gain  $G^*$ .

$F_2$  and  $F_3$  are derived from the boundaries of the ZVS region. They are expressed as

$$F_2(\varphi) = \frac{4(1-D)(\varphi - \Delta\varphi) - I_{\min}/I_B + D - 2D^2}{6 - 4D} \quad (29)$$

$$F_3(\varphi) = \frac{4(1-D)(\varphi - \Delta\varphi) - I_{\min}/I_B - D + 2D^2}{4D - 2} \quad (30)$$

where  $\Delta\varphi$  is a margin for the phase shift ratio  $\varphi$  relative to the ZVS boundary, which can be set smaller than 0.01 during practical design. Meanwhile, the maximum and minimum values for  $\varphi$  are

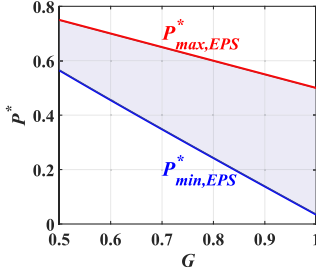
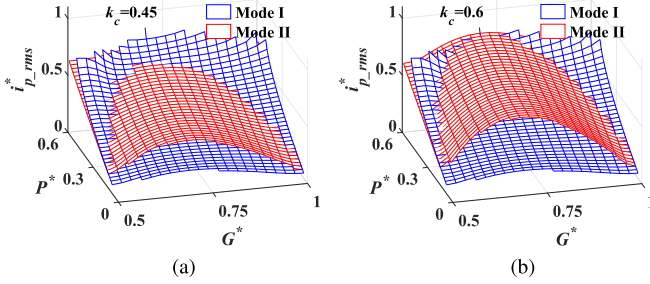
$$\begin{aligned} \varphi_{\min} &= I_{\min}/[4I_B(1-D)] + \Delta\varphi \\ \varphi_{\max} &= 0.25. \end{aligned} \quad (31)$$

Under conditions with different voltage gains, the trajectory can also be derived with the abovementioned expressions. Trajectories under conditions,  $G^* = 1$ ,  $G^* = 0.8$ , and  $G^* = 0.57$ , are shown in Fig. 5(b). When  $G^* = 0.5$ , the primary side operates in the half-bridge SPS mode with matched voltage, and the variable  $d$  does not influence the modulation. Therefore, the modulation for  $G^* = 0.5$  is similar to the condition  $G^* = 1$  whose  $d$  is always 0. The power transfer characteristics of the hybrid modulation can be derived and plotted versus  $\varphi$  under different gains in Fig. 6(a), by substituting (26) into (20). Since each line has minimum and maximum  $P^*$  values, the ZVS power range of the proposed scheme versus gain  $G^*$  is plotted in Fig. 6(b).

To validate the extended ZVS range of the proposed modulation strategy, a comparison is made with the conventional EPS method [13], which also targets soft-switching enhancement. Fig. 7 plots the ZVS load range of EPS under normalized power ( $P_{\text{base}}$ ) and gain ( $G^*$ ), including MOSFET junction capacitance ( $C_{oss}$ ) effects. Compared to Fig. 6(b), the proposed scheme achieves a wider ZVS range—notably at gains deviating for  $G^* = 1$ .

### C. Modulation Boundary of Coupled Inductor

With two inductor modulation modes, the coupled inductor leads to two gears of equivalent series inductances, which greatly influence the ZVS range and the rms inductor current. According to the operation principle of the coupled inductor introduced in

Fig. 7. Operation range versus gain  $G^*$  of EPS modulation.Fig. 8. Normalized rms inductor current of Modes I and II versus normalized power  $P^*$  with different  $G^*$  and  $k_c$  in 3-D plot. (a)  $k_c = 0.45$ . (b)  $k_c = 0.6$ .

Section II-C, the two equivalent inductances,  $L_{eqI}$  and  $L_{eqII}$ , can be designed by the self-inductance  $L_k$  and coupling coefficient  $k_c$ .

With different coupling coefficients, the rms inductor currents of the two inductor modes are plotted in Fig. 8. The rms inductor current is calculated by

$$i_{p\_rms} = \sqrt{\frac{1}{T_s} \int_0^{T_s} i_{pA}^2(t) dt} \quad (32)$$

where  $i_{pA}$  is determined by control variables ( $D$ ,  $\varphi$ , and  $d$ ).  $\varphi$  and  $d$  follow designed trajectory (26), and  $D$  satisfies (6). The base power and current of Mode I are taken for plotting the normalized current and power

$$P_{base\_I} = \frac{V_{bus}^2 T_s}{8n^2 L_{eqI}}, \quad I_{base\_I} = \frac{V_{bus} T_s}{8n L_{eqI}} \quad (33)$$

so the normalized values of Mode II should time a conversion ratio  $\alpha$  when plotting

$$\alpha = \frac{L_{eqI}}{L_{eqII}} = \frac{1 + k_c}{1 - k_c}. \quad (34)$$

It can be easily found that Mode I with larger equivalent inductance  $L_{eqI}$  takes advantage of rms current when the converter operates at middle voltage gain and achieves an extended ZVS range at light load. Meanwhile, Mode II with smaller equivalent inductance  $L_{eqII}$  has rms current advantages at heavy load when  $G^*$  is close to 0.5 or 1. Thus, the control boundary for Modes I and II according to  $P^*$  and  $G^*$  is shown in Fig. 9. The boundary between Modes I and II is plotted with a dotted line, which is solved by (20), (26), and (32). To simplify the calculation on the controller, the fitted boundary is used to approximate the

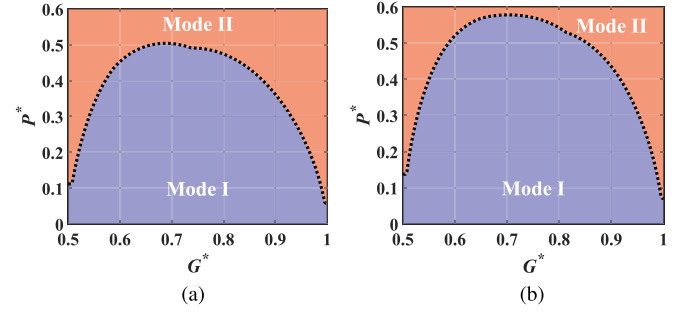
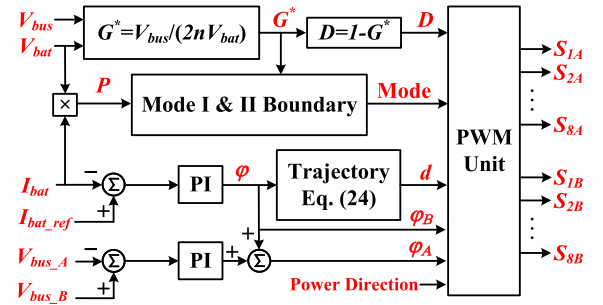
Fig. 9. Coupled inductor modulation boundary of the converter. (a)  $k_c = 0.45$ . (b)  $k_c = 0.6$ .

Fig. 10. Control diagram of the hybrid modulation.

original boundary, which will be discussed in the next section when the parameters of the coupled inductor and other necessary parameters have been determined.

To summarize the control strategy, Fig. 10 shows the basic control diagram of the hybrid modulation. As shown,  $V_{bus\_A}$  and  $V_{bus\_B}$  are the output voltages of the two DAB modules and  $I_{bat\_ref}$  is the reference current of the input battery current. Duty cycle  $D$  is obtained through voltage match principle in (6). To control the transfer power, respective to the battery current, the outer phase shift ratio  $\varphi$  is obtained by the error between  $I_{bat}$  and  $I_{bat\_ref}$  through PI controller. Besides, the error between  $V_{bus\_A}$  and  $V_{bus\_B}$  is calculated and passed through proportional integral (PI) controller to achieve voltage balance between the DAB modules. Variable  $d$  is calculated by (26) to follow the designed trajectory. Meanwhile, the operation mode, selected between Modes I and II, is determined by  $P$  and  $G^*$ .

#### IV. DESIGN CONSIDERATIONS

In this work, an IPOS-DAB prototype with parameters of 100 kHz, 2000 W,  $V_{bat} = 200\text{--}400$  V, and  $V_{bus} = 800$  V is given as a design example.

##### A. Transformer Turns Ratio

According to the previous analysis, each module of the converter operates under hybrid modulation, including APWM and PSM, and achieves an extended ZVS range and optimized rms current over a wide normalized gain range, 0.5–1. The turns ratio  $n$  of the transformer should be designed to match the real gain

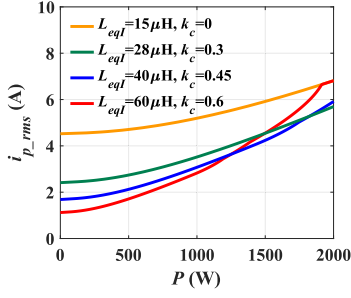


Fig. 11. RMS inductor current comparison of the converter when  $V_{bat} = 300$  V.

with the normalized operation range

$$\begin{cases} G_{min}^* = \frac{V_{bus}}{2nV_{bat\_max}} \geq 0.5 \\ G_{max}^* = \frac{V_{bus}}{2nV_{bat\_min}} \leq 1 \end{cases} \quad (35)$$

so the turns ratio  $n$  can be solved and equal to 2.

### B. Coupled Inductor

The adaptive equivalent inductance of the modulated coupled inductor further optimizes the rms current based on the hybrid modulation. Thus, the equivalent inductances of modes I and II,  $L_{eqI}$ , and  $L_{eqII}$ , (or the self-inductance  $L_k$  and coupling coefficient  $k_c$ ) should be properly designed.

For Mode II with a smaller equivalent inductance, the advantage range is wider when the gain is close to the two extreme gain points, as shown in Fig. 9. Thus,  $L_{eqII}$  should be designed to achieve optimized rms currents at  $G^* = 0.5$  or  $G^* = 1$  conditions, where the converter operates under conventional SPS modulation. Respectively, the outer phase shift ratio  $\varphi$  at rated power should be minimized. In this design, the equivalent inductance of Mode II can be calculated according to (18) and shown as

$$L_{eqII} = \frac{V_{bus}^2 T_s P_{rated}^*}{8n^2 P_{rated}} = 15 \mu\text{H} \quad (36)$$

where  $P_{rated}^*$  is the normalized power calculated by (20) when  $\varphi = 0.04$  and  $G^* = 1$  ( $D = 0$ , respectively).

For Mode I,  $L_{eqI}$  should be designed considering the rms current when  $0.5 < G^* < 1$ . The relationship between  $i_{p\_rms}$  and transfer power  $P$  with different equivalent series inductance can be derived by solving (20), (26), and (32). Fig. 11 shows the rms inductor current versus transfer power with different  $L_{eqI}$  when  $V_{bat} = 300$  V ( $G^* = 0.67$ ). As  $L_{eqI}$  increases from  $15 \mu\text{H}$ , the rms current of full load decreases at first. However, if  $L_{eqI}$  is too large, the rms current of high load begins to increase for the operation point of Mode I is close to the maximum power point. Therefore, making a compromise for rms current over the entire load, determining an optimal  $L_{eqI}$  is a tradeoff. To optimize quantitatively, a parameter  $\lambda$ , which characterizes the utilization of the circulating current in transferring active power is

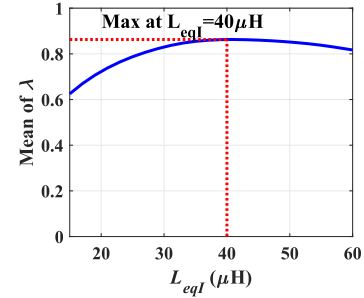


Fig. 12. Mean of  $\lambda$  versus  $L_{eqI}$  when  $V_{bat} = 300$  V.

defined as

$$\lambda = \frac{P}{\frac{V_{bus}}{n} i_{p\_rms}(P, L_{eq})}. \quad (37)$$

To characterize the current utilization within a load range, the mean of  $\lambda$  is derived as

$$\bar{\lambda} = \frac{1}{P_2 - P_1} \int_{P_1}^{P_2} \lambda(P, L_{eq}) dP. \quad (38)$$

The rms current  $i_{p\_rms}$  mainly influences the conduction loss and switching loss of the DAB converter and these losses dominate the efficiency at heavy load. Thus,  $i_{p\_rms}$  will be optimized with the load range from 1000 to 2000 W. Fig. 12 shows the  $\bar{\lambda}$  versus  $L_{eqI}$ . Numerical analysis shows that when  $L_{eqI}$  is near  $40 \mu\text{H}$ , the mean value of  $\lambda$  reaches its maximum. Respectively, the self-inductance  $L_k$  and coupling coefficient  $k_c$  of the coupled inductor can be calculated

$$\begin{aligned} L_k &= (L_{eqI} + L_{eqII})/2 = 27.5 \mu\text{H} \\ k_c &= 1 - L_{eqI}/L_k = 0.45. \end{aligned} \quad (39)$$

Fig. 13 compares rms inductor currents between the proposed hybrid scheme and EPS modulation [13], evaluating two cases. 1) *Coupled inductor*: EPS with the identical coupled inductor (current-optimized configuration). 2) *Independent inductors*: EPS with  $L = 27.5 \mu\text{H}$  (average  $L_{eqI}$  and  $L_{eqII}$ ). The proposed scheme exhibits lower rms currents across a wide voltage gain range.

### C. Magnetizing Inductance

The magnetizing currents act as injection currents to achieve the full load range ZVS for the secondary side switches. Thus, at the switching instant of the secondary switches, the magnetizing current should be larger than the minimum charging/discharging current for switches'  $C_{oss}$ , which is  $95$  pF according to the datasheet of selected switches devices

$$-i_m(t_1) = \frac{V_{bus} T_s}{8n L_m} \geq I_{min}. \quad (40)$$

The maximum  $I_{min}$  appears when the converter operates in Mode II with low equivalent inductance. Thus

$$L_m \leq \frac{T_s}{8n \sqrt{C_{oss,s}/L_{eqII}}} = 250 \mu\text{H}. \quad (41)$$



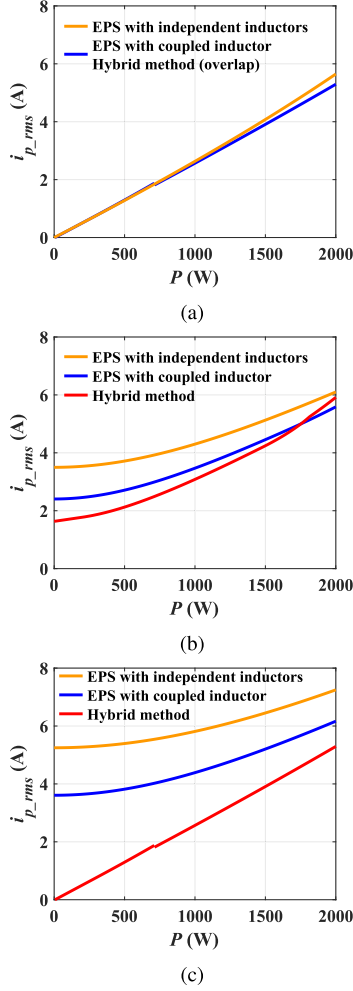


Fig. 13. RMS inductor current comparison between EPS and proposed hybrid method. (a)  $V_{bat} = 200$  V. (b)  $V_{bat} = 300$  V. (c)  $V_{bat} = 400$  V.

However, if the magnetizing inductance is too small, the rms current of the secondary-side switches rises. Thus, the magnetizing inductance is designed to be  $250 \mu\text{H}$ .

#### D. DC Blocking Capacitor

The blocking capacitors,  $C_{pA}$  and  $C_{pB}$ , hold a dc voltage bias. Its peak value is  $0.5V_{bat\_max}$ . Thus, their voltage rating should be larger than 200 V. Besides, the capacitance should be large enough to hold a relatively constant voltage when  $i_{pA}$  and  $i_{pB}$  charge or discharge them. The charge which inductor current charges and discharges in a period can be expressed approximately

$$Q_c = 0.5 \int_0^{T_s} |i_p(t)| dt \quad (42)$$

and the voltage ripple of the blocking capacitor can be expressed as

$$\Delta v = \frac{Q_c}{2C_p}. \quad (43)$$

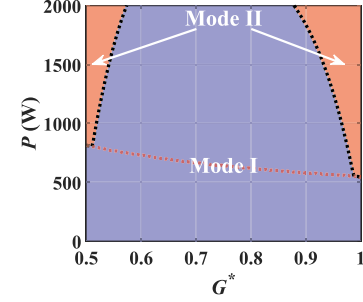


Fig. 14. Coupled inductor modulation boundary of the converter expressed with absolute power.

TABLE I  
DESIGN PARAMETERS

Component	Parameter
Primary voltage ( $V_{bat}$ )	200–400 V
Secondary voltage ( $V_{bus}$ )	800 V
Rated power	2k W
Switching frequency ( $f_s$ )	100 kHz
Blocking capacitor ( $C_{pA}$ & $C_{pB}$ )	12 $\mu\text{F}$
Turns ratio (1 : n)	16 : 32
Magnetizing inductance ( $L_{mA}$ & $L_{mB}$ )	250 $\mu\text{H}$
Self-inductance ( $L_k$ )	27.5 $\mu\text{H}$
Coupling coefficient ( $k_c$ )	0.45

$Q_c$  reaches maximum value when  $V_{bat} = 300$  V and  $P = 2\text{kW}$ , and the maximum voltage ripple occurs. In this design, to ensure that the voltage ripple is smaller than 1% of the peak voltage bias,  $C_{pA}$  and  $C_{pB}$  are designed to be 12  $\mu\text{F}$ .

#### E. Control Boundary

After determining the parameters of the coupled inductor, transformers, and switches, the boundary between modes I and II can be derived and shown in Fig. 14. The fitted expression of the black dotted line is

$$P = (-37.78G^{*4} + 115.67G^{*3} - 133.69G^{*2} + 68.94G^* - 13.10) \times 10^4. \quad (44)$$

Besides, Mode II exhibits a minimum boundary to satisfy ZVS according to the analysis in Section III-B, shown as the red dotted line in the figure. The operation points below this boundary should operate in Mode I. It can be derived by the  $\varphi_{min}$  in (31) and (20), where the margin  $\Delta\varphi$  is set 0.005 in this design.

#### V. EXPERIMENTAL RESULTS

To verify the effectiveness of the proposed modulation scheme, a 2-kW prototype of the IPOS-DAB converter with a coupled inductor is built. Fig. 15 shows the picture of the prototype. The key parameters of the prototype are listed in Table I. MOSFETs of 650V-rated silicon carbide (SiC) are selected for switches and X7R multilayer ceramic capacitors are selected for the blocking capacitors. It should be noted that the leakage inductances of the two transformers are minimized when building them.

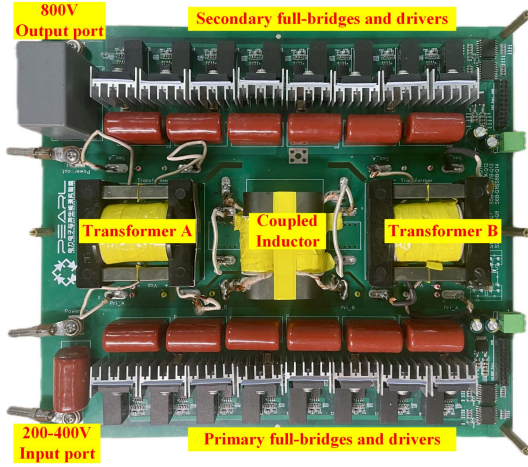
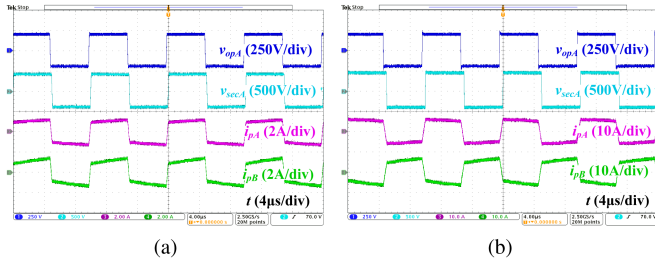
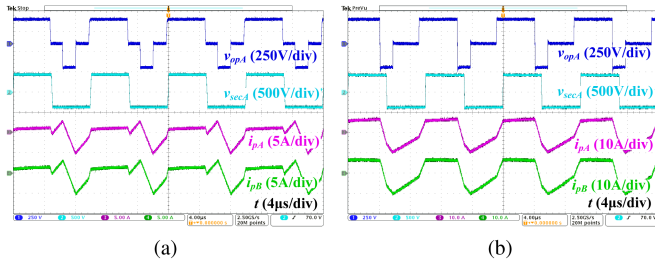
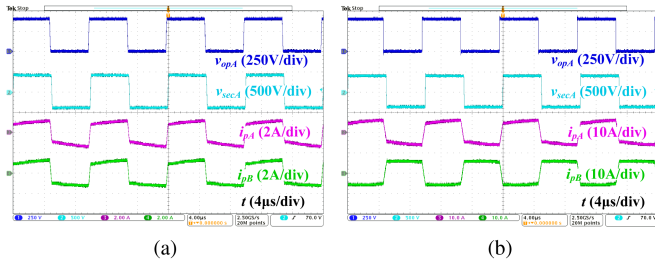
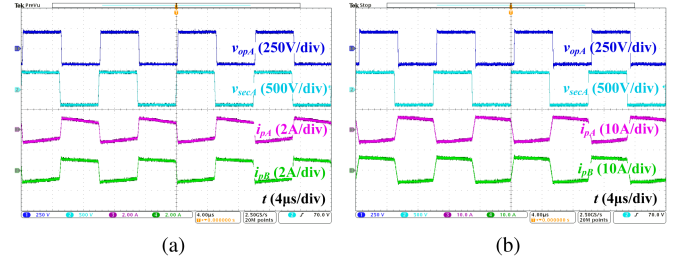
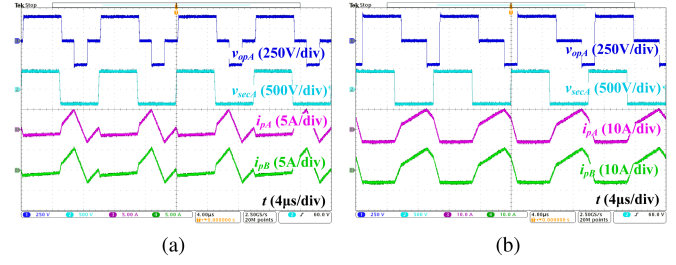
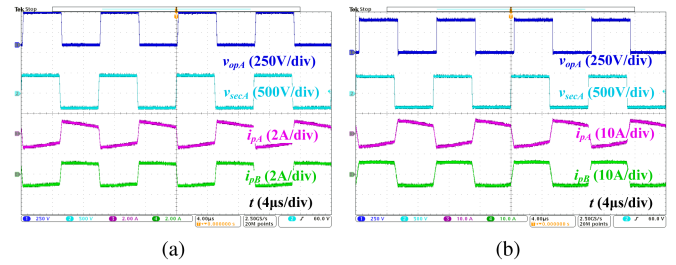


Fig. 15. Prototype of designed IPOS-DAB converter with coupled inductor.

Fig. 16. Experimental waveforms when  $V_{bat} = 200$  V with forward power. (a) Light load ( $P = 400$  W). (b) Heavy load ( $P = 2$  kW).Fig. 17. Experimental waveforms when  $V_{bat} = 300$  V with forward power. (a) Light load ( $P = 400$  W). (b) Heavy load ( $P = 2$  kW).Fig. 18. Experimental waveforms when  $V_{bat} = 400$  V with forward power. (a) Light load ( $P = 400$  W). (b) Heavy load ( $P = 2$  kW).Fig. 19. Experimental waveforms when  $V_{bat} = 200$  V with backward power. (a) Light load ( $P = 400$  W). (b) Heavy load ( $P = 2$  kW).Fig. 20. Experimental waveforms when  $V_{bat} = 300$  V with backward power. (a) Light load ( $P = 400$  W). (b) Heavy load ( $P = 2$  kW).Fig. 21. Experimental waveforms when  $V_{bat} = 400$  V with backward power. (a) Light load ( $P = 400$  W). (b) Heavy load ( $P = 2$  kW).

Figs. 16–18 show the steady-state waveforms when the converter operates in forward mode with different input voltage  $V_{bat}$ . Figs. 16 and 18 show that the primary and secondary sides' voltages completely match and the modulation is identical to SPS with trapezoidal current waveforms when the input voltage is 200 V or 400 V. The converter operates in Mode I at light load ( $P = 400$  W) with paralleled inductor current waveforms,  $i_{pA}$  and  $i_{pB}$ , and in Mode II at heavy load ( $P = 2$  kW) with contrary inductor current waveforms, matching the mode boundary, as shown in Fig. 14. The normalized gains  $G^*$  of the two conditions are 1 and 0.5, respectively. Fig. 17 shows that when the input voltage is 300 V and the primary and secondary sides' voltages do not completely match, the converter operates in Mode I within the full load range and matches the mode boundary. The light-load waveforms in Fig. 17(a) match the Mode A, as shown in Fig. 3(a), while the heavy-load waveforms in Fig. 17(b) match the Mode B, as shown in Fig. 3(b), for the modulation trajectory in Section III-B is taken.

Besides, Figs. 19–21 plot the steady-state waveforms when the converter operates in backward mode. Figs. 19 and 21 show

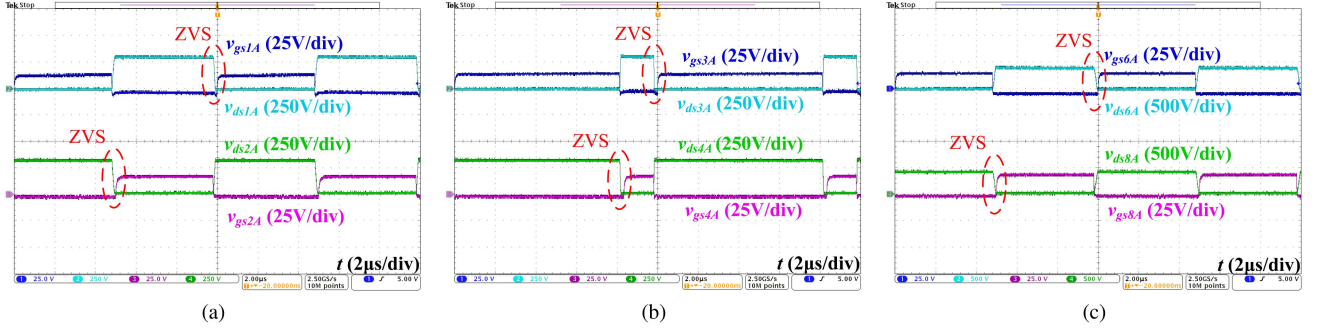


Fig. 22. ZVS waveforms when  $V_{bat} = 300$  V at light load (400 W). (a)  $S_{1A,2A}$ . (b)  $S_{3A,4A}$ . (c)  $S_{7A,8A}$ .

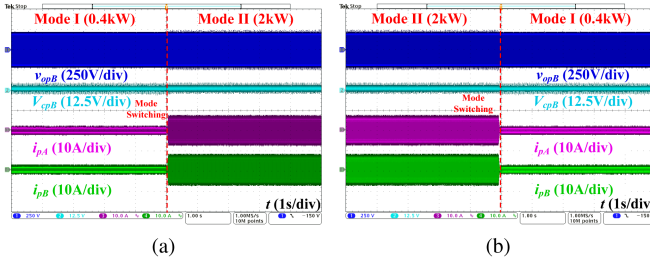


Fig. 23. Mode switching waveforms when  $V_{bat} = 200$  V. (a) Mode I to II. (b) Mode II to I.

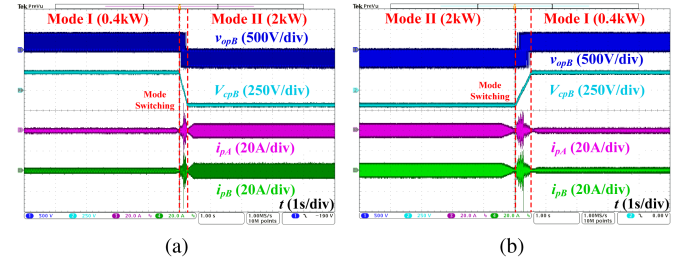


Fig. 24. Mode switching waveforms when  $V_{bat} = 400$  V. (a) Mode I to II. (b) Mode II to I.

that when the input voltage is 200 V or 400 V the converter also operates as an SPS modulation. Mode I is taken at light load and Mode II is taken at heavy load. Fig. 20 shows that when the input voltage is 300 V the converter operates in Mode I within the full load range and matches the mode boundary in Fig. 14. Light-load waveforms in Fig. 20(a) match Mode D in Fig. 3(d) and heavy-load waveforms in Fig. 20(b) match Mode E in Fig. 3(e), for the modulation of backward power is symmetrical to the forward modulation.

The ZVS waveforms of module A are plotted in Fig. 22, when  $V_{bat} = 300$  V and  $P = 400$  W. An apparent gap exists between every rising edge of  $v_{gs}$  and the corresponding falling edge of  $v_{ds}$ . Fig. 22(a) and (b) shows that all MOSFETs on the primary side achieve ZVS. Fig. 22(c) shows that the low-side MOSFETs on the secondary side also achieve ZVS, which dedicates the secondary side achieves ZVS. Owing to the symmetric modulation on module B, the ZVS characteristic of module B is identical to module A. The converter is proven to achieve ZVS soft-switching when the primary and secondary sides' voltages do not completely match. Thus, the light-load ZVS of the converter can be achieved over the wide voltage range.

Load switching waveforms for  $V_{bat} = 200$  V–400 V are shown in Figs. 23–25. Mode transitions between I/II occurs at  $V_{bat} = 200$  V and  $V_{bat} = 400$  V per the boundary control in Fig. 14, while the converter remains in Mode I at 300 V. Key observations include: 1) No significant voltage spikes occur during mode transitions; 2) Smooth current transitions at 200 V and 300 V operation; and 3) Elevated currents at 400 V due to dc-block capacitor charge/discharge dynamics and voltage mismatch.

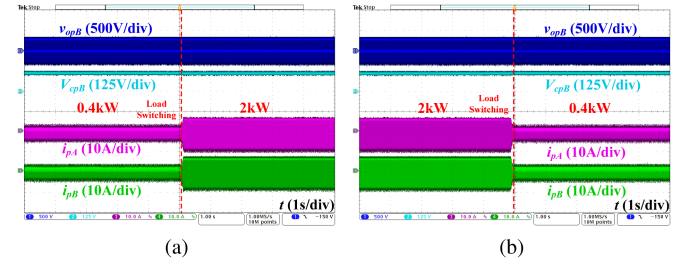


Fig. 25. Load switching waveforms when  $V_{bat} = 300$  V. (a) Light load to heavy load. (b) Heavy load to light load.

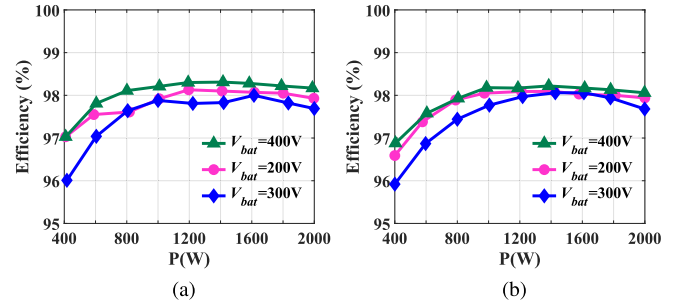


Fig. 26. Measured efficiency versus transfer power under different  $V_{bat}$ . (a) Forward mode. (b) Backward mode.

Fig. 26 shows the efficiency curves for different input voltages in forward and backward modes. The converter's loss breakdown under various loads and battery voltages is analyzed and plotted in Fig. 27. Here,  $P_{T\_cop}$  and  $P_{L\_cop}$  denote the copper losses of

TABLE II  
COMPARISONS OF EXISTING WORKS

Converter	Additional hardware per module	Modulation	rms current	ZVS range	Input/Output voltage	Power level	Efficiency
DAB [13]	None	EPS (Simple)	Reduced (SPS compared)	Medium	600V/300-600V	10kW	79-92%
DAB [16]	One capacitor	EPS (Simple)	Reduced (SPS compared)	Wide	200V/100-400V	1kW	92-98.1%
DAB [22]	One capacitor	APWM+SPS (Simple)	Reduced (EPS compared)	Narrow	100-200V/300V	500W	91-97.9%
DAB [23]	One capacitor	AEPS+TPS (Complex)	Reduced (TPS compared)	Wide	380-420V/40-56V	5kW	93.7-97.7%
DAB with VI (variable inductor) [28]	Auxiliary winding with current bias	SPS (Simple)	Reduced (SPS compared)	Wide	100V/50-100V	400W	88-92%
ISOP DAB with coupled inductor [26]	None	Hybrid SPS (Simple)	Reduced (SPS compared)	Wide	800V/380-420V	2kW	91.5-97%
This work	One capacitor	APWM+PSM (Medium)	Reduced (EPS compared)	Wide	200-400V/800V	2kW	96-98.3%

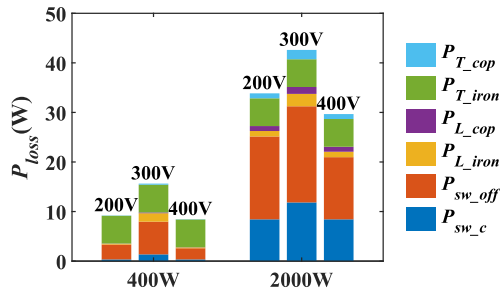


Fig. 27. Loss breakdown under different loads with different  $V_{bat}$ .

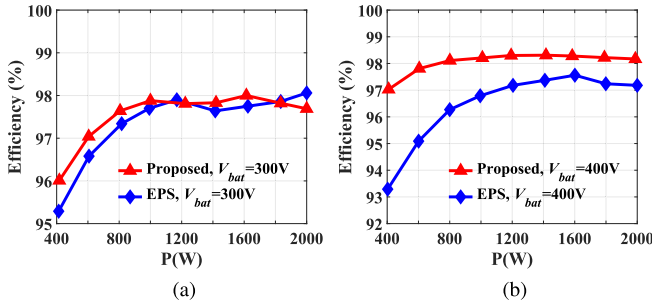


Fig. 28. Efficiency comparison between EPS modulation and proposed hybrid modulation scheme in forward mode. (a)  $V_{bat} = 300$  V. (b)  $V_{bat} = 400$  V.

the transformers and the coupled inductor, respectively, while  $P_{T_{iron}}$  and  $P_{L_{iron}}$  represent the iron losses.  $P_{sw_c}$  is the switch conduction loss and  $P_{sw_off}$  is the turn-OFF loss. The turn-ON loss is negligible due to ZVS soft-switching. At light load, magnetic losses dominate, whereas switch losses prevail at heavy load. For  $V_{bat} = 200$  V and  $V_{bat} = 400$  V, the converter operates in SPS modulation with matched voltages, yielding lower conduction and turn-OFF losses, as well as higher efficiency than the  $V_{bat} = 300$  V case due to reduced current stress. In addition, the  $V_{bat} = 400$  V condition exhibits lower turn-OFF loss than  $V_{bat} = 200$  V, enhancing the efficiency, since half of the primary-side MOSFETs remain either ON or OFF. The peak efficiency is 98.3% in forward mode and 98.2% in backward mode. Although efficiency drops slightly for  $V_{bat} = 300$  V, the

additional switch losses are marginal, and efficiency remains high ( $> 96.0\%$ ).

Fig. 28 compares efficiencies of the proposed hybrid modulation and EPS at  $V_{bat} = 300$  V and 400 V. At  $V_{bat} = 200$  V, both schemes operate identically in SPS mode, yielding matched efficiencies. Results demonstrate superior performance of the proposed method across the tested load range, particularly at  $V_{bat} = 400$  V.

Comparisons between the proposed hybrid modulation scheme and existing methods are presented in Table II. The proposed hybrid scheme offers a wide voltage gain, extends the ZVS range, and reduces the rms current across the entire load range without requiring additional active circuits or complex control strategies.

## VI. CONCLUSION

In this article, we propose a hybrid modulation scheme for an adaptive coupled-inductor-based IPOS-DAB converter for energy storage integrated dc microgrids with a wide voltage gain range. The scheme consists of APWM, PSM, and coupled inductor modulation. APWM adjusts the voltages of the dc blocking capacitors to achieve voltage match of the primary and secondary sides. With the phase shifts, the ZVS range is expanded over a wide voltage range. Besides, the coupled inductor modulation further optimizes the rms current with self-adaptive equivalent inductances. Operational principles of the modulation, control strategy, and design considerations are analyzed in detail. Finally, a 2-kW prototype linking 200–400 V battery modules and an 800 V dc bus is built to validate the concepts. The experimental steady-state waveforms, ZVS waveforms, and efficiency curves are illustrated. The prototype achieves a peak efficiency of 98.3% and keeps the efficiency above 96.0% within above 20% load range.

## ACKNOWLEDGMENT

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