Threshold Voltage Drift in GaN Power Modules Under Mass Production: Evaluation and Solution to Overcurrent Protection Failure

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***Abstract*—Threshold voltage V_{th} drift in gallium nitride (GaN) high-electron-mobility transistors remains a major reliability barrier for mass-produced power modules, causing latent and unpredictable failures in critical power conversion functions such as overcurrent protection (OCP) during startup, in critical applications such as data center hybrid switched capacitor converters. While device-level solutions exist, there remains a certain gap between these solutions and their practical application in large-scale commercial production. This article presents a converter-level framework to estimate and mitigate voltage-drift issue at scale. It quantitatively describes the impact of device threshold voltage drift on circuit behavior. Crucially, it propose using the output charge integral during a fixed detection plateau as a circuit-observable proxy for drift. By evaluating the soft-start parameters, it enlarge the safety margin to prevent OCP failures. Experimental validation on 6000+ modules shows a failure rate reduction to 0.05% (from 3.1% baseline) after parameter adjustment. This work enables cost-effective, software-only reliability enhancement for GaN-based power modules in industrial deployment.**

***Index Terms*—Gallium nitride (GaN), mass production, power module, reliability, threshold voltage drift, transient modeling, soft-start.**

I. Introduction

GALLIUM nitride high-electron-mobility transistors (GaN HEMTs) have demonstrated market dominance in medium- and low-power charging applications—enabled by nearly a decade of laboratory research. Significant progress has been made in device structures, driving schemes, and packaging techniques, with these improvements validated across a wide range of power levels. In the data center applications, the growing demand for high-power-density and high-dynamic-load power supplies in computing systems is driving the industry toward commercialization of GaN-based power modules. Manufacturers are increasingly transitioning from laboratory-scale demonstrations to practical deployment. However, the shift to mass production has revealed critical non-cost-related challenges at the converter level. Among these, extensive empirical studies have identified dynamic ON-resistance (R_{ds}) and threshold voltage (V_{th}) drift as primary concerns. These dynamic effects strongly influence converter-level transient behavior and pose significant obstacles to achieving high production yield.

Threshold voltage drift has long been recognized as a key reliability concern for GaN HEMTs. While this issue has been extensively studied, most prior research has focused on device-level mechanisms. A variety of stress conditions, such as gate bias temperature instability and OFF-state high-voltage stress, have been shown to cause either positive or negative V_{th} drift depending on device structure and process variations [1], [2], [3], [4], [5]. To mitigate V_{th} drift at the device level, several structural design strategies have been proposed. Cascode architectures combining SiC JFETs and GaN HEMTs [6], [7], [8] effectively isolate the gate from stress-induced degradation. Hybrid gate structures, such as p-GaN/MIS combinations [9], have also shown promise in stabilizing gate control characteristics. However, these techniques are largely confined to laboratory prototypes and are not yet compatible with mass production or commercial-grade process flows. Challenges remain in translating these advanced structural solutions into cost-effective, scalable manufacturing practices. Laboratory-developed device-level solutions for V_{th} stability have not been widely adopted by mainstream GaN HEMT manufacturers (e.g., Innoscience, Navitas, and EPC), requiring more time for commercialization and large-scale production application.

Currently, the popular device structures, such as enhancement-mode (E-mode) GaN HEMTs, still suffer from V_{th} drift. This reliability issue remains unresolved in practical, mass-produced devices. Since hardware-level modifications are limited by manufacturing constraints and cost, circuit-level solutions are essential to mitigate the impact of V_{th} drift in commercial applications. At the circuit level, most studies have

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focused on the dynamic modeling and measurement of GaN HEMT devices, while relatively few have paid attention to the impact of device dynamics on circuit behavior. Among the research related to the influence of dynamic device parameters on circuit performance, researchers have mainly focused on the effect of dynamic resistance on circuit efficiency [10], [11], [12], [13], [14], [15]. These efforts provide valuable insight into transient performance but largely overlook the influence of V_{th} drift on overall circuit behavior. One major challenge is that threshold voltage is inherently difficult to measure in real-time circuit operation. Moreover, its impact is often negligible at low switching frequencies, further contributing to the scarcity of related circuit-level studies. However, with the development of power electronics technology, more and more studies have adopted switching frequency above megahertz [16], [17], [18], [19], [20], [21], [22], which will make the impact caused by threshold voltage drift more significant. Although prior works such as those by Yang et al. [2] and Wang et al. [23] proposed that raising the gate voltage above 5 V could help mitigate V_{th} drift, such high gate voltages are beyond the safe operating range of most commercial GaN HEMTs. For GaN HEMTs, increasing the gate drive voltage is an extremely risky practice—especially for those deployed in low-voltage application scenarios. This operation introduces an extremely high risk of gate breakdown and permanent device failure.

To bridge the gap between device-level physical mechanisms and converter-level reliability challenges, this work proposes a converter-level solution for large-scale estimation of V_{th} drift in GaN-based hybrid switched-capacitor (HSC) modules. These HSC modules are widely adopted in data center power supply systems, and serve as the research vehicle and engineering verification object of this study .

The rest of this article is organized as follows. Section II establishes the HSC startup transient model and defines the output current integral (Q_o). Section III models V_{th} drift as GaN HEMT ON-time variation, develops the V_{th}–Q_o correlation model using the transient model, and proposes a software-based nonintrusive detection method without hardware modifications. Compared with the Pulsed *I*–*V* and custom test circuit methods, this method needs no destructive module testing, hardware modification or extra circuits, and can be implemented only by firmware upgrade, suitable for large-scale mass production and application. Section IV (Experiments) verifies the modeling reliability via GaN HEMT destructive testing. Section V (Experiments) validates the proposed overcurrent protection (OCP) method's effectiveness with over 6000 power modules from three batches. Compared with noncommercial device-level solutions and high-risk high gate voltage schemes, the pure software converter-level solution proposed in this work is better suited for mass production and large-scale industrial application. Finally, Section VI concludes this article.

In the aforementioned workflow, this work innovatively observed and revealed the significant influence of GaN HEMT V_{th} drift on circuit behavior, namely OCP—a fundamental function of power modules, based on one of the few large-scale commercial IBC modules for data center power supply. A modeling method was then proposed to uncover the mechanism of V_{th} drift affecting circuit behavior, and a pure software-based solution was derived from the model. The reliability of the modeling method and effectiveness of the software solution were verified by multibatch, multidimensional, and large-scale experiments. This modeling method is also applicable to other GaN-based circuits. Validated on more than 6000 industrial-grade modules, the proposed software-only and firmware-upgradable solution significantly improves yield in mass production and long-term reliability enhancement in the field, addressing a key bottleneck in the commercialization of GaN technologies for data center power systems.

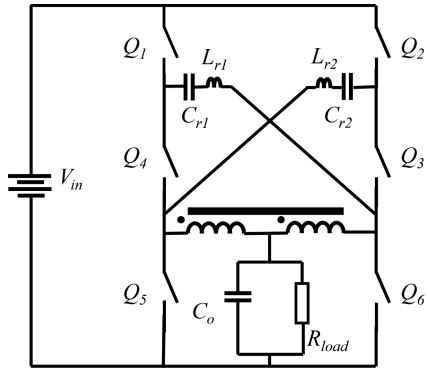

Fig. 1. Topology of the HSC circuit.

II. GaN-Based HSC Converter

A. Converter Topology

The HSC converter is widely employed as the unregulated stage in power conversion systems, as shown in Fig. 1. Combined with the superior performance of GaN HEMTs, HSCs have demonstrated particular suitability for front-end applications—such as 48-V/12-V DC–DC transformers—in data center applications. The steady-state performance of GaN-based HSCs has been well validated in prior papers [23]. In recent years, several power module manufacturers (including Delta Corp.) have explored the integration of GaN HEMTs into 4:1 HSC designs.

Unlike Si MOSFETs, V_{th} variation in GaN HEMTs occurs not only during device fabrication but also after the converter assembly. For instance, in an Si-based HSC converter, once the V_{th} is verified to be stable during testing, it generally remains reliable throughout its operational life. However, for GaN-based HSCs, even if the converters pass all manufacturer-side quality inspections, failures may still occur after a certain period of customer usage. A significant number of these failures have been traced to unpredictable V_{th} drift, which compromises the effectiveness of OCP mechanisms—particularly during large-transient procedures.

The most practical mitigation strategy is to address the issue from a software perspective. After the HSC is fabricated, the GaN HEMTs are typically soldered directly onto the printed circuit board (PCB), making it extremely challenging to measure V_{th} variations in a straightforward and efficient manner. Therefore, this work aims to develop a converter-level model that

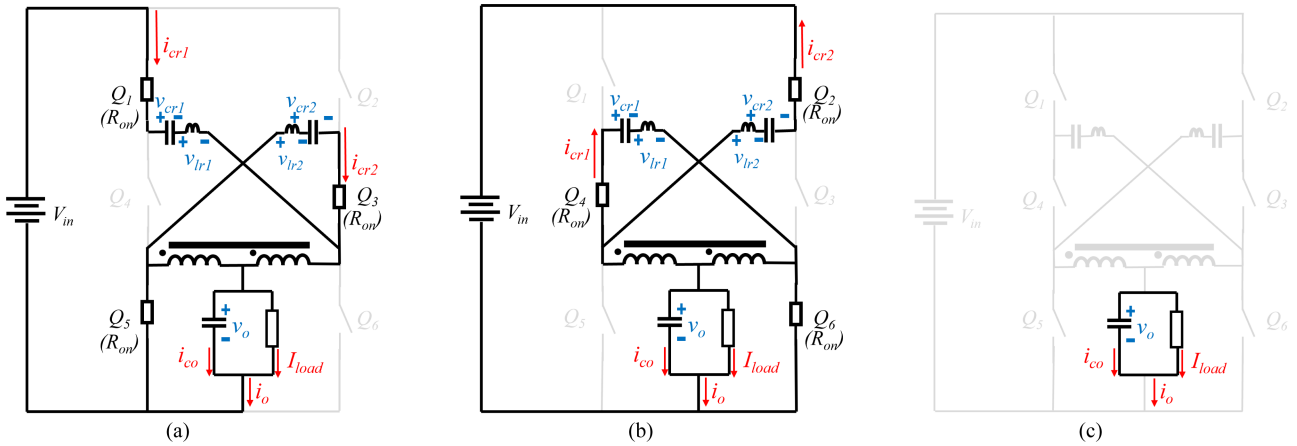

Fig. 2. Three modes. (a) Mode 1. (b) Mode 2. (c) Mode 3.

can equivalently reflect the impact of V_{th} drift, and to propose a simple, low-cost solution to enhance of reliability of OCP.

B. Transient Model

The HSC converter shown in Fig. 1 consists of six transistors (Q_1–Q_6), two resonant inductors (L_{r1} and L_{r2}), two resonant capacitors (C_{r1} and C_{r2}), a coupled inductor with unity coupling coefficient, and an output filter capacitor C_o. This configuration is well known for its fixed voltage conversion ratio, such as $V_{\text{in}} : V_o = 4 : 1$, making it suitable for front-end applications in data centers. In the transient model, each transistor is represented as a fixed ON-state resistance when conducting and as an open circuit when turned OFF. The output load is modeled as a purely resistive element (R_{load}).

There are three typical operation modes for the HSC converter as shown in Fig. 2. The key state variables of the system include the voltages and currents of capacitors C_{r1} and C_{r2}, denoted by $v_{cr1}, i_{cr1}, v_{cr2},$ and i_{cr2}, respectively, as well as the output voltage v_o.

1) Mode 1: In this mode, switches Q_1, Q_3, and Q_5 are turned ON, as illustrated in Fig. 2(a). The corresponding state-space equations are given by

$$\begin{cases} \frac{dv_{cr1}}{dt} = \frac{i_{cr1}}{C_{r1}}, \\ \frac{dv_{cr2}}{dt} = \frac{i_{cr2}}{C_{r2}}, \\ \frac{di_{cr1}}{dt} = \frac{-i_{cr1}R_{\text{on}} - v_{cr1} - 2v_o + V_{\text{in}} - (2i_{cr2} + i_{cr1})R_{\text{on}}}{L_{r1}}, \\ \frac{di_{cr2}}{dt} = \frac{-v_{cr2} - i_{cr2}R_{\text{on}} - 2v_o - (2i_{cr1} + 4i_{cr2})R_{\text{on}}}{L_{r2}}, \\ \frac{dv_o}{dt} = \frac{2i_{cr1} + 2i_{cr2} - I_{\text{load}}}{C_o}. \end{cases} \tag{1}$$

2) Mode 2: When switches Q_2, Q_4, and Q_6 are conducting, as depicted in Fig. 2(b), the converter operates in Mode 2. The system dynamics are described by

$$\begin{cases} \frac{dv_{cr1}}{dt} = \frac{i_{cr1}}{C_{r1}} \\ \frac{dv_{cr2}}{dt} = \frac{i_{cr2}}{C_{r2}} \\ \frac{di_{cr1}}{dt} = \frac{-i_{cr1}R_{\text{on}} - v_{cr1} + 2v_o - (4i_{cr1} + 2i_{cr2})R_{\text{on}}}{L_{r1}} \\ \frac{di_{cr2}}{dt} = \frac{2v_o - (2i_{cr1} + i_{cr2})R_{\text{on}} - V_{\text{in}} - i_{cr2}R_{\text{on}} - v_{cr2}}{L_{r2}} \\ \frac{dv_o}{dt} = \frac{-2i_{cr1} - 2i_{cr2} - I_{\text{load}}}{C_o}. \end{cases} \tag{2}$$

3) Mode 3: In this mode, all six switches are turned OFF, as shown in Fig. 2(c). The converter enters a freewheeling state, and the system dynamics simplify to

$$\begin{cases} \frac{dv_{cr1}}{dt} = 0 \\ \frac{dv_{cr2}}{dt} = 0 \\ \frac{di_{cr1}}{dt} = 0 \\ \frac{di_{cr2}}{dt} = 0 \\ \frac{dv_o}{dt} = -\frac{I_{\text{load}}}{C_o}. \end{cases} \tag{3}$$

4) Initial Conditions: To analyze the converter's transient response during startup, the initial conditions is specified as $v_{cr1} = v_{cr2} = i_{cr1} = i_{cr2} = v_o = 0$. Once the time durations of each operation mode are determined, the state variables can be predicted by sequentially solving the aforementioned differential equations based on the mode transitions.

C. Large Transient Process: Soft-Start

It is well established that V_{th} drift can lead to a significant mismatch between the intended gate-driving signal and the actual device turn-ON time. Consequently, the worst condition often occurs during the high-frequency startup process, where even small deviations can cause substantial changes in the gate-driving waveform. For an unregulated HSC, it is generally necessary to fine-tune the startup parameters to ensure the effectiveness of OCP, particularly in light of potential V_{th} shifts following converter fabrication.

Commercial HSC converters typically adopt a soft-start strategy that employs fixed-frequency and variable-duty-cycle control, coupled with OCP. When evaluating the current-handling capability of GaN HEMTs, both the magnitude and duration of the current must be taken into account due to their impact on thermal stress.

A representative startup profile of the gate-driving signal is illustrated in Fig. 3. During the initial interval ($t < t_a$), the pulsewidth modulated (PWM) duty cycle increases linearly, allowing the system to gradually accumulate energy.This fixed-frequency PWM signal is generated by the microcontroller unit (MCU). The duty cycle increases linearly by 0.1% every 50

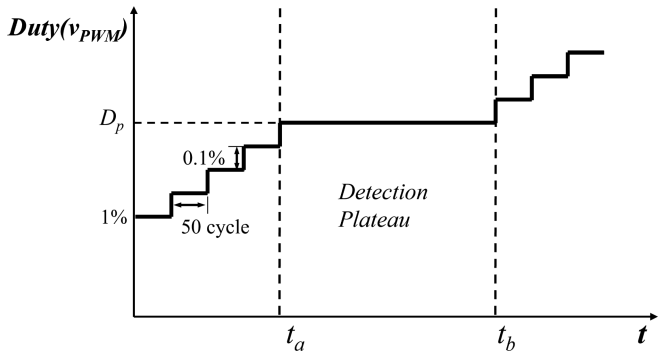

Fig. 3. Gate driving signal during the soft-start with OCP.

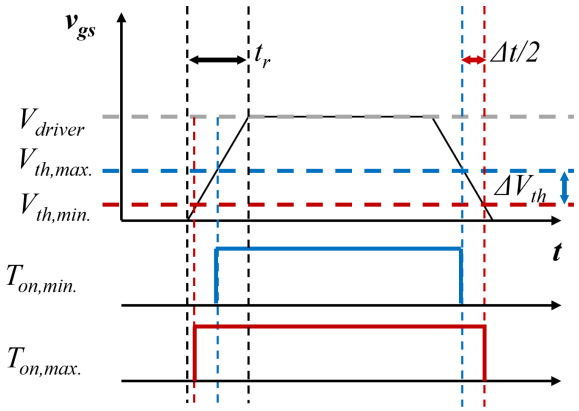

Fig. 4. Influence of V_{th} drift on the actual conduction time.

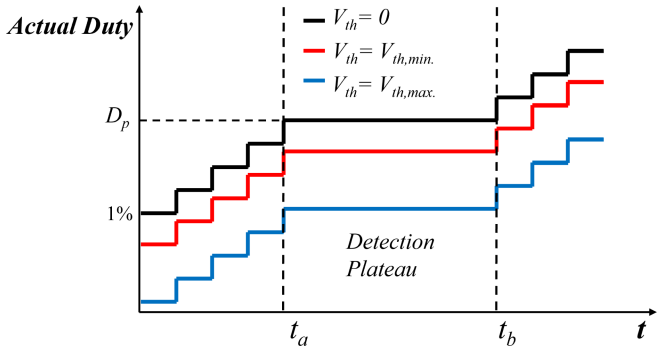

Fig. 5. Actual device on time under different V_{th}.

cycles. When the duty cycle rises to the preset value D_p, it is held constant for 50 cycles to form a fixed detection plateau. Upon completion of the OCP detection, the duty cycle continues to increase linearly until it reaches the steady-state operating condition. In the subsequent interval ($t_a < t < t_b$), the duty cycle is held constant (i.e., D_p) to form a current observation plateau. During this period, the integral of the output current is computed as

$$Q_o = \int_{t_a}^{t_b} i_o(t)\, dt. \tag{4}$$

This integral, Q_o, is then compared against a reference value Q_{ref} obtained under nominal conditions. If the observed value exceeds the reference threshold, it indicates potential overcurrent conditions. Once the system passes the overcurrent check, the duty cycle continues to ramp up until reaching the steady-state operating condition ($t > t_b$).

During the quality-check process, a fabricated module is expected to successfully activate the OCP during short-circuit startup when over load happens. Furthermore, this protection mechanism should remain effective throughout its operational lifetime. This assumption holds for Si-based HSC modules. However, when applied to their GaN counterparts, the module may initially pass the quality check but later fail to trigger OCP after prolonged usage. Therefore, this work aims to model the V_{th} drift and investigate its detrimental impact on protection reliability from a converter-level perspective.

III. Threshold Voltage Drift

A. Device On-Time Variation

The V_{th} drift of GaN HEMTs can occur both during fabrication and during operation. A direct impact of V_{th} drift is the variation in the actual conduction time of the device. Turning the GaN HEMT ON or OFF involves charging or discharging the gate capacitance, which causes the gate–source voltage v_{gs} to rise or fall. This work studies this problem from the converter-level perspective, which necessitates a simplified model describing the effect of V_{th} drift on ON-time variation.

In this study, v_{gs} is approximated by a simple isosceles trapezoidal waveform, as illustrated in Fig. 4. When V_{th} drifts within a defined range, i.e., $[V_{\text{th,min}}, V_{\text{th,max}}]$, the effective turn-ON time correspondingly changes. For instance, a smaller $V_{\text{th,min}}$ results in a longer conduction period, whereas a larger $V_{\text{th,max}}$ shortens it. The total drift range $\Delta V_{\text{th}} = V_{\text{th,max}} - V_{\text{th,min}}$ leads to a conduction time variation denoted as Δt. This work proposes a simplified linear relationship between ΔV_{th} and Δt to characterize the influence of threshold voltage drift on converter operation. Note that the established linear relationship is not a linear model for the physical mechanism of V_{th} drift itself, but only for approximating the effect of V_{th} variations on the device effective ON-time Δt.

In a low-frequency system, v_{PWM} of Fig. 3 is sufficient to represent the real conduction time of a transistor. Given the initial state and known v_{PWM}, it is able to use the transient model to predict the state variables and guide the design of OCP parameters. Based on the simplified model of Fig. 4, it assume there is a linear relationship between ΔV_{th} and Δt. Therefore, the given v_{PWM} is able to predict the range of actual conduction time of a GaN HEMT. As shown in Fig. 5, the black line means v_{pwm} (i.e., $V_{\text{th}} = 0$), the blue line means $V_{\text{th}} = V_{\text{th,min}}$, and the red line means $V_{\text{th}} = V_{\text{th,max}}$.

B. V_{th}–Q_o Curve

This article proposes employing Q_o as an indicator for estimating V_{th} drift and addressing the associated OCP challenge in mass production. The parameters of a representative HSC converter, along with its startup configuration, are listed in Table I. By combining these converter parameters with any case in Table II, key state variables, including the output current i_o

TABLE I
CIRCUIT PARAMETERS

Parameter	Value	Parameter	Value
Cr_1, Cr_2	880 nF	Lr_1, Lr_2	30 nH
R_{on}	2.4 mΩ	C_o	1 mF
f_s	1 MHz	D_p	3.8%
V_{drive}	5 V	t_r	90 ns
t_a	1400 μs	t_b	2700 μs

TABLE II
SIX OPERATING CONDITIONS

	Case A	Case B	Case C
V_{in}	60 V	40 V	60 V
I_{load}	20 A	20 A	0 A
	Case D	Case E	Case F
V_{in}	40 V	48 V	48 V
I_{load}	0 A	20 A	0 A

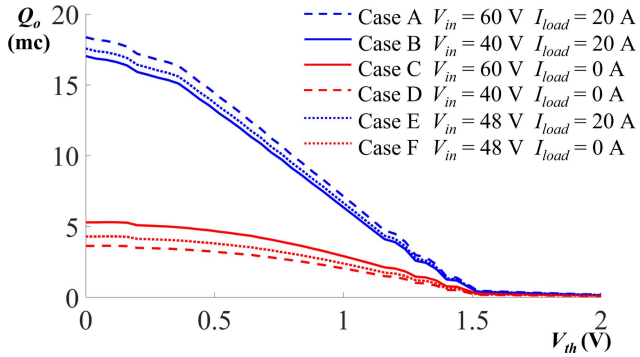

Fig. 6. V_{th}–Q_o curve of six cases.

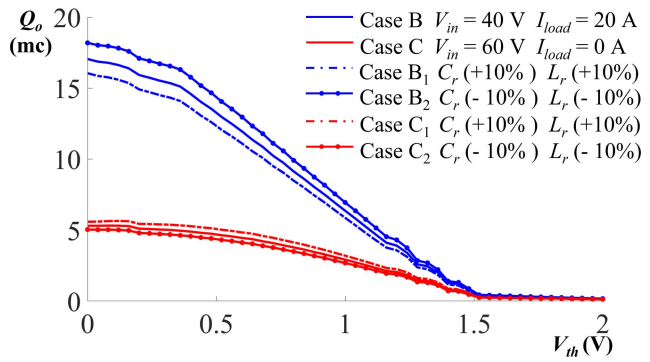

Fig. 7. V_{th}–Q_o curve considering passive component deviations.

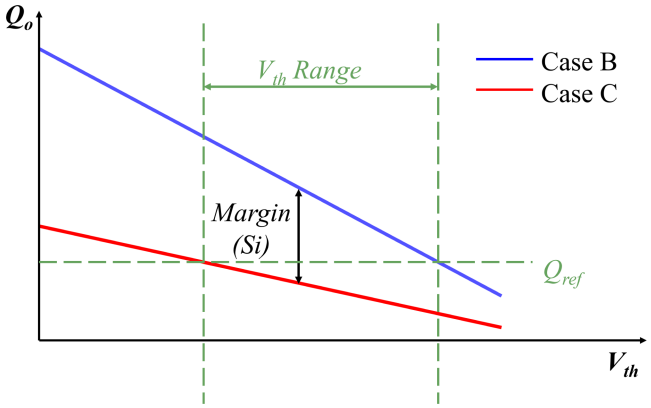

Fig. 8. Design margin of Q_{ref}.

and the charge quantity Q_o, can be obtained using the transient model.

As shown by the blue dash curve in Fig. 6, each specific V_{th} corresponds to a unique Q_o [refer to (4)] when Case A is adopted. For $V_{\text{th}} = 0$, the gate signal v_{pwm} aligns exactly with the transistor conduction interval, yielding the maximum Q_o. Q_o decreases approximately linearly with increasing V_{th}, stabilizing at high V_{th} due to the small duty cycle (D_p =3.8%). In this regime, the device remains nearly OFF.

The terminal conditions also influence the V_{th}–Q_o curve. When adopting other cases from Table II, the blue curve, red curve, and red dash curve, respectively, are obtained in Fig. 6. For an unregulated HSC operating over a wide input voltage range (from 40 to 60 V), Cases A, B, and E correspond to overload conditions in which the OCP should be triggered. Cases C, D, and F represent nominal startup conditions with zero output current. The Q_o-based OCP must reliably distinguish between these two scenarios, particularly in the presence of V_{th} drift.

Moreover, deviations in capacitance and inductance of passive components are commonly encountered in large-scale mass production. Considering a maximum parameter tolerance of 10%, Case B_1, Case B_2, Case C_1, and Case C_2 are plotted in Fig. 7. It can be observed that compared with V_{th} drift, the deviations of capacitance and inductance of passive components impose an insignificant influence. Such deviations do not change the overall trend of the V_{th}–Q_o relationship and only slightly affect its amplitude. This indicates that the method for improving the overcurrent detection margin presented in the next subsection remains still applicable when taking passive component tolerances into account.

C. Design Margin of Q_{ref}

When a commercial power module is fabricated, it must pass a quality check to ensure functional reliability. The Q_o-based OCP inherently accounts for thermal effects; thus, the objective is to set Q_{ref} to identify overload conditions. However, it has been observed that when Q_{ref} for a GaN-based module is chosen in the same manner as for its Si counterpart, the module may pass the initial OCP check but fail after a period of operation. In such cases, OCP may either fail to activate during an actual overload event or be falsely triggered in the absence of an overload.

The selection of Q_{ref} is relatively straightforward. First, a reference current—for example, 20 A—is defined as the OCP threshold. As shown in Fig. 6, Q_o is positively correlated with the input voltage. To distinguish between the 0- and 20-A operating conditions of I_{load} over the full input voltage range (40–60 V), it is only necessary to focus on the two curves of Case B and Case C, which is the lower boundary of 20-A cases and the upper boundary of 0-A cases, as shown in Fig. 6.

To illustrate the selection of Q_{ref}, a simplified V_{th}–Q_o schematic is presented in Fig. 8, considering only Cases B and C. The x-axis is the real-time V_{th} of the GaN HEMT. For an Si-based module, the V_{th} drift is negligible, and the design margin of Q_{ref} is represented by the black vertical line at a fixed V_{th}. In contrast,

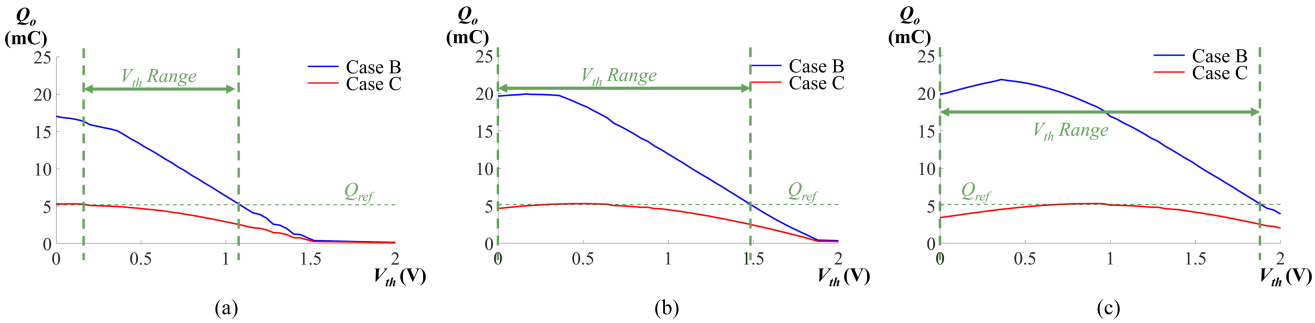

Fig. 9. Influence of D_p. (a) $D_p = 3.8\%$. (b) $D_p = 4.8\%$. (c) $D_p = 5.8\%$.

for a GaN-based module, the variation of V_{th} must be taken into account. Given a specific Q_{ref}, its intersections with the blue and red curves define a corresponding range of V_{th}. Within this voltage range, the chosen Q_{ref} can effectively distinguish between the two operating conditions. When the GaN HEMT V_{th} drifts to the left of this range, the OCP misidentifies normal startup as overcurrent events via Q_{ref} and causes startup failure. When the V_{th} drifts to the right of this range, the OCP mistakes overcurrent startup for normal ones, leading to module burnout. Such failures are inadmissible for data center power supply applications, and this also accounts for the 3.1% error rate in the first batch of 973 samples mentioned later.

D. Mitigating the Conflict Between Q_{ref} and V_{th} Range

A qualified module must have both soft-start and OCP functionality. Therefore, testing the OCP during soft-start is often used as one of the most important transient tests for the module. As a result, the soft-start parameters are closely related to the OCP's Q_{ref}. The soft-start parameters include t_a, t_b, and D_p. As shown in Fig. 3, v_{pwm} increases by 0.1% every 50 cycles and the time window $(t_b - t_a)$ is fixed, D_p is the only design parameter. An increase in D_p effectively corresponds to larger values of both t_a and t_b.

When $D_p = 3.8\%$, Fig. 9(a) presents two Q_o–V_{th} curves corresponding to Case B and Case C of Table II. Select an example Q_{ref}, its intersections with the two curves define a V_{th} range. In this case, the chosen Q_{ref} allows 100% discrimination between nominal and overload conditions when V_{th} lies within the green region. By increasing D_p to 4.8% as shown in Fig. 9(b), the selected Q_{ref} results in a wider V_{th} range. Further increasing D_p can expand this range even more. Therefore, the soft-start parameter D_p is able to mitigate the conflict between Q_{ref} and V_{th} range. Nonetheless, since a larger D_p implies larger t_a and t_b, the increase in t_a may exacerbate heat failure risks during the soft-start process. A large D_p should be avoided in practice. It should be noted that adjusting the D_p parameter does not affect the total time consumed during the entire startup process. As is well known, the drift of threshold voltage is inherently bounded. Appropriately increasing D_p can extend the V_{th} coverage range to fully accommodate the maximum V_{th} drift interval. In addition, the introduction of the detection platform only increases the startup time by 6% (1.5 ms/25 ms) compared with the soft-start process without the OCP function.

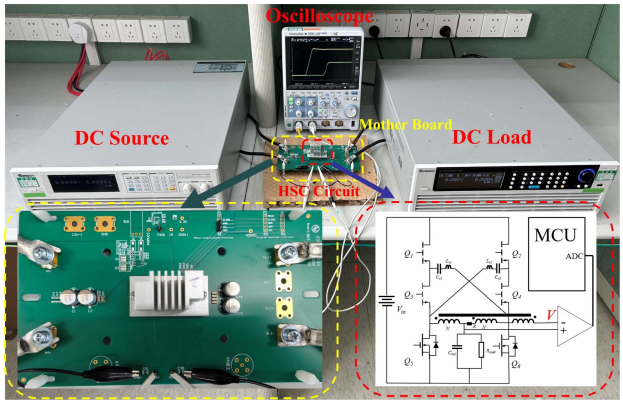

Fig. 10. Converter-level test.

This modeling method is also applicable to other GaN-based topologies with similar startup modes (e.g., Buck and *LLC*), for analyzing and predicting the impact of V_{th} drift on these topologies.

IV. Experimental Verification of Ten Converters

A. Test Setup for Converter and Device

An experimental platform for the converter is established to indirectly detect Q_o, thereby validating the V_{th}-related transient model and demonstrating the effectiveness of the modified soft-startup logic. As shown in Fig. 10, a commercial 1-MHz, 48-V/12-V, 800-W HSC is integrated onto a custom-designed motherboard. The system is powered by a DC source (Chroma 62100H-100P) and connected to an electronic load (Chroma 63203A-150-300). The transient waveforms are captured using an oscilloscope (YOKOGAWA DLM3054). At the center of the motherboard lies the HSC converter, where switches Q_1, Q_2, Q_3, and Q_4 are implemented with GaN HEMTs, while Q_5 and Q_6 remain Si MOSFETs due to cost considerations. The parameters of the remaining circuit components are summarized in Table I. The circuit used for current detection and Q_o estimation is illustrated in the right corner of Fig. 10. By utilizing the auxiliary winding, the output current is sensed and subsequently transmitted to the MCU for further processing.

In addition to the converter-level test, a device-level test is conducted to accurately measure V_{th}. It is important to note that the tested device is not a new one but the same GaN HEMT

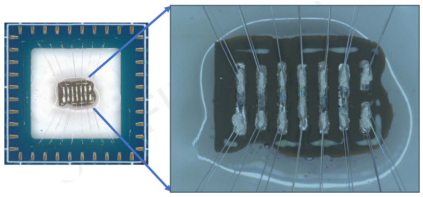

Fig. 11. Device-level test.

previously used in the converter. Since temperature variations can affect V_{th}, the device is not removed using a hot air gun. Instead, a destructive method is adopted: the PCB board, to which the GaN HEMT is soldered, is mechanically ground using an angle grinder to expose the device leads, as illustrated in Fig. 11. This approach ensures that the measured V_{th} corresponds to its actual value during the converter-level operation.

B. V_{th}–Q_o Model Verification

The device-level test enables accurate measurement of V_{th}. However, as this test requires destructive disassembly of the converter, only ten modules are selected for measurement. It should be noted that, to further guarantee the reliability of the measurement, relevant tests on a large scale of more than 6000 modules are performed in the subsequent experimental section of this work to verify the reliability of the proposed scheme based on the V_{th}–Q_o model. In the OCP test, the output current is fixed at 20 A. Of the ten modules subjected to destructive tests, OCP was triggered successfully in eight modules and failed to trigger in the remaining two. The typical waveforms corresponding to successful and failed OCP operations are shown in Fig. 12. It should be noted that a test failure does not indicate device failure of the GaN HEMTs; rather, it implies that the startup parameters are not sufficient to ensure the module passes the protection test. Even among the successful modules, noticeable differences in current waveforms are observed. The transient model proposed in this article is not intended to predict the full transient current waveform; instead, it aims to relate the detected Q_o within a specific observation plateau to the corresponding V_{th}.

The Q_o values is obtained from the converter-level test. Subsequently, all the GaN HEMTs are removed for a device-level test to further validate the proposed V_{th}–Q_o model. Fig. 13 is plotted by mapping the average V_{th} of each module onto the curve derived in Fig. 6. The measured data show good agreement with the model predictions.

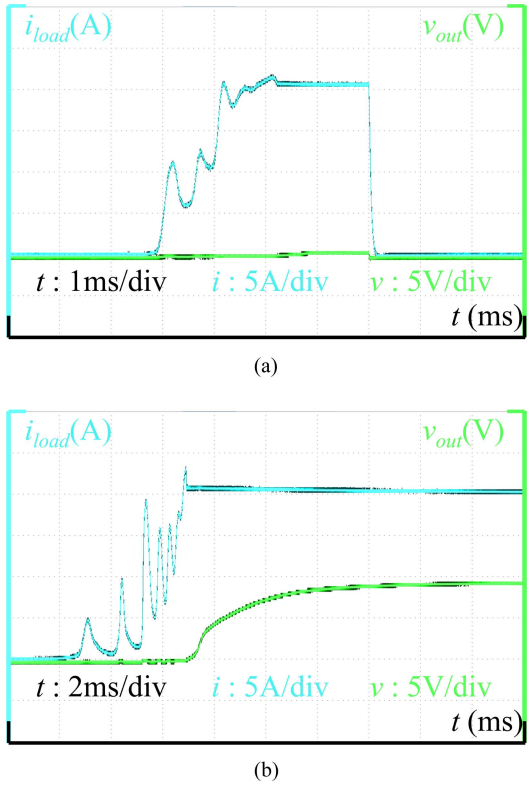

Fig. 12. Typical Waveform of OCP. (a) OCP triggered successfully. (b) OCP failed to trigger.

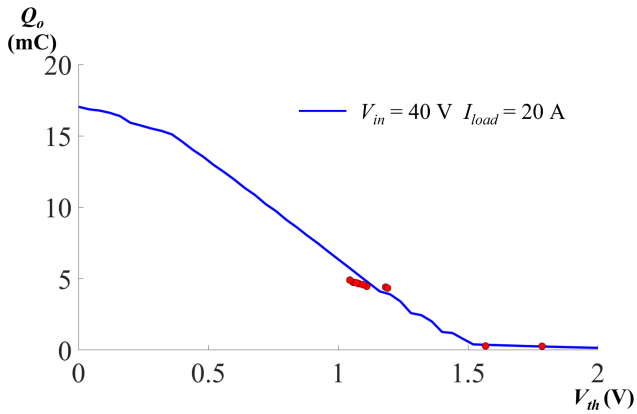

Fig. 13. Experimental verification of $V_{\text{th}} - Q_o$ model.

V. Massive Test and Validation

A. Burn-In Test

After the model is validated through the device-level test, it becomes feasible to monitor Q_o in order to identify V_{th} drift and evaluate the effectiveness of the OCP design. Since the mechanism of V_{th} drift is complex and influenced by various factors—such as blocking voltage and ambient temperature—it exhibits a certain degree of randomness at the circuit level. To expedite the emergence of V_{th} drift in a short period, accelerated aging tests were performed following multiple internationally accepted authoritative standards [24], [25], [26], [27], [28], [29], [30], for simulating the V_{th} drift of power modules during long-term operation (e.g., 1000 h). The burn-in test intensifies the electron trapping effect by holes via high temperature and high OFF-state voltage stress, which reduces the density of the 2DEG and accelerates the V_{th} drift, thus realizing full lifecycle reliability detection of GaN devices. More than 6000 converter samples are tested, providing sufficient data to statistically analyze the probability distribution of Q_o variation.

The one-hour cycle of the burn-in test is illustrated in Fig. 14. The test is conducted at a temperature of $95 \pm 5\,^{\circ}\text{C}$, with a module input voltage of 54 V and an output current of 10 A. In each cycle, the module operates continuously for 40 min,

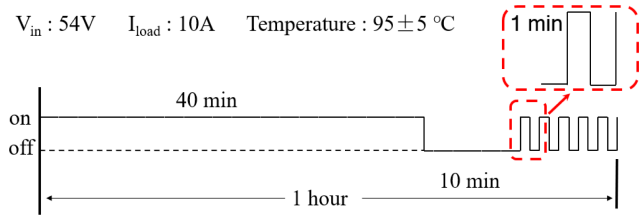

Fig. 14. 16-h burn-in at $95 \pm 5\,^{\circ}\mathrm{C}$ with $V_{\text{in}} = 54$ V and $I_{\text{out}} = 10$ A, following JESD47G [26] and AEC-Q100 [28], is applied to accelerate the V_{th} shift mechanism prevalent in GaN HEMTs, simulating thousands of hours of field operation.

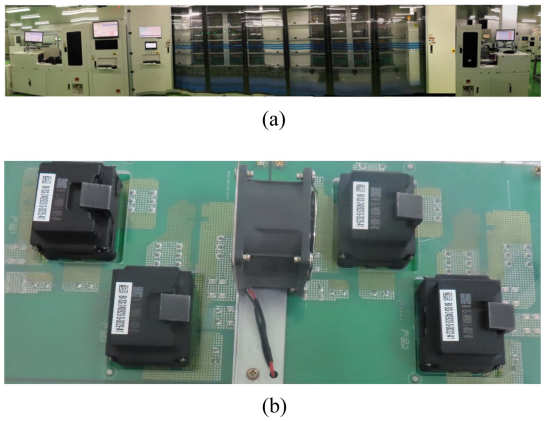

Fig. 15. Platform for the burn-in test. (a) External view. (b) Internal view.

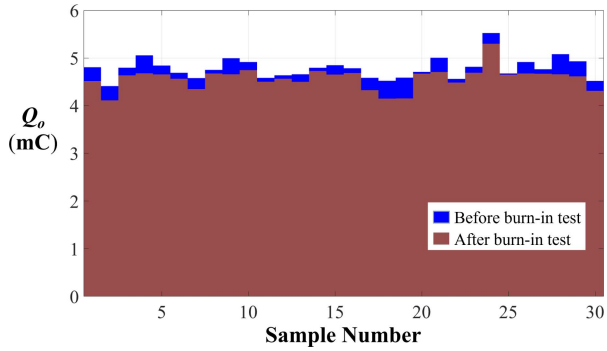

Fig. 16. Q_o comparison of 30 HSC modules before and after burn-in testing.

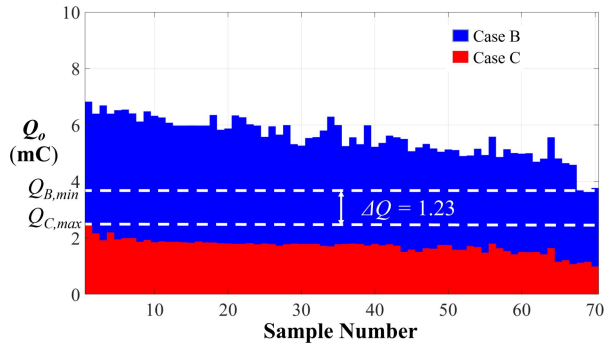

Fig. 17. Measured Q_o of 70 HSC modules when $D_p = 3.8\%$.

followed by a 10-min idle period. During the final 10 min, the module alternates between ON and OFF states every minute to introduce additional switching stress. The entire test consists of repeated execution of this cycle.

The burn-in test platform is shown in Fig. 15(a). An industrial computer is used to control the internal temperature of the central burn-in cabinet, as well as the input voltage and output load of the modules. The power supply motherboard inside the burn-in cabinet, which powers the modules under test, is depicted in Fig. 15(b). The HSC modules are placed directly into four black molds for simultaneous burn-in testing. With this setup, a large number of HSC modules can be efficiently subjected to burn-in testing under controlled and accelerated aging conditions.

B. Massive Validation

A total of 973 HSC converters were initially fabricated and tested. After calibrating their overcurrent detection threshold values Q_{ref}, they underwent a 16-h burn-in test. Upon completion of the burn-in process, the OCP functionality of each converter was verified by setting $D_p = 3.8\%$, as illustrated in Fig. 9(a). Among these samples, 30 HSC converters exhibited a significant reduction in Q_o during startup compared to their preburn-in levels, as shown in Fig. 16, resulting in failure of their OCP function. This corresponds to a failure rate of 3.1% ($= 30/973$). This indicates that 30 HSC modules initially succeeded in identifying the overload condition but failed to do so after the burn-in process, due to V_{th} drift. Such a high failure rate is unacceptable from an industry perspective. These failing converters continued startup operation even in the presence of an overcurrent condition, thereby failing the protection test. All failed samples showed a noticeable drop in Q_o, which correlates with an increase in V_{th}.

Q_o-based OCP should ensure there is a clear difference between Case B and C. To further investigate the influence of startup parameters, 70 new HSC converters were fabricated and tested. Initially, $D_p = 3.8\%$ (as used in the previous 973 samples) was applied. In Case B, with $V_{\text{in}} = 40$ V and $I_{\text{load}} = 20$ A, the corresponding Q_o values for all samples are shown in Fig. 17, where each column represents one sample. In Case C, with $V_{\text{in}} = 60$ V and $I_{\text{load}} = 0$ A, the Q_o values were also measured. The difference $\Delta Q = Q_{B,\min} - Q_{C,\max}$ is greater than zero—indicating that none of the tested samples failed the protection function initially. Note that Q_{ref} could be selected between $Q_{B,\min}$ and $Q_{C,\max}$, which define the practical design margin. However, this does not guarantee that the selected startup parameters will always be robust under large-scale production conditions. Note that a failure rate of 3.1% is obtained when $D_p = 3.8\%$.

Based on the conclusions drawn from Fig. 9, increasing D_p can further mitigate the conflict between the Q_{ref} and the V_{th} range. After increasing the startup parameters D_p to 4.8%, as shown in Fig. 9(b), the Q_o values for Cases B and C were reevaluated and are presented in Fig. 18. As predicted by the model, Q_{ref} margin (i.e., ΔQ) increases with the increased D_p. Q_{ref} is, finally, selected in the Q_{ref} margin, such as the black solid line.

The 70 HSC samples were subsequently subjected to a 16-cycle burn-in test. Posttest evaluation of their overcurrent detection capabilities showed that, although a reduction in Q_o was

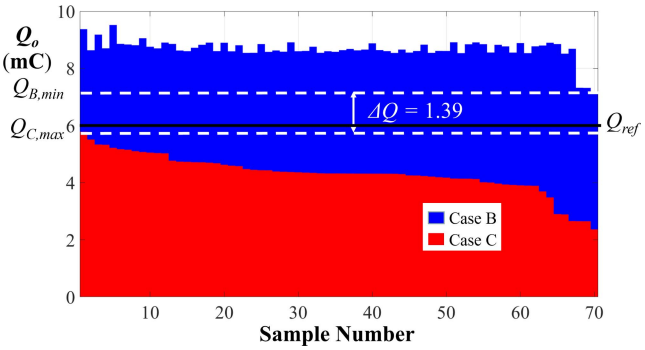

Fig. 18. Measured Q_o of 70 HSC modules when $D_p = 4.8\%$.

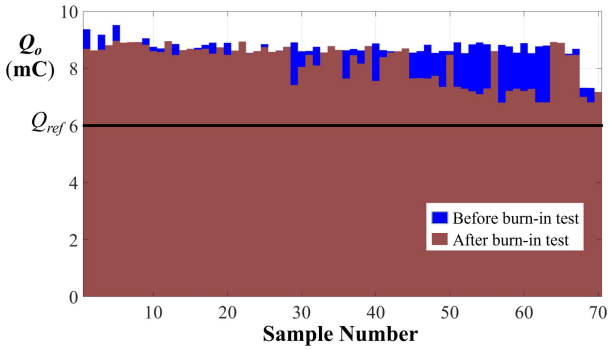

Fig. 19. Measured Q_o of 70 HSC modules after burn-in testing.

observed in several samples, no detection failures occurred. This is attributed to the enlarged Q_{ref} margin shown in Fig. 18. After the burn-in test, Q_o was measured for all samples in Fig. 19. All of these new Q_o values remain above the selected Q_{ref} from Fig. 18, explaining the continued success of OCP after V_{th} drift.

Furthermore, the modified startup parameter was applied to the 30 faulty HSC converters identified from the original batch of 973. Upon retesting, all of these modules successfully passed the OCP test, confirming that the proposed parameter adjustment effectively eliminates detection failures.

Finally, a total of 5981 HSC converters were fabricated and subjected to a 16-h burn-in test, with the failure rate reduced from a baseline of 3.1% to just 0.05%. This result demonstrates the scalability and robustness of the proposed model and startup parameter design when applied to large-scale production.

Fig. 20 is plotted to clarify the inspiration, research framework, and experimental design of this study. Delta Electronics found that the V_{th} drift of GaN HEMTs (distinct from Si devices) significantly affects circuit behavior during large-scale Si-to-GaN replacement. Based on this, we established a theoretical model and designed experiments for three batches of over 6000 HSC modules: the first batch was used for model establishment and issue recurrence, with device-level experiments verifying the model's accuracy and supporting the proposal of a software correction. The second batch conducted small-scale verification of the software correction's effectiveness. Finally, applying the software correction in the 5981-module mass production batch reduced the defect rate from 3.1% (first batch) to 0.05% and repaired the 30 defective modules from the first batch.

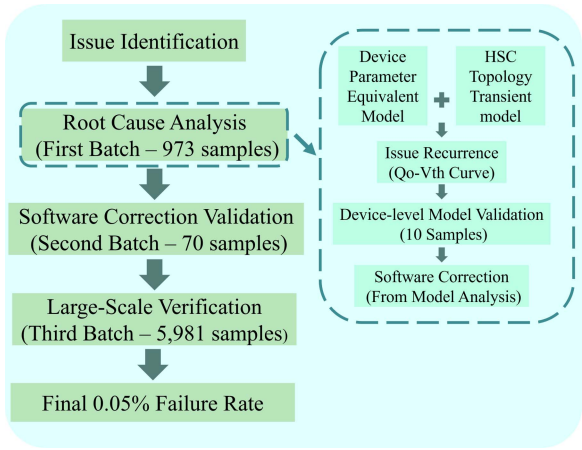

Fig. 20. Experimental design flowchart.

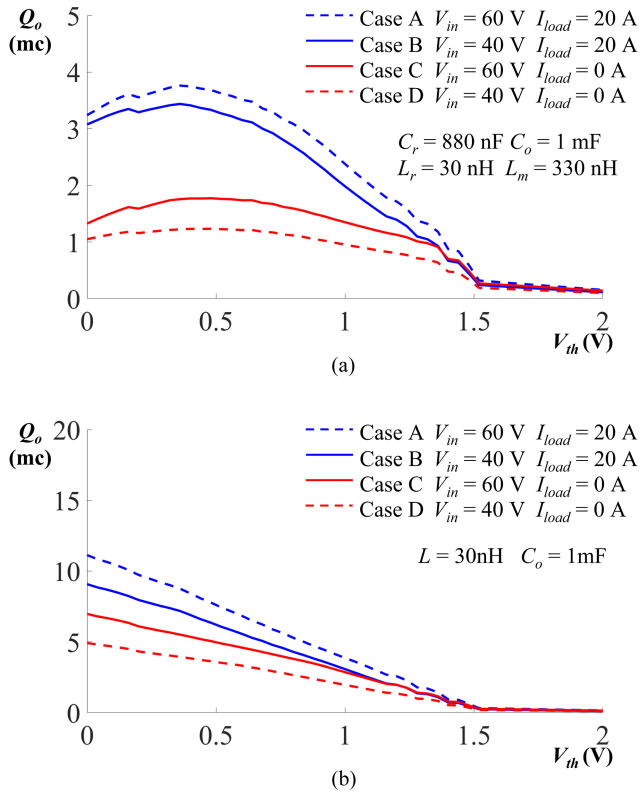

Fig. 21. Example of modeled Q_o–V_{th} curves, with circuit parameters marked in the figure. (a) *LLC*. (b) Buck.

VI. Conclusion

This work addresses the critical reliability challenge of threshold voltage drift in GaN power modules through a scalable circuit-level solution. It introduces a noninvasive monitoring method using output charge integration during soft-start to detect voltage drift, eliminating hardware modifications. By adaptively optimizing startup timing parameters, the proposed approach maximizes fault-detection margins to ensure robust OCP. Validation involved rigorous accelerated aging tests (95 °C for 16 h) compliant with AEC-Q100/JESD47G standards across 6000+

industrial modules. The solution achieved a field-failure rate dropped from an initial 3.1% to 0.05%.

VI. Appendix

The core idea of this article is to establish a mapping from V_{th} variation to conducted Q_o, based on the assumed linear relationship between V_{th} and turn-ON time, under a defined startup sequence and in conjunction with the transient model of the specific converter. This allows calculation of the current integral over any given time window. This V_{th}-to-Q_o mapping follows a general circuit analysis logic and is independent of the converter topology. For example, similar modeling curves can also be obtained for circuits such as *LLC* and Buck, as illustrated in Fig. 21.

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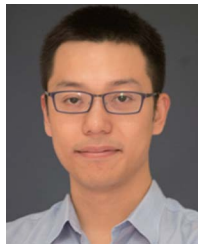

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