Cycle Estimation-Based Deadbeat Interleaving Method for Critical Mode Totem-Pole Rectifiers

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***Abstract*—In totem-pole boost rectifiers, critical mode (CRM) operation is associated with varying switching frequency and duty ratio. This makes it difficult to precisely manage the phase shift between interleaved phases. To address this challenge, we propose a novel interleaving method based on cycle estimation. The switching cycle is estimated by predicting the zero-crossing instants. By analyzing the input current ripple, the relationship among phase shift, duty ratio, and switching cycle can be derived. Therefore, after frequency transition, the phase shift and switching cycle can be updated to provide a precise deadbeat control. Different from conventional methods, the proposed interleaving methods can dynamically modulate the phase shift without the usage of high-speed current sensors. A 1.6 kW, 160–950 kHz GaN-based, two-phase interleaved totem-pole rectifier is designed as the proof of concept. 98.24% peak efficiency and 0.995 power factor are captured. Experimental results effectively validate the interleaving method.**

***Index Terms*—Critical mode (CRM), cycle estimation, interleaving, power factor correction (PFC), totem-pole.**

I. Introduction

In power factor correction (PFC) rectifiers, totem-pole boost topology stands out for low component count, simple structure, and bidirectional power flow [1], [2]. Critical mode (CRM) operation enhances the converter efficiency by achieving zero-voltage switching or valley switching through the resonance between MOSFET C_{oss} and boost inductor. However, the triangular current results in a high input current ripple. This compromises the heavy load performance [3]. Employing multiphase interleaving can enhance the power ratings and mitigate the ripple current [4], [5]. Fig. 1 shows the schematic of a two-phase interleaved totem-pole PFC rectifier. There are two mainstream scenarios for CRM interleaving: fixed switching frequency and variable switching frequency.

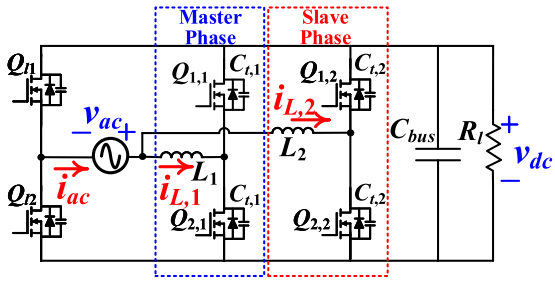

Fig. 1. Schematic of a two-phase interleaved totem-pole PFC rectifier.

In fixed switching-frequency scenarios, the controller updates either the on-time or boost inductance to regulate the input current [6], [7], [8], [9]. Since the switching cycle is fixed, the carrier and modulation waves are fully decoupled. Thus, it is easy to realize phase interleaving. However, for CRM operation, large circulating loss occurs at light load [7]. Increasing the boost inductance can suppress this circulating loss, but at the cost of an additional magnetizing circuit [8], [9]. In summary, although phase interleaving at fixed switching frequency is easy to implement, both efficiency and control remain unsatisfactory.

In variable switching-frequency scenarios, the on-time, switching cycle, and duty ratio all vary according to the input current. This is beneficial to suppressing the circulating current. However, both the carrier and the modulation waves are updated in real-time, and the phase shift also adjusts simultaneously. This necessitates additional control efforts to maintain stable interleaving. Generally, there are two types of variable frequency interleaving methods: 1) closed-loop interleaving; 2) open-loop interleaving.

Closed-loop interleaving utilizes a phase-locked loop (PLL) to dynamically control the phase shift and switching cycle [10], [11], [12], [13], [14], as illustrated in Fig. 2. The activation of master phase (v_{gs-M}) and slave phase (v_{gs-S}) is initiated by the corresponding zero-crossing detection (ZCD) signals. Upon the arrival of ZCD, the carrier is reset, triggering v_{gs-M}. As v_{gs-M} rises, the output of the phase detection flip-flop ($Ph_{diff,1}$) also rises. Subsequently, when v_{gs-S} rises, $Ph_{diff,1}$ resets. The duty ratio of $Ph_{diff,1}$ is determined using the enhanced capture module (ECap) in the microcontroller, indicating the phase shift between the master and slave phases.

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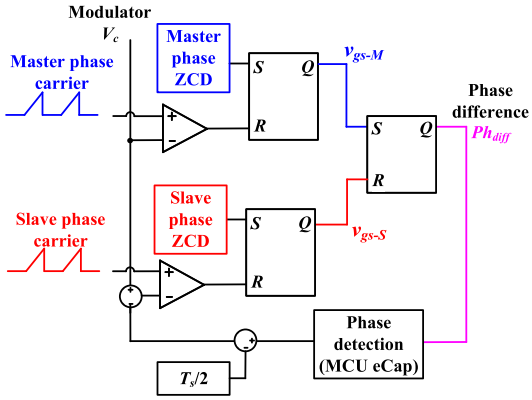

Fig. 2. A CRM phase interleaving scheme based on phase-locked loop.

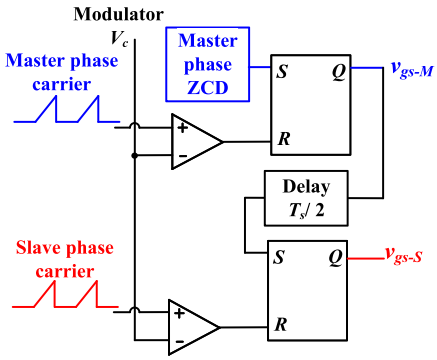

Fig. 3. CRM phase interleaving scheme based on open loop control.

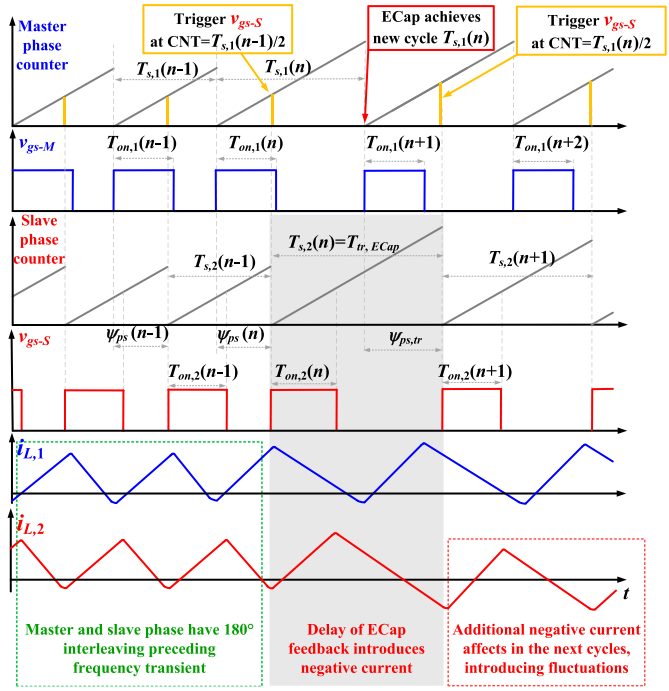

Fig. 4. Feedback delay effects on conventional open-loop interleaving method with ECap when switching cycle updates.

By comparing $Ph_{diff,1}$ with the target phase, if the phase difference exceeds half of the switching cycle ($T_s/2$), the on-time of the slave phase is decreased while the switching frequency is increased to reduce the phase difference.

PLL regulates the phase shift through feedback control [12], [13]. It dynamically adjusts the phase difference when T_s updates. However, the bandwidth of the phase detection circuit limits the phase control responses [11]. This may lead to oscillations at high switching frequency [15].

To enable phase interleaving at high switching frequency, open-loop approaches are investigated. The operating principle is illustrated in Fig. 3 [15], [16]. v_{gs-M} is triggered by the ZCD of master phase. v_{gs-S} is triggered by the signal generated by v_{gs-M} delayed by $T_s/2$, which resets the carrier of the slave phase. The on-times of the master and slave phases are identical.

Open-loop method regulates the phase shift without employing phase detection feedback. At steady state, the phase shift is fixed. However, if T_s varies, a periodically triggered signal (such as ZCD) needs to be captured by ECap to inform the controller of the latest T_s and generate the interleaved carrier for the slave phase [17], [18], [19], [20]. Hence, the delay and accuracy of ZCD and feedback of ECap affect the interleaving accuracy (see Fig. 4). The slave phase counter resets as v_{gs-S} rises. A transition cycle $T_{tr,ECap}$ occurs in the slave phase, $T_{tr,ECap} = [T_{s,1}(n) - T_{s,1}(n-1)]/2 + T_{s,1}(n)$. If $T_{s,1}(n) > T_{s,1}(n-1)$, $T_{tr,ECap} > T_{s,1}(n) > T_{s,1}(n-1)$. $T_{tr,ECap}$ is much larger than the CRM state T_s, making the inductor current of the slave phase fluctuate. Since the slave phase has no ZCD signal, the introduced negative current cannot be eliminated rapidly and keeps introducing the slave phase in the succeeding cycles. The magnitude of these fluctuations directly correlated to the disparity between cycles preceding and succeeding the transition. These effects are obvious when the switching frequency is low. In [21], the sensing delay is compensated with modified control model. In [22], a center-aligned carrier is introduced to generate real-time interleaved signals and avoid using ECap for a two-phase system. However, for general multiphase interleaving control, generation of carrier is hard to design.

For both closed-loop and open-loop interleaving, a significant challenge lies in how to precisely determine T_s of the master phase. Delays introduced by ECap and ZCD circuits jeopardize system performance. Predictive control offers a solution to reduce the sensing delay and simplify control loop [23], [24], [25], [26]. In [23], [24], deadbeat controller predicts the optimal duty ratio to achieve sinusoidal input current. In [25], T_s is estimated by the sensed input current. In [26], [27], current zero-crossing prediction is proposed to replace the ZCD circuit. However, these predictive control systems primarily concentrate on single-phase operation. Investigating predictive control for the interaction between master and slave phases is crucial for advancing interleaving performance.

In this article, we propose an optimized interleaving method for CRM totem pole rectifiers. It utilizes a T_s estimator based on zero-current prediction (ZCP). By employing ZCP, the time

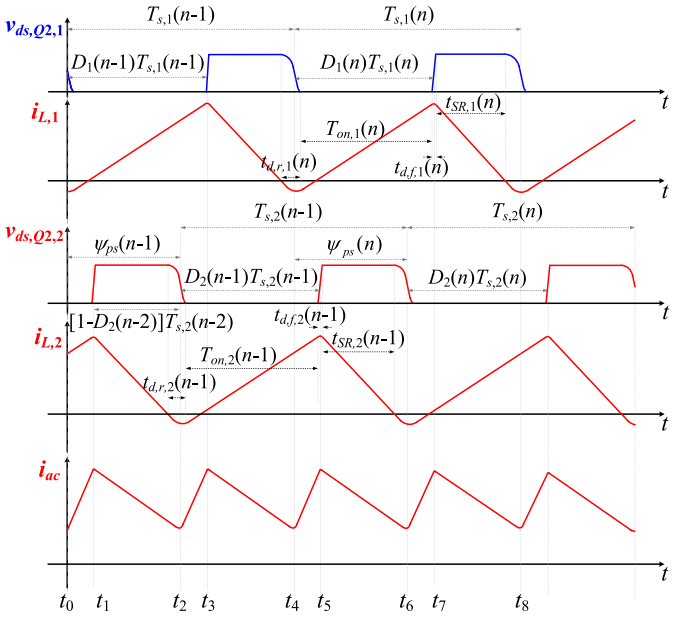

Fig. 5. Relationship among phase shift, duty ratio and input current ripple when $\psi_{ps}(n-1) < D_1(n-1)T_{s,1}(n-1)$.

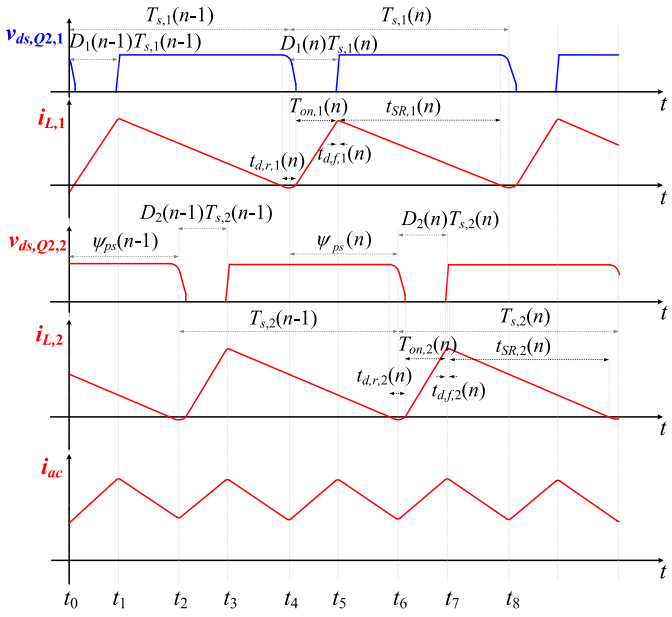

Fig. 6. Relationship among phase shift, duty ratio and input current ripple when $\psi_{ps}(n-1) \geq D_1(n-1)T_{s,1}(n-1)$.

delays associated with ECap can be eliminated, and the advantages can be better leveraged, With the predicted T_s, it can dynamically adjust the duty ratio of the slave phase to maintain an optimized ripple-cancellation through deadbeat control. Therefore, the proposed interleaving method achieves the dynamical phase management that is generally regarded as a feature of PLL in old wisdom. Since no closed-loop is employed in phase management, oscillations can be eliminated and the proposed method is naturally as stable as the open-loop solutions.

The remainder of this article is structured as follows. Section II outlines the derivation of the switching cycle estimator and introduces the proposed predictive interleaving phase shift control. Section III elaborates on the design considerations. Section IV presents the experimental verification and discussion. Finally, section V concludes this work.

II. Proposed Deadbeat Interleaving Control

A. Switching Cycle Estimator

As defined in Fig. 1, the input voltage is $v_{\rm ac}$ with line frequency ω_l. The input current is $i_{\rm ac}$. The dc-link voltage is $v_{\rm dc}$. The dc load current is $i_{\rm dc}$. $Q_{1,i}$, $Q_{2,i}$ are high frequency switches and $Q_{1,l}, Q_{2,l}$ are line frequency switches. In the following analysis, $i = 1$ for the master phase and $i = 2$ for the slave phase.

Figs. 5 and 6 illustrate the relationship among phase shift, equivalent duty ratio, and input current ripple in two adjacent cycles. Fig. 5 is the scenario when $\psi_{\rm ps}(n-1) < D_1(n-1)$ $T_{s,1}(n-1)$. Fig. 6 is the scenario when $\psi_{\rm ps}(n-1) \geq D_1$ $(n-1)T_{s,1}(n-1)$. Considering the influence of the resonant process, $D_i(n)$ is defined as the ratio of the time duration over which the inductor current rises from its valley to its peak, relative to the entirety of the switching cycle $T_{s,i}(n)$. The inductor current can be approximated as a triangular waveform in CRM. $\psi_{\rm ps}$ is the phase shift between the turn-on instant of master and slave phases.

For phase i, the critical impedance is $Z_{r,i}$ and the resonant angular frequency is $\omega_{r,i}$. $C_{t,i}$ is the time equivalent C_{oss} of high-frequency switches. It can be calculated from the method described in [28]. Equation (1) defines two variables: time-equivalent critical impedance $Z_{r,i}$ and resonant angular frequency $\omega_{r,i}$

$$Z_{r,i} = \sqrt{\frac{L_i}{2C_{t,i}}},\ \frac{1}{\omega_{r,i}} = \frac{L_i}{Z_{r,i}} = \sqrt{2C_{t,i}L_i}. \tag{1}$$

The turnon period of active switch is $T_{{\rm on},i}$. Phase i delivers the power of P_i, where $P_i = v_{\rm dc}i_{\rm dc}/\eta$. η is the conversion efficiency

$$T_{{\rm on},i}(n) = \frac{2Z_{r,i}L_iP_iv_{\rm ac}(n)/V^2_{\rm ac,rms} + L_i(v_{\rm dc} - v_{\rm ac}(n))}{v_{\rm ac}(n)Z_{r,i}.} \tag{2}$$

When phase i operates in normal power transfer scenario, $T^2_{{\rm on},i}(n) > -2K_iL_i^2/v^2_{\rm ac}(n)$, $K_i = Q_{{\rm tot},i}(2v_{\rm ac}(n) - v_{\rm dc})/L_i$. $Q_{{\rm tot},i}$ is the stored output charge, which can be derived from C_{oss} -$v_{\rm ds}$ curve in the datasheet, $Q_{{\rm tot},i} = \int_0^{v_{\rm dc}} C_{oss}(v_{\rm ds})v_{\rm ds}{\rm d}v_{\rm ds}$.

$t_{{\rm SR},i}$ represents the ON time of the synchronous rectifier switch (SR). It corresponds to $Q_{1,i}$ when $v_{\rm ac} > 0$ and $Q_{2,i}$ when $v_{\rm ac} < 0$. $k_{\rm po}$ is the disturbance damping coefficient with zero-current prediction control.

$$t_{{\rm SR},i}(n) = \frac{k_{\rm po}L_i\sqrt{\frac{v^2_{\rm ac}(n)}{L_i^2}T^2_{{\rm on},i}(n) + 2K_i}}{v_{\rm dc} - v_{\rm ac}(n).} \tag{3}$$

The deadband between the turning-off of active switch and the turning-on of SR switch is $t_{d,f,i}$. The process that the

inductor current ascends to its peak value spans approximately half of the deadtime interval

$$t_{d,f,i}(n) = \frac{\arctan\frac{1}{T_{on,i}(n)\omega_{r,i}} + \operatorname{arccot}\frac{Z_{r,i}\sqrt{\frac{v_{\rm ac}^2(n)}{L_i^2}T_{{\rm on},i}^2(n)+2K_i}}{v_{\rm dc}-v_{\rm ac}(n)}}{\omega_{r,i}} \tag{4}$$

The deadband between the turning-off of SR switch and the turning-on of active switch is $t_{d,r,i}$, which is adjusted with the zero-current prediction flag. The process that the inductor current decreases from 0 to its valley value spans $\pi/2/\omega_{r,i}$.

$$t_{d,r,i}(n) = \begin{cases} t_{{\rm SR}.i}(n)\dfrac{1-k_{\rm po}}{k_{\rm po}} + \dfrac{L_i\sqrt{-2K_i}}{v_{\rm ac}(n)} \\ \quad + \dfrac{\pi + \arctan\frac{Z_{r,i}\sqrt{-2K_i}}{v_{\rm ac}(n)}}{\omega_{r,i}}, & K_i \le 0 \\ \dfrac{\pi}{\omega_{r,i}} + t_{{\rm SR},i}(n)\dfrac{1-k_{\rm po}}{k_{\rm po}}, & K_i > 0. \end{cases} \tag{5}$$

Equations (2)–(5) show the calculation results of the four durations in the normal power transfer scenario. When phase i operates in nonpower transfer scenario, $T_{{\rm on},i}^2(n) \le -2K_iL_i^2/v_{\rm ac}^2(n)$, and $t_{{\rm SR},i}(n) = 0$. V_D is the voltage drop on the body diode

$$t_{d,f,i}(n) = \frac{\arctan\frac{1}{T_{{\rm on},i}(n)\omega_{r,i}}}{\omega_{r,i}} \tag{6}$$

$$t_{d,r,i}(n) = \frac{\arctan\frac{1}{T_{{\rm on},i}(n)\omega_{r,i}}}{\omega_{r,i}} + \frac{v_{\rm ac}}{v_{\rm ac}+V_D}T_{{\rm on},i}(n). \tag{7}$$

$T_{{\rm on},i}, t_{{\rm SR},i}, t_{d,r,i}, t_{d,f,i}$ are all derived in [26]. Equations (6) and (7) are the calculation results of the four durations in the nonpower transfer scenario

$$T_{s,i}(n) = T_{{\rm on},i}(n) + t_{{\rm SR},i}(n) + t_{d,f,i}(n) + t_{d,r,i}(n) \tag{8}$$

For phase i, the estimated switching cycle $T_{s,i}(n)$ can be estimated with (8) by summing these four durations. The equivalent duty ratio $D_i(n)$ in Figs. 5 and 6 is (9)

$$D_i(n) = \frac{T_{\rm on,i}(n) + t_{d,r,i}(n) - \pi/(2\omega_{r,i}) + t_{d,f,i}(n)/2}{T_{s,i}(n).} \tag{9}$$

B. Predictive Interleaving Phase Shift

When the switching frequency of master phase equals the switching frequency of slave phase, the phase shift is fixed, as shown in (10)

$$T_{s,2}(n-1) = T_{s,1}(n-1) \iff \psi_{\rm ps}(n) = \psi_{\rm ps}(n-1). \tag{10}$$

Considering the switching frequency transition, as shown in Figs. 5 and 6, the master phase changes before the slave phases. $T_{s,2}(n-2) = T_{s,1}(n-2)$, $T_{s,2}(n) = T_{s,1}(n) = T_{s,1}(n-1)$. $T_{s,2}(n-1)$ is determined by the transition process. The phase $\psi_{\rm ps}(n)$ varied from $\psi_{\rm ps}(n-1)$ follows:

$$\psi_{\rm ps}(n) = T_{s,2}(n-1) + \psi_{\rm ps}(n-1) - T_{s,1}(n-1). \tag{11}$$

On the other hand, the slave phase will introduce a transition cycle $T_{s,2}(n-1)$, and $T_{s,2}(n-1)$ is not equal to $T_{s,1}(n-1)$, resulting in a change in the phase shift between the master phase and the slave phase when the transition cycle is generated, as illustrated in (11).

C. Deadbeat Phase Shift Control for Cycle Transition

When $T_{s,1}$ changes from $T_{s,1}(n-1)$ to $T_{s,1}(n)$, it introduces a transition cycle T_{tr} as $T_{s,2}(n-1)$ and transition phase $\psi_{ps,tr}$ in the slave phase, as shown in Figs. 5 and 6. In such cases, the duty ratio of the slave phase $D_2(n-1)$ must be adjusted to preserve the phase difference.

To maintain the phase shift between master phase and slave phases, the transient caused by $T_{s,2}(n-1)$ on $i_{\rm ac}$ must be null, implying $i_{\rm ac}(t_2) - i_{\rm ac}(t_6) = 0$. Pretransient, $i_{\rm ac}(t_2)$ equals $i_{\rm ac}(t_0)$. Posttransient, for deadbeat control, $i_{\rm ac}(t_8)$ equals $i_{\rm ac}(t_6)$. Hence, $i_{\rm ac}(t_8)$ equals $i_{\rm ac}(t_0)$. Otherwise, the phase shift gradually increases or decreases, leading to low-frequency oscillations in $i_{\rm ac}$ and degradation of the input current iTHD. Beyond t_8, the phase remains at 180^o. Therefore, to sustain the phase shift when updating switching cycles, the duty ratio of the slave phase should update correspondingly. The derivation of $i_{\rm ac}(t_8)$ is in the Appendix A.

With $i_{\rm ac}(t_8) - i_{\rm ac}(t_0) = 0$, $D_2(n-1)$ during $T_{s,2}(n-1)$ can be derived in two cases. When $\psi_{\rm ps}(n-1) < D_1(n-1)$ $T_{s,1}(n-1)$, as shown in Fig. 5

$$\begin{aligned} D_2(n-1) = {} & 1 + \frac{(1-D_2(n-2))T_{s,2}(n-2)}{T_{s,2}(n-1)} \\ & + \frac{[(1-D_1(n))T_{s,1}(n) + (1-D_1(n-1))T_{s,1}(n-1)]L_2}{L_1T_{s,2}(n-1)} \\ & - \frac{(L_1+L_2)(T_{s,1}(n)+T_{s,1}(n-1))v_{\rm ac}(n)}{L_1T_{s,2}(n-1)v_{\rm dc}.} \end{aligned} \tag{12}$$

When $\psi_{\rm ps}(n-1) \ge D_1(n-1)T_{s,1}(n-1)$, as shown in Fig. 6,

$$\begin{aligned} D_2(n-1) = {} & \frac{[L_1 + L_2(1-D_1(n))]T_{s,1}(n)}{L_1T_{s,2}(n-1)} \\ & - \frac{(L_1+L_2)(T_{s,1}(n)+T_{s,1}(n-1))v_{ac}(n)}{L_1T_{s,2}(n-1)v_{dc}} - \frac{D_2(n)T_{s,2}(n)}{T_{s,2}(n-1)} \\ & + \frac{((L_1+(1-D_1(n-1))L_2)T_{s,1}(n-1)}{L_1T_{s,2}(n-1)} \end{aligned} \tag{13}$$

Equations (12) and (13) show the calculation results of the duty cycle in the transition cycle for achieving $i_{\rm ac}(t_8) = i_{\rm ac}(t_0)$. In our proposed interleaving method, the phase is dynamically adjusted using predictive control, resulting in deadbeat performance.

III. Design Considerations

A. Phase Optimization in Switching Cycle Transition

Fig. 7 illustrates the operating principle of the proposed phase optimization method during switching cycle transition when $v_{\rm ac} > 0$. The master phase triggers $v_{{\rm gs}-S}$ at the midpoint of switching cycle. The slave phase reset the carrier (counter

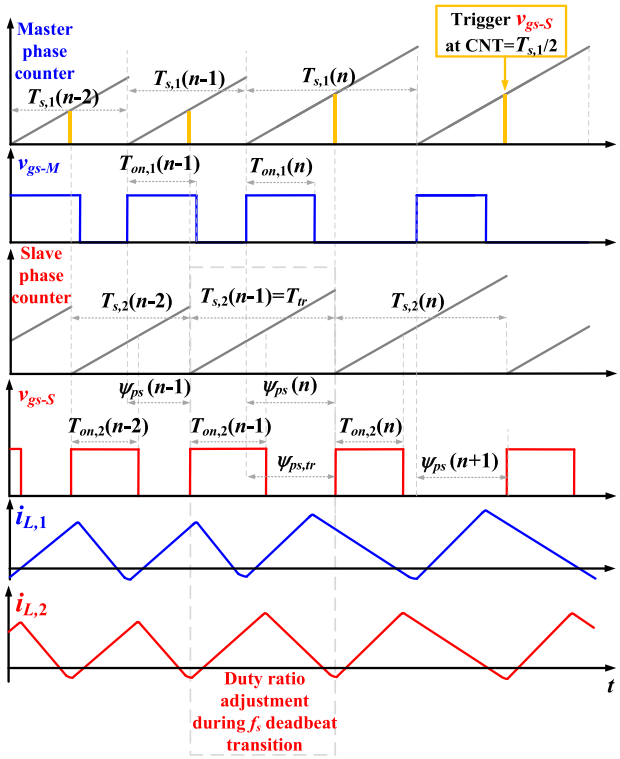

Fig. 7. Optimized phase interleaving mechanism when switching cycle updates.

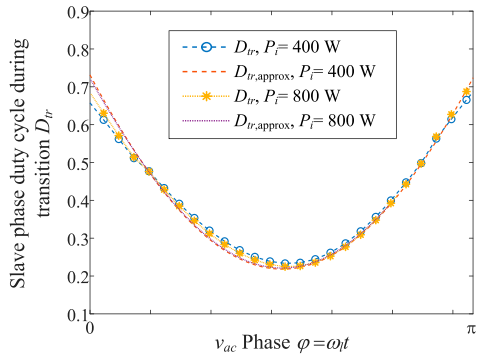

Fig. 8. Comparison between $D_{\rm tr}$ and $D_{\rm tr,approx}$ during the switching cycle transition.

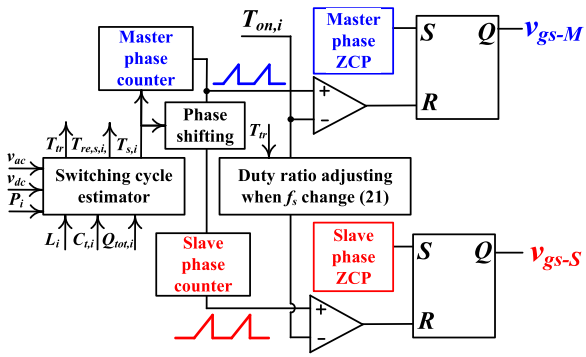

Fig. 9. Interleaving mechanism with switching cycle estimator.

value) when $v_{\rm gs-S}$ rises. Therefore, at steady state, the master and the slave phases exhibit 180^o phase shift. This avoids the failure induced by the counter-compare mechanism [29].

During the switching frequency transition, a transient switching cycle $T_{\rm tr}$ with a transient phase $\psi_{\rm ps,tr}$ exists between the prior switching cycle $T_{s,2}(n-2)$ and the new switching cycle $T_{s,2}(n)$ in the slave phase. With the feed-forward switching cycle estimator, the switching cycle and duty ratio between master and slave phases have $T_{s,2}(n-2)=T_{s,1}(n-2)=T_{s,1}(n-1)$, $T_{s,2}(n)=T_{s,1}(n)$, $D_2(n-2)=D_1(n-2)=D_1(n-1)$, $D_2(n)=D_1(n)$. With the interleaved signal generation mechanism, $\psi_{\rm ps,tr}$ and $T_{\rm tr}$ can be derived as follows:

$$T_{s,2}(n-1)=T_{\rm tr}=\frac{T_{s,1}(n-1)}{2}+\frac{T_{s,1}(n)}{2} \tag{14}$$

$$\psi_{\rm ps}(n-1)=\frac{1}{2}T_{s,1}(n-1),\ \psi_{\rm ps,tr}=\frac{1}{2}T_{s,1}(n)$$

$$D_{\rm tr}=D_2(n-1). \tag{15}$$

The transient duty ratio at $T_{s,2}(n-1)$ can be derived with (15). This ratio is calculable through the multiplication of variables $v_{\rm ac}$, $v_{\rm dc}$, $T_{s,1}(n-1)$, and $T_{s,2}(n)$. Detailed derivation is provided in the Appendix B. Hence, the transient slave phase on-time $T_{\rm on,2}(n-1)$ can be derived as follows:

$$T_{\rm on,2}(n-1)=D_{\rm tr}T_{\rm tr}+\frac{\pi}{2\omega_{r,2}}-\frac{t_{d,f,2}(n-1)}{2}-t_{d,r,2}(n-1). \tag{16}$$

Since the magnitude difference between the voltage used in the operation and the switching cycle is too large, variable overflow may occur during the calculation. To optimize the calculation process, the approximation $D_{\rm tr,approx}$ is used

$$D_{\rm tr,approx}=[D_1(n-1)+D_1(n)]/2. \tag{17}$$

Fig. 8 compares the differences between the precisely calculated transient duty ratio ($D_{\rm tr}$) and the approximate transient duty ratio ($D_{\rm tr,approx}$), demonstrating the feasibility of using $D_{\rm tr,approx}$ instead of $D_{\rm tr}$. $D_{\rm tr,approx}$ approximates $D_{\rm tr}$ with higher accuracy at heavy load. The heavier the load is, the more accurate the approximation becomes. To speed up the calculation during the frequency change transition, the formula (17) is used to approximate the slave phase duty ratio during the frequency change transition.

B. Control System Implementation

Fig. 9 depicts the pulse width signal generating mechanism of the proposed method. The driving signal for the active switch in the master phase is $v_{\rm gs-M}$, corresponding to $Q_{2,1}$ and $Q_{1,1}$ during the positive and negative half line periods, respectively. Similarly, the driving signal for the active switch in the slave phase is $v_{\rm gs-S}$, corresponding to $Q_{2,2}$ and $Q_{1,2}$ during the positive and negative half line periods, respectively. Both $v_{\rm gs-M}$ and $v_{\rm gs-S}$ are triggered by their respective ZCP flags.

The cycle estimator predicts the next $T_{s,1}$ based on given circuit parameters, such as $v_{\rm ac}$, $v_{\rm dc}$, and $i_{\rm dc}$. The carriers of

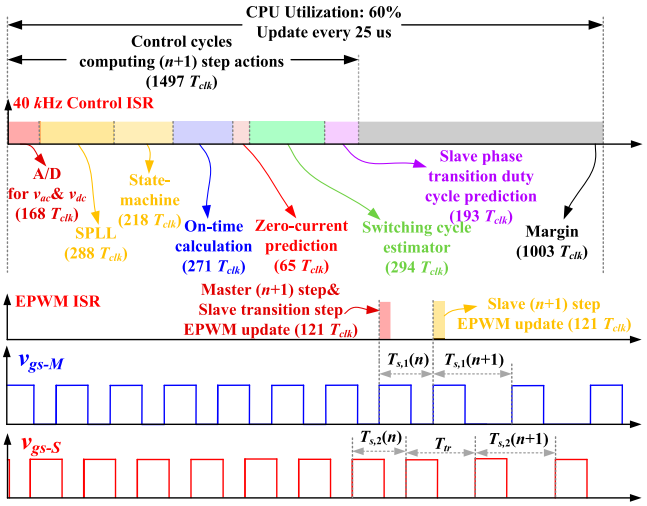

Fig. 10. Control clocks of the proposed interleaving method.

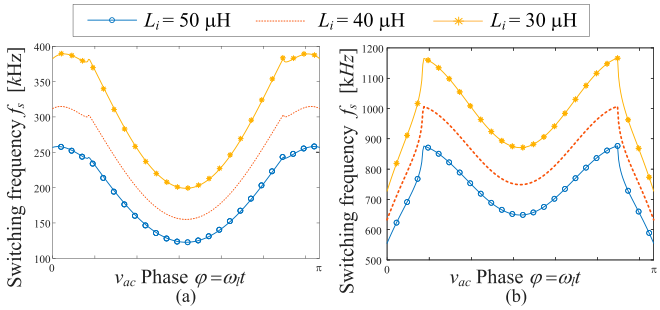

Fig. 11. Comparison of switching frequency variation range with different inductances at: (a) $P_i = 800$ W; (b) $P_i = 50$ W when $v_{\rm dc} = 400$V, $v_{\rm ac} = 311\sin(\omega_l t)$V.

the master and slave phases are interleaved directly with the estimated switching cycle. If the next switching cycle is not matched with the current switching cycle, a transient switching cycle $T_{\rm tr}$ is generated. To achieve deadbeat interleaving during switching cycle transitions, the duty ratio of the slave phase is alternated using (12) and (13).

The proposed method mitigates control delay through feed-forward prediction, capitalizing on the inherently low-bandwidth nature of the PFC application. This allows for the preemptive computation of the input current prior to the upcoming switching event. Specifically, within our approach, the determination of the switching cycle is expedited by one full control cycle, thereby intrinsically offsetting the latency inherent to the control process.

Using a 100 MHz DSP (TMS320F280049) as an example, the control cycles are shown in Fig. 10. The total calculation algorithms execute in 1497 $T_{\rm clk}$ ($T_{\rm clk}$ is the DSP clocking cycle). The 40 kHz control interrupt service routine (ISR) runs with 60% CPU utilization. The EPWM parameter updates in EPWM ISR. During the final switching cycle of the EPWM ISR utilizing step n switching parameters, the step $n+1$ parameters are updated to the shadow register associated with the master phase, while the transition parameters are concurrently updated to the slave phase's shadow register. These updated parameters are then loaded into the operational registers at the onset of the subsequent switching cycle. Upon the initial EPWM ISR execution for step $n+1$, the corresponding parameters are updated to the slave phase's shadow register. The EPWM update process consumes 121 $T_{\rm clk}$ and remains uninterrupted when $f_s < 820$ kHz. Consequently, the proposed method is viable with cost-effective microcontrollers as shown in Fig. 10.

Phase shedding is widely used in interleaved systems to improve the performance at light load. The interleaving algorithm should work above half load per-phase. For instance, a 1600 W interleaved CRM totem-pole PFC may work in phase shedding mode below 800 W. When the load exceeds 800 W, both master and slave phases are enabled. Therefore, performance of the interleaving algorithm above 400 W (1/4 full load) is important. Since the switching frequency decreases as the load rate increases in CRM state, the interleaving control performance at low switching frequency is more attractive than that in high switching frequency.

In the proposed predictive control, the switching cycle is achieved with estimator instead of peripheral circuit. The switching cycle variation can be predicted. The slave phase can be dynamically controlled during the switching cycle transition. Hence, most high-speed sensing circuits can be eliminated. On the other hand, as described in the introduction, at high switching frequency, the time delay due to the ECap feedback also decreases. Compared with open-loop method, the proposed method can be implemented on MHz prototype without additional hardware cost and has better performance at several hundred kHz switching frequency case.

C. Switching Frequency Range Optimization

The switching frequency of the CRM totem-pole power factor correction converter relates to the inductance and load. A larger inductance results in a lower switching frequency. A lower switching frequency reduces magnetic and copper losses. However, if the switching frequency is excessively low, both $v_{\rm ac}$ and $v_{\rm dc}$ fluctuate during the switching cycle, leading to control errors. Furthermore, under a digital control system, an excessively low switching frequency increases the execution delay of input current control and diminishes the effectiveness of PFC [30]. Conversely, if the switching frequency is too high, it will induce a significant skin effect and escalate the copper and magnetic losses of the boost inductor. Therefore, the switching frequency range and inductance must be optimally designed.

In the proposed controller, the control interruption frequency is set at $f_{\rm con} = 40$ kHz. To achieve a more effective input current control, the switching frequency needs to satisfy $f_s \geq 4f_{\rm con} = 160$ kHz.

$T_{s,i}$ is affected by six parts: L_i, $C_{t,i}$, $Q_{{\rm tot},i}$, $v_{\rm ac}$, $v_{\rm dc}$, P_i via (8). To achieve a stable phase interleaving, $T_{s,i}$ should be close to each other. Therefore, inductor consistency should be guaranteed, $L_1 \approx L_2$. In Fig. 11, $v_{\rm dc} = 400$V, $v_{\rm ac} = 311\sin(\omega_l t)$V. $C_{t,i} = 450$ pF, $Q_{{\rm tot},i} = 145$ nC.

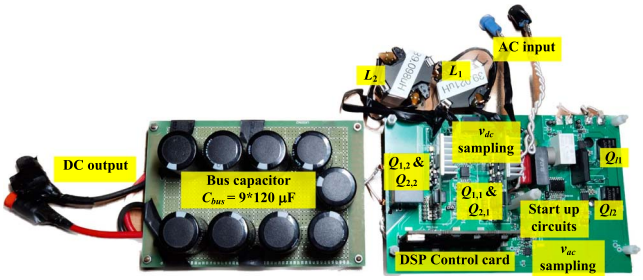

Fig. 12. Prototype of designed two-phase interleaved totem pole PFC converter.

TABLE I
DESIGNED PARAMETERS

Symbol	Parameter	Value
L_1, L_2	Boost inductor	39.021 μH, 39.098 μH
$Q_{1,1}, Q_{2,1}$, $Q_{1,2}, Q_{2,2}$	High frequency switches	LMG3410R070
$Q_{1,l}, Q_{2,l}$	Line frequency switches	IPW60R180P7
v_{dc}	DC-link voltage	400 V
v_{ac}	AC input voltage	220 $V_{\rm rms}$
C_{bus}	DC capacitance	1080 μF

Fig. 11(a) illustrates the switching frequency range for a single-phase 800 W converter with various inductances. It is evident that when $L_i \leq 40$ μH, the minimum switching frequency exceeds 160 kHz, meeting the required switching frequency range. Fig. 11(b) depicts the switching frequency range for a single-phase 50 W converter with different inductances. It can be observed that when $L_i \geq 40$ μH, the peak switching frequency under light load reaches approximately 1 MHz. Smaller inductance leads to higher peak switching frequency. Since circulating power contributes a significant portion at light load, higher switching frequencies result in increased magnetic and conduction losses, which affects the system efficiency. Therefore, the optimal L_i should be around 40 μH.

IV. EXPERIMENTAL RESULTS

To validate the concept, a 1.6 kW GaN-based two-phase interleaved totem pole PFC prototype is designed, as illustrated in Fig. 12. The designed parameters are outlined in Table I. The controller utilized is TMS320F280049 with 100 MHz clock frequency. The switching frequency range of the prototype spans from 160 to 950 kHz. High-speed GaN devices LMG3410R070 with integrated drivers are employed as the high-speed switches, while super-junction MOSFETs, IPW60R180P7, are selected as the line frequency switches.

The dc bus capacitor employs an electrolytic capacitor array to suppress the overall equivalent series resistance (ESR) of the bus capacitor, thereby minimizing the capacitor power loss. Compared with single-phase configurations, the interleaved structure reduces input and output current ripples, resulting in a higher power level with the same bus capacitance.

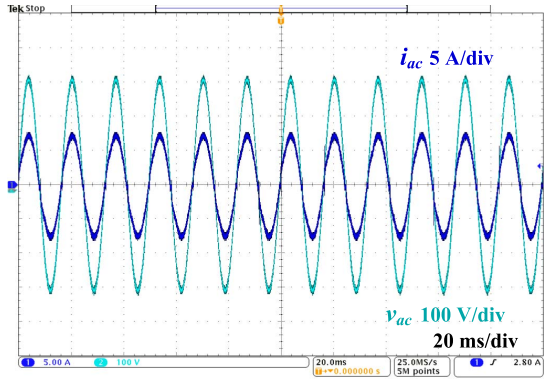

Fig. 13. Input voltage and current waveforms at 1.2 kW.

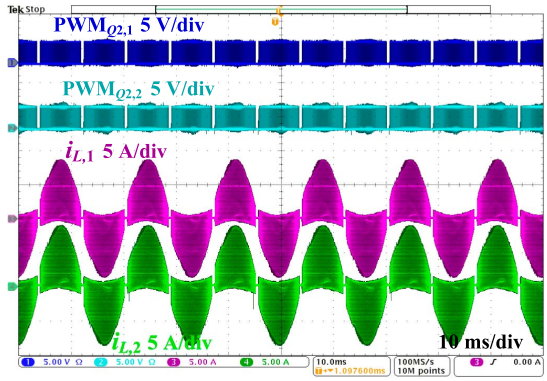

Fig. 14. Inductor current waveforms at 1.2 kW (grid cycle scale).

The prototype incorporates a starting circuit that precharges the bus capacitor before switching operations, effectively mitigating surge currents during the boost circuit's starting process. The boost inductors L_1 and L_2 are wound using RM14 cores with DMR51W material from DMEG, suitable for operation below 3 MHz.

Figs. 13 and 14 show the steady-state operating waveforms of the designed prototype at 1.2 kW. The waveforms of $v_{\rm ac}$ and $i_{\rm ac}$ are captured in Fig. 13. As shown, $v_{\rm ac}$ and $i_{\rm ac}$ are in phase, exhibiting a unit power factor.

Figs. 14 and 15 show the interleaved inductor currents and the corresponding drive signal. In Fig. 14, at line frequency scale, $i_{L,1}$ and $i_{L,2}$ have smooth envelopes. The slave and the master phases exhibit currents with identical amplitudes. This indicates an evenly distributed power between phases.

In Fig. 15, at switching scale, $i_{L,1}$ and $i_{L,2}$ exhibit triangular waveforms, achieving a 180^o phase shift. Through the proposed control, a precise interleaving is attained. $\rm PWM_{Q2,1}$ and $\rm PWM_{Q2,2}$ rises correspondingly when $i_{L,1}$ and $i_{L,2}$ cross zero, respectively. Notably, the proposed interleaving method is compatible with zero-current prediction, thereby avoiding excessive computational burden.

Fig. 16 records the inductor current waveforms under fluctuating switching frequencies when utilizing the conventional open-loop interleaving method. As the switching cycle shifts

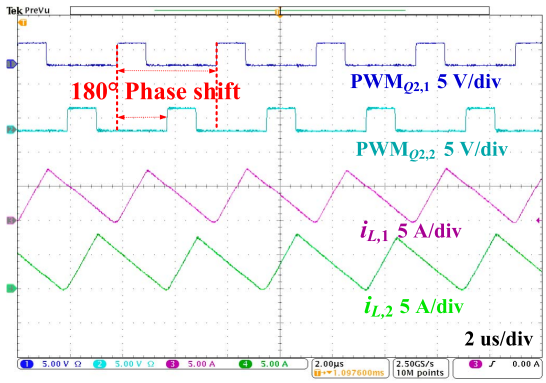

Fig. 15. Inductor current waveforms at 1.2 kW (switching cycle scale).

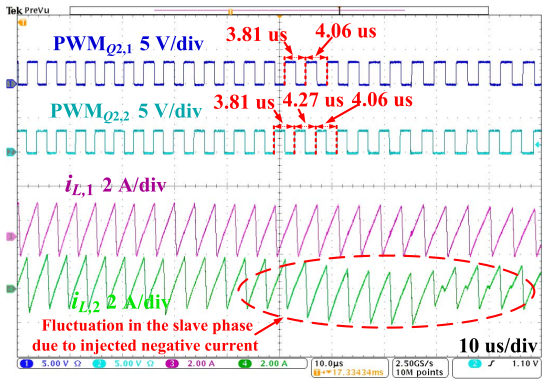

Fig. 16. Inductor current waveforms when switching frequency changes (conventional open-loop interleaving method).

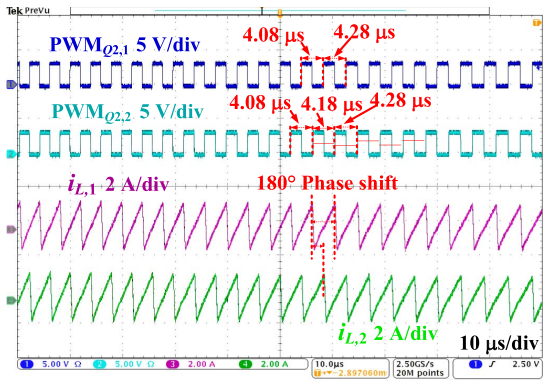

Fig. 17. Inductor current waveforms when switching frequency changes (proposed method).

from 3.81 to 4.06 μs, an extra switching cycle at 4.27 μs is superimposed on the slave phase, characterized by the injection of a negative current. In the followed cycles, this negative current has an inherent disruptive effect on the slave phase, manifesting as fluctuations in the current waveform. Meanwhile, the master phase preserves its CRM state.

Fig. 17 records the inductor current waveforms under fluctuating switching frequencies when utilizing the proposed interleaving method. The master phase switching cycle shifts

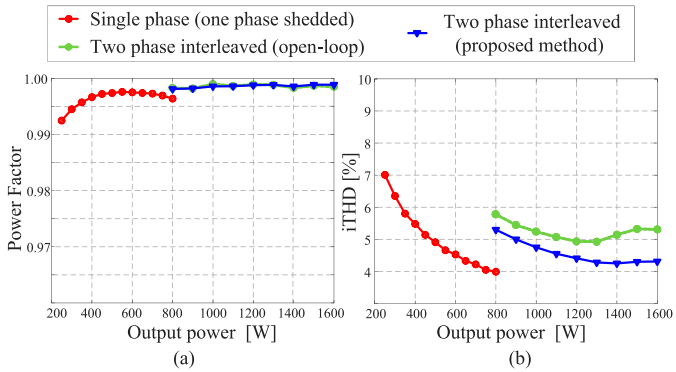

Fig. 18. Test results: (a) power factor; (b) iTHD.

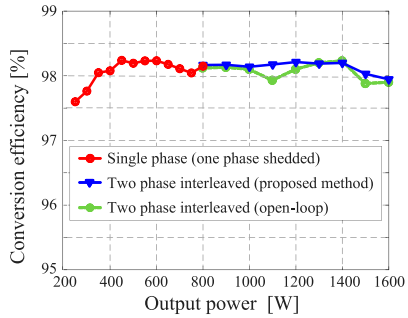

Fig. 19. Measured efficiency.

from 4.08 to 4.28 μs. During the frequency transition, the slave phase injects an additional switching cycle 4.18 μs, and $4.08/2 + 4.28/2 = 4.18$. In the injected cycle, the master phase current and the slave phase current have 180^o phase shifts.

Fig. 18 displays the power factor and input current THD of the tested prototype. As shown, the proposed interleaving method demonstrates better THD performance compared with the conventional open-loop interleaving. In both methods, the power factor is above 0.995. The proposed method enhances the interleaving PFC performance, with the prototype achieving a power factor higher than 0.995 from 20% load to full load. At 1.6 kW, the input current THD is measured at 4.31%.

In Fig. 19, the efficiency of the tested prototype is recorded. The blue curve represents the efficiency using proposed predictive interleaving method. The green curve is the results under conventional open-loop interleaving method. The peak efficiency reaches 98.24%. Efficiency of the proposed method and conventional open-loop interleaving are close to each other.

In Fig. 19, the conversion efficiency of the test prototype is depicted. The blue curve represents the measured efficiency using proposed predictive interleaving control method. The green curve is the results under conventional open-loop interleaving method. The peak efficiency reaches 98.24%. Efficiency of the proposed method and conventional open-loop interleaving are close to each other. At light load, the dominant power loss is magnetic loss. Switching to single-phase mode enhances the system efficiency. As the load increases, conduction loss dominates. Switching to interleaving mode is beneficial to

TABLE II
PERFORMANCE COMPARISON ON INTERLEAVING CONTROL ALGORITHMS

Reference	[6]	[12]	[14]	[17]	Proposed
Power rating	1600 W	200 W	1000 W	1000 W	1600 W
Conduction mode	CCM	CRM	CRM	CRM	CRM
Soft switching	ZVS	ZVS	ZVS/ZCS	ZVS	ZVS/ZCS
Switching Frequency	200 kHz fixed	300 kHz−900 kHz	100 kHz−550 kHz	80 kHz−140 kHz	160 kHz−950 kHz
High-speed current sensing	Master + slave current sensing	Master + slave ZCD	Master + Slave ZCD	Master ZCD	N/A
High-speed voltage Sensing	N/A	N/A	N/A	Master + slave ZVD	N/A
Interleaving method	Fix switching frequency	Closed-loop PLL	Closed-loop PLL	Open-loop	Feedforward predictive
Controller	DSP	DSP+FPGA	DSP	DSP	DSP
Peak efficiency	98.21%	96.9%	97.85%	97.83%	98.24%

system performance. However, at heavy load, the conduction loss of the line frequency switch ($Q_{1,l}$, $Q_{2,l}$) surpasses that at light load. Despite the power processed by the master and slave phases being equivalent to the single-phase power at light load, the ratio of total loss to input power remains high at heavy load. Consequently, peak efficiency is achieved at single-phase mode.

A comparison among the proposed and some recently reported interleaving method is made and summarized in Table II. The proposed method is compatible with soft switching performance, wide switching range that is from hundreds kHz to MHz, low-cost controller without high-speed current/voltage sensing, and good peak efficiency.

V. CONCLUSION

In this article, we present a deadbeat predictive interleaving method for totem-pole PFC rectifiers. Through the switching cycle estimator, the switching cycles of the master and slave phases are obtained, enabling a direct generation of interleaved carrier signals. By analyzing the multiphase interleaved input current ripple, the slave phase duty ratio can be determined during frequency transition to dynamically control the master-slave phase difference. The master and slave phases are triggered by their respective zero-current prediction flags. The switching cycle estimator and the zero current prediction method are compatible, eliminating the need for high-speed detection circuits and current sampling units, thereby reducing the computational burden.

A GaN-based 1.6 kW totem-pole PFC converter prototype is designed as the proof of concept. The prototype achieves two-phase interleaving of the master and the slave phases within a switching frequency range from 160 to 950 kHz. It attains a power factor exceeding 0.995 from 20% load to full load. The peak efficiency reaches 98.24%, and at rated power, the THD of the input current is measured at 4.31%.

APPENDIX A
DERIVATION OF CURRENT RIPPLES

In Figs. 5 and 6, the slope of $i_{\rm ac}$ is m_i during instant $t_{i-1}-t_i$, $i=1,2,...,8$. Fig. 5 is the scenario when $\psi_{\rm ps}(n-1) < D_1(n-1)T_{s,1}(n-1)$. The switching instant current of $i_{\rm ac}$ can be derived

$$\begin{aligned}
i_{\rm ac}(t_1) &= m_1\left[\psi_{\rm ps}(n-1) + D_2(n-2)T_{s,2}(n-2)\right.\\
&\quad \left. -T_{s,2}(n-2)\right] + i_{\rm ac}(t_0)\\
i_{\rm ac}(t_2) &= m_2\left[1-D_2(n-2)\right]T_{s,2}(n-2) + i_{\rm ac}(t_1)\\
i_{\rm ac}(t_3) &= m_3\left[D_1(n-1)T_{s,1}(n-1) - \psi_{\rm ps}(n-1)\right] + i_{\rm ac}(t_2)\\
i_{\rm ac}(t_4) &= m_4\left[1-D_1(n-1)\right]T_{s,1}(n-1) + i_{\rm ac}(t_3)\\
i_{\rm ac}(t_5) &= m_5\left[\psi_{\rm ps}(n) + D_2(n-1)T_{s,2}(n-1)\right.\\
&\quad \left. - T_{s,2}(n-1)\right] + i_{\rm ac}(t_4)\\
i_{\rm ac}(t_6) &= m_6\left[1-D_2(n-1)\right]T_{s,2}(n-1) + i_{\rm ac}(t_5)\\
i_{\rm ac}(t_7) &= m_7\left[D_1(n)T_{s,1}(n) - \psi_{\rm ps}(n)\right] + i_{\rm ac}(t_6)\\
i_{\rm ac}(t_8) &= m_8\left[1-D_1(n)\right]T_{s,1}(n) + i_{\rm ac}(t_7).
\end{aligned}$$

The slope is as follows:

$$\begin{aligned}
m_1 &= \frac{v_{\rm ac}}{L_1}+\frac{v_{\rm ac}}{L_2},\ m_2 = \frac{v_{\rm ac}}{L_1}-\frac{v_{\rm dc}-v_{\rm ac}}{L_2}\\
m_3 &= \frac{v_{\rm ac}}{L_1}+\frac{v_{\rm ac}}{L_2},\ m_4 = -\frac{v_{\rm dc}-v_{\rm ac}}{L_1}+\frac{v_{\rm ac}}{L_2}\\
m_5 &= m_1,\ m_6 = m_2,\ m_7 = m_3,\ m_8 = m_4.
\end{aligned} \tag{19}$$

Fig. 6 is the scenario when $\psi_{\rm ps}(n-1) \geq D_1(n-1)T_{s,1}(n-1)$. The switching instant current of $i_{\rm ac}$ can be derived.

$$\begin{aligned}
i_{\rm ac}(t_1) &= m_1 D_1(n-1)T_{s,1}(n-1) + i_{\rm ac}(t_0)\\
i_{\rm ac}(t_2) &= m_2\left[\psi_{\rm ps}(n-1) - D_1(n-1)T_{s,1}(n-1)\right] + i_{\rm ac}(t_1)\\
i_{\rm ac}(t_3) &= m_3 D_2(n-1)T_{s,2}(n-1) + i_{\rm ac}(t_2)\\
i_{\rm ac}(t_4) &= m_4\left[T_{s,1}(n-1) - \psi_{\rm ps}(n-1)\right.\\
&\quad \left. -D_2(n-1)T_{s,2}(n-1)\right] + i_{\rm ac}(t_3)\\
i_{\rm ac}(t_5) &= m_5 D_1(n)T_{s,1}(n) + i_{\rm ac}(t_4)\\
i_{\rm ac}(t_6) &= m_6\left[\psi_{\rm ps}(n) - D_1(n)T_{s,1}(n)\right] + i_{\rm ac}(t_5)\\
i_{\rm ac}(t_7) &= m_7 D_2(n)T_{s,2}(n) + i_{\rm ac}(t_6)\\
i_{\rm ac}(t_8) &= m_8\left[T_{s,1}(n) - \psi_{\rm ps}(n) - D_2(n)T_{s,2}(n)\right] + i_{\rm ac}(t_7).
\end{aligned} \tag{20}$$

The slope is as follows:

$$m_1 = \frac{v_{\rm ac}}{L_1} - \frac{v_{\rm dc}-v_{\rm ac}}{L_2},\ m_2 = -\frac{v_{\rm dc}-v_{\rm ac}}{L_1} - \frac{v_{\rm dc}-v_{\rm ac}}{L_2}$$
$$m_3 = -\frac{v_{dc}-v_{\rm ac}}{L_1} + \frac{v_{\rm ac}}{L_2},\ m_4 = -\frac{v_{\rm dc}-v_{\rm ac}}{L_1} - \frac{v_{\rm dc}-v_{\rm ac}}{L_2}$$
$$m_5 = m_1,\ m_6 = m_2,\ m_7 = m_3,\ m_8 = m_4. \tag{21}$$

Appendix B
Transition Duty Cycle Derivation

The transient duty cycle at $T_{s,2}(n-1)$ can be derived with (12), (13), and (14). When $\psi_{\rm ps}(n-1) < D_1(n-1)T_{s,1}(n-1)$, or $D_1(n-1) > 0.5$ for two phase interleaving

$$\begin{aligned} D_{\rm tr} = D_2(n-1) = \frac{1}{T_{\rm tr}v_{\rm dc}}\big[&-2T_{s,1}(n)v_{\rm ac}(n) + T_{s,1}(n)v_{\rm dc} \\ &- 2T_{s,1}(n-1)v_{\rm ac}(n) + T_{tr}v_{\rm dc} + 2T_{s,1}(n-1)v_{\rm dc} \\ &- D_1(n)T_{s,1}(n)v_{\rm dc} - 2D_1(n-1)T_{s,1}(n-1)v_{\rm dc}\big]. \end{aligned} \tag{22}$$

When $\psi_{\rm ps}(n-1) \geq D_1(n-1)T_{s,1}(n-1)$, or $D_1(n-1) \leq 0.5$ for two phase interleaving

$$\begin{aligned} D_{tr} = D_2(n-1) = \frac{1}{T_{tr}v_{dc}}\big[&-4T_{s,1}(n-1)v_{ac}(n) \\ &+ 2T_{s,1}(n-1)v_{dc} - 2D_1(n)T_{s,1}(n)v_{dc} \\ &- D_1(n-1)T_{s,1}(n-1)v_{dc} + 2T_{s,1}(n)v_{dc}\big] \end{aligned} \tag{23}$$

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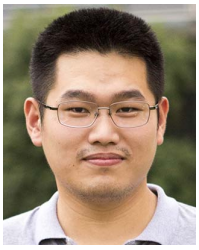

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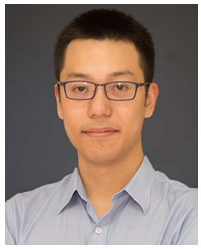

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