SI100B – Electrical Engineering, 2023 Spring

Homework #2

Notes:

1. The submission deadline is **2023-04-23 23:59:59**. Late assignments will incur a 10-point deduction per day.
2. You must work on this homework individually. Any plagiarism will result in a zero grade for this assignment.
3. You can either type your answers in a word document or handwrite them and scan them as a pdf file.
4. The simulation files that support your analysis should be named according to the problems. You can zip them together with your solutions into a single file.

Problem 1. CMOS logic gate (40 points)

A CMOS logic gate consists of complementary and symmetrical pairs of p-type and n-type MOSFETs that implement a desired logic function. In this problem, you will apply your knowledge of CMOS logic gate design and analysis. You will also learn how to determine the logic function from a given CMOS transistor network.

1) Write the truth table for the CMOS transistor network shown in **Fig. 1-1**. **(10 points)**

2) What is the logic function realized by the CMOS transistor network in Fig. 1-1? Express it in Boolean algebra with a simplified form. **(10 points)**

3) Construct this gate using the basic CMOS logic units, such as NOT, AND, OR. Draw the schematic diagram of your design. **(10 points)**

4) Use MATLAB to simulate your design and show an example result to verify your solution. **(10 points)**

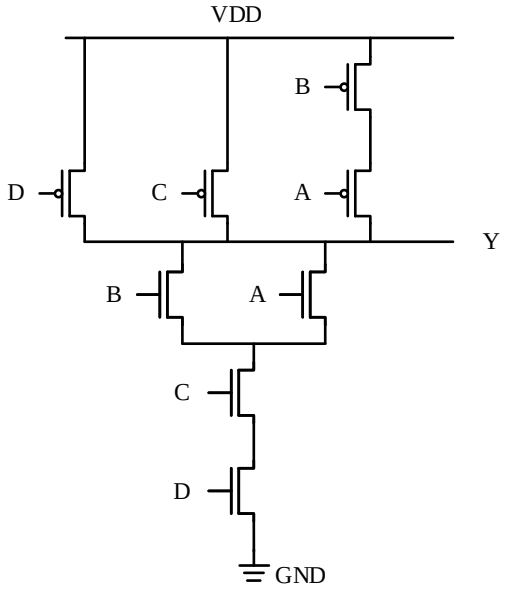

Fig. 1-1

(Hint: You can use the truth table to help you find the logic function if it is not obvious from the CMOS transistor network.)

Problem 2. Combinational logic circuit (30 points)

A combinational logic circuit is a circuit that performs a logic operation based on the input values. Karnaugh maps (K-maps) is a graphical approach to simplifying logic circuits by finding the minimum SOP (sum of product) or POS (product of sum) form for a logic function. NAND and NOR gates are universal gates that can implement any logic function using only one type of gate. For this problem: use K-maps to find the minimum SOP or POS form for a given logic function and then implement it using given gates.

1) Find the minimum SOP form for the logic function: $\mathrm{Z} = (\mathrm{A} + \mathrm{B} + \mathrm{C})(\bar{A} + \bar{B} + \bar{C})$, and implement it with only NAND gates (Draw the circuit diagram composed of NAND gates). **(10 points)**

2) Find the minimum POS form for the logic function: $\mathrm{Z} = \bar{A} + \mathrm{B}\bar{C} + \bar{B}C$, and implement it with only NOR gates (Draw the circuit diagram composed of NOR gates). **(10 points)**

3) Find the minimum SOP form for the logic function: $\mathrm{Z} = \bar{A}\mathrm{B} + \bar{B}C + C\bar{D} + \bar{D}A$ and implement it with AND, OR and NOT gates (Draw the circuit diagram composed of AND, OR and NOT gates). **(10 points)**

(Hint: Refer to the Figure 7.20, Figure 7.21, Example 7.14 and Example 7.15 from reference book EEPA)

Problem 3. Sequential logic circuit (30 points)

1) Given the input waveforms shown in the following figure, sketch the waveform of output Q and $\bar{Q}$ of an SR latch (Considering the initial value of Q is high). (**Note: If the output is uncertain, use a dotted line to indicate it.**) **(15 points)**

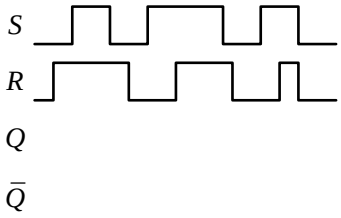

Fig. 3-1

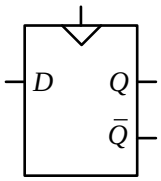

Fig. 3-2

2) In the class, we have learned that JK flip-flop is the most versatile. Design a circuit to convert D flip-flop to JK flip-flop with the AND, OR and NOT gates. (The symbol of D flip-flop is shown in **Fig. 3-2.**) **(15 points)**

(Hint: For D flip-flop, $Q^{n+1} = D$, for JK flipflop, $Q^{n+1} = J\overline{Q^n} + \bar{K}Q^n$)