SI100B – Electrical Engineering, 2023 Spring

Homework #3

Notes:

1. The submission deadline is **2023-05-06 23:59**. Late assignments will incur a **20-point** deduction per day.
2. You must work on this homework individually. Any plagiarism will result in a zero grade for this assignment.
3. You can either type your answers in a word document or handwrite them and scan them as a pdf file.
4. **To get full marks for your answer, you need to show all the necessary steps of your derivations clearly. If you skip any steps, you will get zero grade for that part.**

Problem 1. Finite-state machine (40 points)

Finite state machines are a powerful way to systematically design sequential circuits from a written specification. Here is the procedure to design an FSM (Mealy machine):

a) Identify the inputs and outputs.
b) Sketch a state transition diagram.
c) Select state encodings—your selection affects the hardware design.
d) Write a combined state transition and output table.
e) Write Boolean equations for the next state and output logic.
f) Sketch the circuit schematic.

A series data detector is a sequential circuit that detects a specific pattern of bits in a binary input stream. In this problem, you will utilize D flip-flops to design a series data detector that has one input X and one output Y. The output Y should be 1 if and only if X has been 1 for three consecutive clock cycles. Otherwise, Y should be 0. For example:

Input X : 0 1 1 1 0 1 1 1 1 0 1 1 0…

Output Y: 0 0 0 1 0 0 0 1 1 0 0 0 0…

(Time sequence: From left to right)

1) Sketch a state transition diagram and select state encodings. **(Note: The number of states should be minimal) (10 points)**

2) Write the combined state transition and output table. **(10 points)**

3) Write Boolean equations for the next state and output logic. **(10 points)**

4) Sketch the circuit schematic (**Note: Use D flip flops**). **(10 points)**

(Hint: ① Two states are equivalent if they produce the same output for the same input and they lead to the same next state. Equivalent states can be merged into one state. ② Refer to Example 3.9 in reference book DDCA. ③ For this problem, the FSM is a Mealy machine.)

Problem 2. Analysis of an Inverting Amplifier (30 points)

In this problem, you will analyze some circuits that use ideal op-amps. An ideal op-amp is a device that has infinite input resistance, zero output resistance, and infinite open-loop gain. To analyze an ideal-op-amp circuit, you need to follow these steps:

a) Verify that negative feedback is present.
b) Assume that the differential input voltage and the input current of the op amp are forced to zero. (This is the summing-point constraint.)
c) Apply standard circuit-analysis principles, such as Kirchhoff's laws and Ohm's law, to solve for the quantities of interest.

1) Figure 2-1 shows a version of the inverting amplifier that can achieve high gain magnitude without using very large or very small resistor values, unlike the standard inverter configuration. Derive an expression for the output voltage under the ideal-op-amp assumption. Also, find the input impedance and output impedance. **(Note: The output voltage should be expressed as $v_{out} = f(v_{in})$).(10 points)**

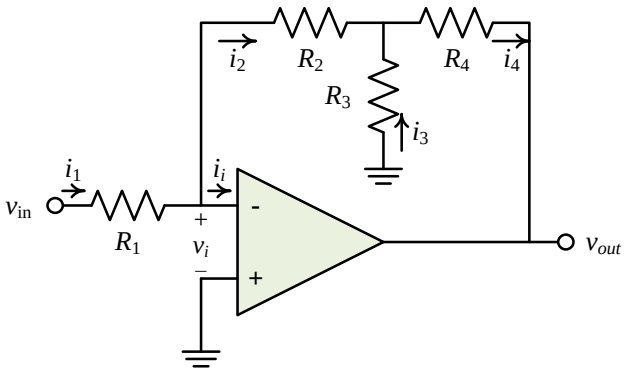

Fig. 2-1 T-type inverting amplifier circuit

2) Figure 2-2 shows a version of digital to analog (DAC) converter that use an inverting amplifier. In this circuit, inputs in volts are weighted in the summing amplifier to produce the corresponding analog voltage. Derive an expression for the output voltage under the ideal-op-amp assumption.

(Note: The output voltage should be expressed as $v_{out} = f(v_1, v_2, v_3, v_4)$). (10 points)

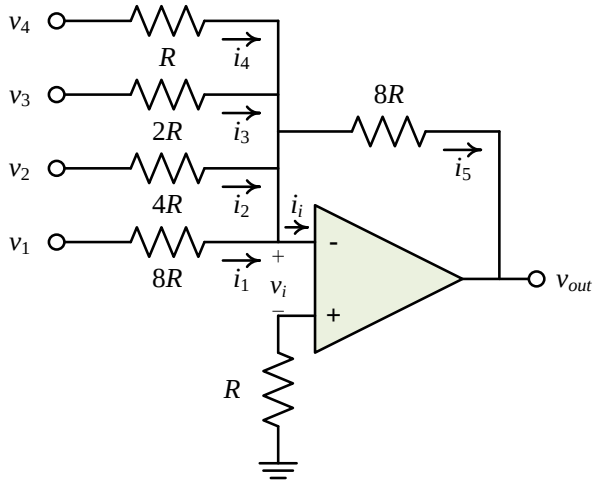

Fig. 2-2 DAC converter

3) An ideal amplifier can also be used to form a comparator, which is a device that compares two input voltages and produces a high or low output voltage depending on which one is larger. Figure 2-3 gives an example of comparator with a **Zener diode**, which is **a type of diode that has a constant voltage drop when it is reverse biased**. Assume that the forward voltage of this diode is 0.7V, and regulator voltage is 5V (The I/V characteristics of the Zener diode is shown in Figure 2-4). The input voltage is v_{in}=5sin(ωt), as shown in Figure 2-5(a). Sketch the waveform of output voltage v_{out} **on the Figure 2-5(b). (Note: The positive pole of DC voltage source is grounded.) (10 points)**

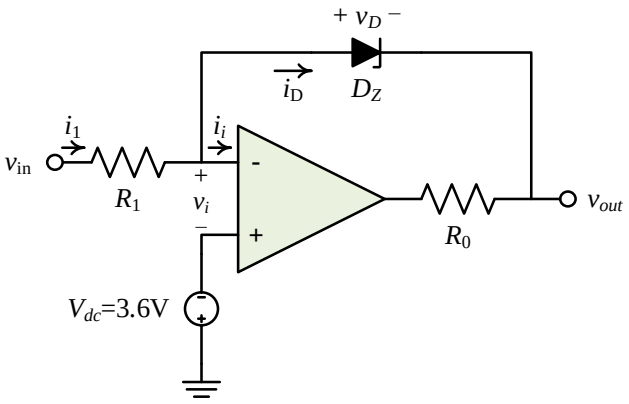

Fig. 2-3 Comparator circuit

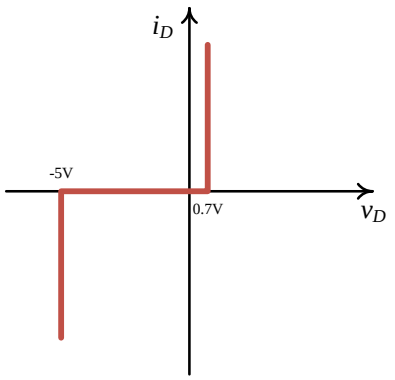

Fig. 2-4 I/V characteristics of Zener Diode

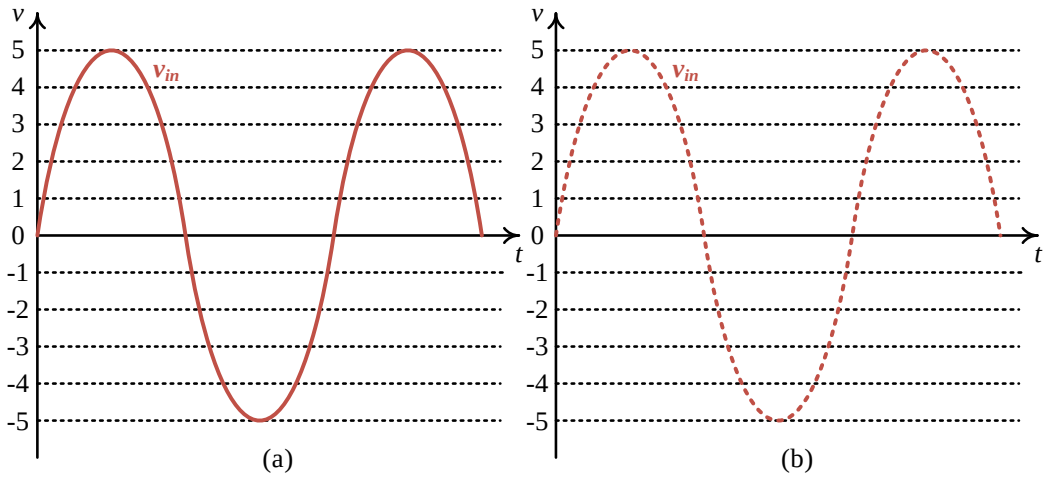

Fig. 2-5 Waveform of input voltage

(Hint: Refer to page 669-670 from reference book EEPA.)

Problem 3. NMOS Transistors (30 points)

Consider the NMOS devices shown in Figure 3-1, where the drains, sources, and gate ports are labeled. For each of the given biasing configurations, find the **mode of operation** (saturation, linear, or cutoff) and **the drain current I_D** of the device.

Use these transistor parameters:

Assume (W/L) =1 and neglect channel-length modulation and velocity saturation effects.

NMOS: $KP = 115\mu A/V^2$, $V_{T0} = 0.43V$

a) NMOS: $V_{GS} = 2.5V$, $V_{DS} = 2.5V$. **(10 points)**

b) NMOS: $V_{GS} = 3.3V$, $V_{DS} = 2.2V$. **(10 points)**

c) NMOS: $V_{GS} = 0.6V$, $V_{DS} = 0.1V$. **(10 points)**

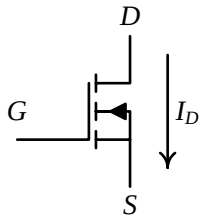

Fig. 3-1 NMOS Transistors

Hint: Refer to EEPA Section 11.1, especially Table 11.1.

The I/V characteristics of NMOS transistors can be expressed as follows

Linear region:

$$I_D = \frac{KP}{2}\frac{W}{L}\left[2(V_{GS} - V_{T0})V_{DS} - V_{DS}^2\right]$$

Saturation region:

$$I_D = \frac{KP}{2}\frac{W}{L}(V_{GS} - V_{T0})^2$$