


 上海科技大学
 ShanghaiTech University

EE115 Analog Circuits

Bias & Discrete Amp

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Outline

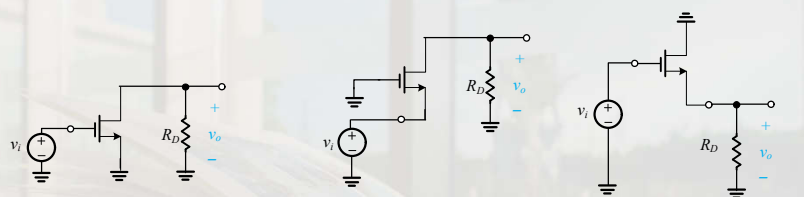
- Transistor Amplifier 3
 - Biasing
 - Discrete-Circuit Amplifiers
- Reading: SEDTRA/SMITH book pages 448-473


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Review: Basic Single-Transistor Amp. Config.



(a) Common source (CS) (b) Common Gate (CG) (c) Common Drain (CD) or Source Follower


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Purposes of Bias Circuit

- Provide a **stable** bias drain current
- Bias **insensitive** to variations in
 - Transistor parameters (V_b , k for MOS)
 - Temperature and other environmental changes
- Keep MOSFET in **flat part** of the I-V curves (**Saturation region**) for desired output swing


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Review: I-V Curves of NMOS

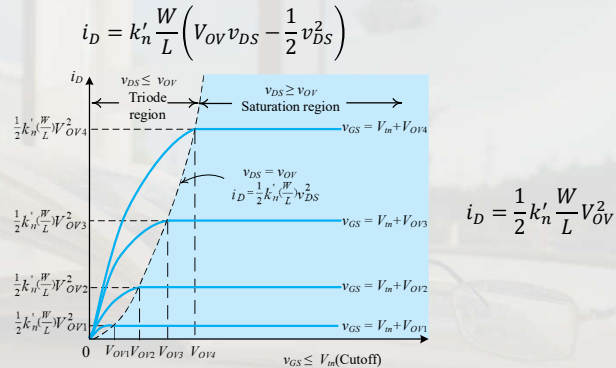


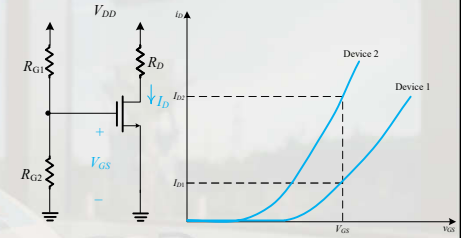
Fig. $i_D - v_{DS}$ characteristic for an enhancement-type NMOS transistor.

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Example of Non-Ideal Bias



- Fixed v_{GS} from voltage divider
- Large variation in i_D due to **device** variations
- Large **temperature** dependence
 - μ_n and V_t are temperature sensitive

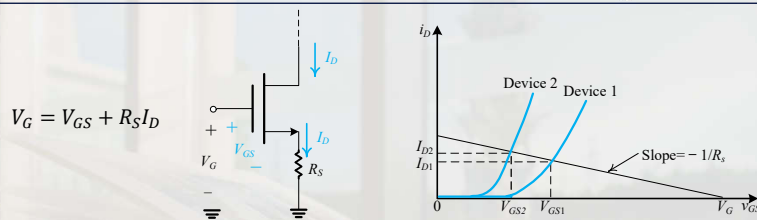


$$i_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (v_{GS} - V_t)^2$$



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Adding Source Resistance R_S



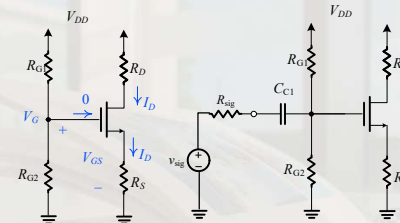
- R_S provides a **negative feedback**
 - If $I_D \uparrow$, $V_{GS} \downarrow \rightarrow I_D \downarrow$
 - If $I_D \downarrow$, $V_{GS} \uparrow \rightarrow I_D \uparrow$
- **Stabilize** I_D w.r.t. device and temperature variations

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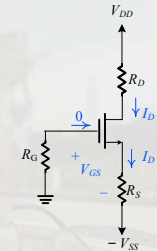
Practical Implementations



Single Power Supply



Dual Power Supply



How to select R_D ?

Rule of thumb: R_D , V_{DS} and R_S each has $1/3 V_{DD}$ voltage drop

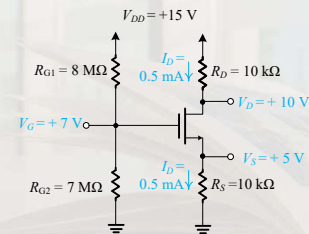


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Bias Example



Given: $I_D = 0.5 \text{ mA}$; $V_t = 1 \text{ V}$, $k_n = 1 \text{ mA/V}^2$, $\lambda = 0$. $V_{DD} = 15 \text{ V}$.
Calculate change in I_D when the MOSFET is replaced with another one with identical k_n but $V_t = 1.5 \text{ V}$



Solution:

Rule of thumb: R_D , V_{DS} and R_S each has

$1/3 V_{DD}$ voltage drop

$$R_D = \frac{V_{DD} - V_D}{I_D} = \frac{15 - 10}{0.5} = 10 \text{ k}\Omega$$

$$R_S = \frac{V_S}{I_D} = \frac{5}{0.5} = 10 \text{ k}\Omega$$

$$I_D = \frac{1}{2} k_n (W/L) V_{OV}^2$$

$$0.5 = \frac{1}{2} \times 1 \times V_{OV}^2$$

$$V_{GS} = V_t + V_{OV} = 1 + 1 = 2 \text{ V}$$

$$V_G = V_S + V_{GS} = 5 + 2 = 7 \text{ V}$$

Replace

$$I_D = \frac{1}{2} \times 1 \times (V_{GS} - 1.5)^2$$

$$V_G = V_{GS} + I_D R_S$$

$$7 = V_{GS} + 10 I_D$$

$$I_D = 0.455 \text{ mA}$$

$$\Delta I_D = 0.455 - 0.5 = -0.045 \text{ mA}$$



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Bias with large drain-to-gate R_G

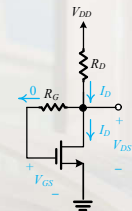


Fig. Biasing the MOSFET using a large drain-to-gate feedback resistance, R_G .

$$V_{GS} = V_{DS} = V_{DD} - R_D I_D$$

$$V_{DD} = V_{GS} + R_D I_D$$

- R_D provides a negative feedback

$$\triangleright I_D \uparrow, V_{GS} \downarrow \rightarrow I_D \downarrow$$

$$\triangleright I_D \downarrow, V_{GS} \uparrow \rightarrow I_D \uparrow$$

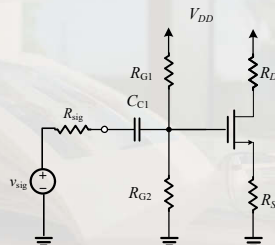
- **Stabilize I_D** w.r.t. device and temperature variations

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Coupling. Cap to Separate AC Signal from DC Bias



- Coupling capacitor is **DC-open** and **AC-short**
- **Prevent** signal source to **change** bias condition
- Coupling capacitor creates a **lower bound** of operating frequency



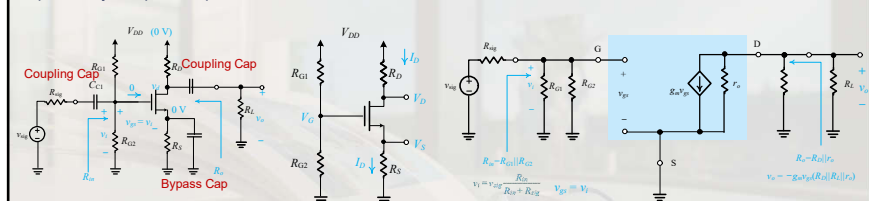
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CS Amplifier with Bias Circuit



- Both coupling and bypass capacitors are DC-open and AC-short

Capacitively Coupled Amplifier:



$$R_{in} = R_{G1} || R_{G2}$$

$$G_v = -\frac{R_{in}}{R_{in} + R_{sig}} g_m (R_D || R_L || r_o)$$



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Typical Freq. Response of Capacitively Coupled Amp. 上海科技大学
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