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EE115 Analog Circuits
Two Stage Amp & Freq Response Basis

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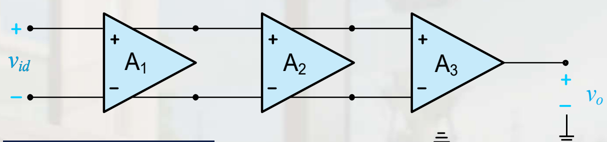
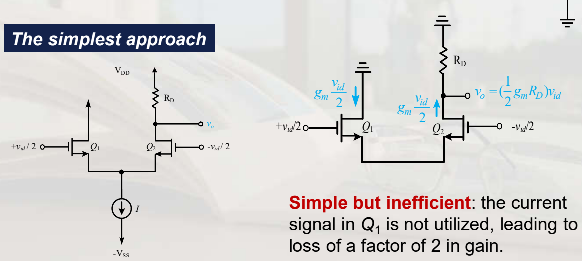
Outline

- Two-stage amplifier
- Reading: SEDTRA/SMITH book pages 640-644
- Frequency Response 1
- Reading: SEDTRA/SMITH book pages 673-680

Review: Differential-to-Single-Ended Conversion



The simplest approach



Simple but inefficient: the current signal in Q_1 is not utilized, leading to loss of a factor of 2 in gain.

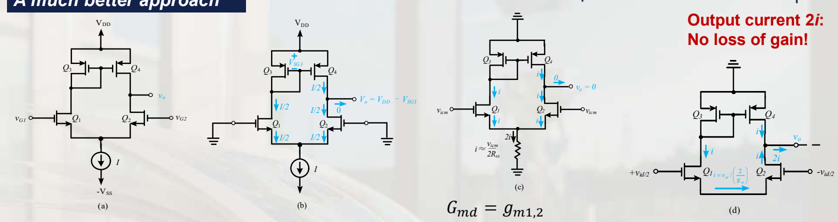
Review: Differential Pair w/ Current Mirror Load

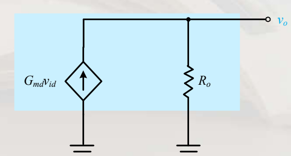
A much better approach

Common mode input

Differential input

Output current 2*i*: No loss of gain!





$$G_{md} = g_{m1,2}$$

$$R_o = r_{o2} || r_{o4} = R_{on} || R_{op}$$

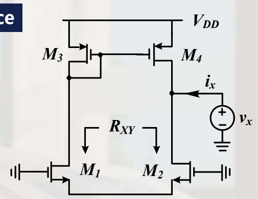
$$A_d \equiv \frac{v_o}{v_{id}} = G_{md} R_o = g_{m1,2}(r_{o2} || r_{o4})$$

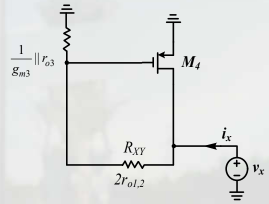
$$A_d = g_{m1,2}(R_{on} || R_{op})$$

$$A_d = \frac{1}{2} g_m r_o = \frac{1}{2} A_o$$

Differential Pair w/ Current Mirror Load

Output Resistance

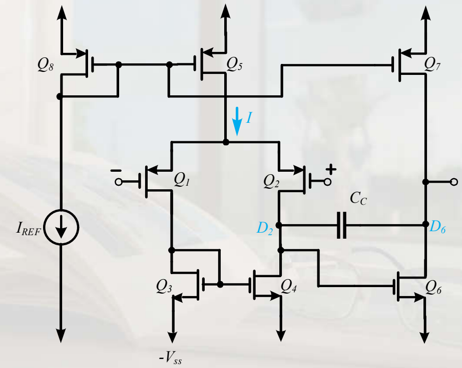




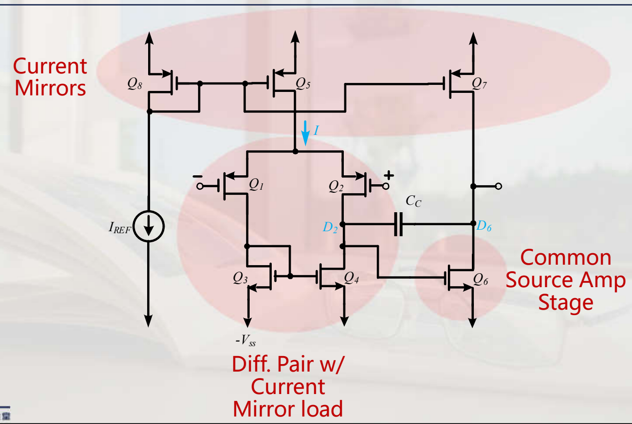
When v_x is applied to measure R_o, v_{g4} **varies!**
For ac analysis, I is OPEN, any current flowing into M_1 most flow out of M_2.
Hence, M_1 and M_2 can be represented by $R_{XY} = 2r_{o1,2}$.
Thus, the current drawn from v_x by R_{XY} is mirrored by M_3 into M_4 with unity gain(**Current doubled!**).

$$i_x = \mathbf{2}\frac{v_x}{2r_{o1,2} + \frac{1}{g_{m3}}||r_{o3}} + \frac{v_x}{r_{o4}} \qquad R_o = \frac{v_x}{i_x} = \frac{1}{\frac{1}{r_{o1,2} + \frac{1}{2g_{m3}}||r_{o3}} + \frac{1}{r_{o4}}} \cong r_{o2}||r_{o4}$$

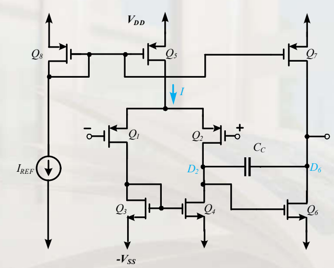
Two-Stage CMOS Op-Amp Circuit



Stages Scrutinize



Voltage Gains



- 1st stage (Q_1, Q_2): differential input, single-ended output:

$$A_1 = -g_{m1}(r_{o2}||r_{o4})$$

- 2nd stage (Q_6): common source amp. with current source load:

$$A_2 = -g_{m6}(r_{o6}||r_{o7})$$

- Total gain

$$A_o = A_1 A_2$$

Example: two stage op-amp

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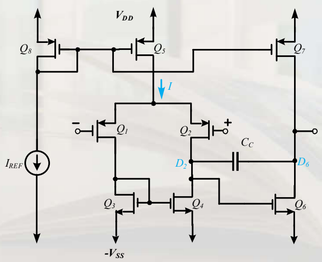
Transistor	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	Q_8
W/L	10/0.4	10/0.4	2.5/0.4	2.5/0.4	20/0.4	5/0.4	20/0.4	20/0.4



- I_{REF} = 100 μA, V_{tn} = 0.5 V, V_{tp} = -0.5 V, $\mu_n C_{ox}$ = 400 $\mu A/V^2$, $\mu_p C_{ox}$ = 100 $\mu A/V^2$, $|V_A|$ = 5 V for all devices V_{DD} = V_{SS} = 1 V.
- Find I_D, $|V_{OV}|$, $|V_{GS}|$, g_m, r_o for all Q's,
- Also find A_1, A_2, the dc open-loop voltage gain, input common mode range, output voltage range.

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Example: solution

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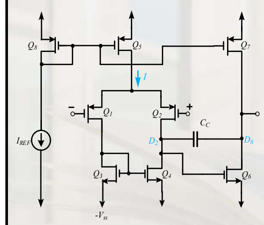

Transistor	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	Q_8
W/L	10/0.4	10/0.4	2.5/0.4	2.5/0.4	20/0.4	5/0.4	20/0.4	20/0.4

Table Determine I_D via mirroring

	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	Q_8
$I_D(\mu A)$	50	50	50	50	100	100	100	100
$\lvert V_{GS}\rvert$(V)	0.7	0.7	0.7	0.7	0.7	0.7	0.7	0.7
$\lvert V_{ov}\rvert$(V)	0.2	0.2	0.2	0.2	0.2	0.2	0.2	0.2
g_m(mA/V)	0.5	0.5	0.5	0.5	1	1	1	1
r_o(kΩ)	100	100	100	100	50	50	50	50

$$I_D = \frac{1}{2}(\mu C_{ox})\left(\frac{W}{L}\right)V^2{}_{ov}$$
$$g_m = \frac{2I_D}{|V_{ov}|}$$
$$r_o = |V_A|/I_D$$

$$A_1 = -g_{m1}(r_{o2}||r_{o4}) = -0.5(100||100) = -25V/V$$
$$A_2 = -g_{m6}(r_{o6}||r_{o7}) = -1(50||50) = -25V/V$$
$$A_o = A_1A_2 = 25 \times 25 = 625V/V$$
$$20\log 625 = 56dB$$

$$V_{ICMmin} = -1.0 + 0.7 + 0.2 - 0.7 = -0.8V$$
$$V_{ICMmax} = 0.8 - 0.7 = +0.1V$$
$$V_{omax} = 1.0 - 0.2 = 0.8V$$
$$V_{omin} = -1.0 + 0.2 = -0.8V$$

Typical Frequency Response of Discrete MOS Amplifiers

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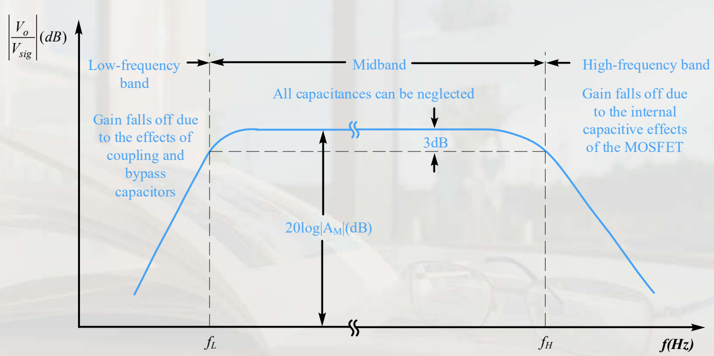

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Low Frequency Dominant Pole Approximation

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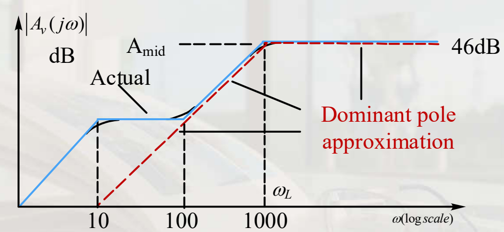
- A ***Dominate Pole*** exists if one of the low frequency poles is much larger than the others.



- In the graph above, ω = 1000 rad/sec is a dominant pole.
- All other poles and zeros are at low enough frequencies that they do not affect the lower cutoff frequency ω_L.

Frequency Response of Direct-Coupled (IC) Amp

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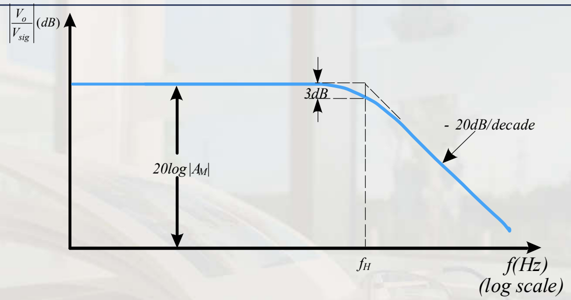

- Gain does not fall off at low frequencies
- Midband gain A_m extends down to **zero frequency**

Cross Section of MOSFET Showing Internal Cap.

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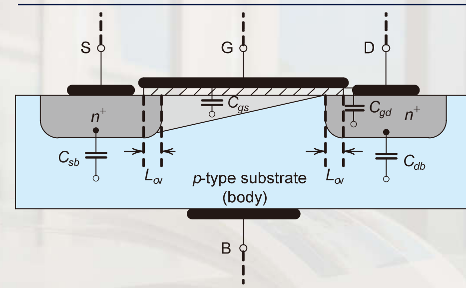

- MOSFET has several internal capacitances, which take time to charge/discharge, limiting the transistor speed.

- Gate/Source capacitance:

$$C_{gs} = \frac{2}{3}WLC_{ox} + C_{ov}$$

where

- $C_{ox} = \varepsilon_{ox}/t_{ox}\ [F/cm^2]$
- W: Transistor width
- L: Gate Length
- $C_{ov} = WL_{ov}C_{ox}$
- L_{ov}: overlap between Gate/source or gate/drain, typically 0.05-0.1L

- Gate/Drain capacitance:

$$C_{gd} = C_{ov}$$

MOSFET High-f Equivalent-Circuit Model

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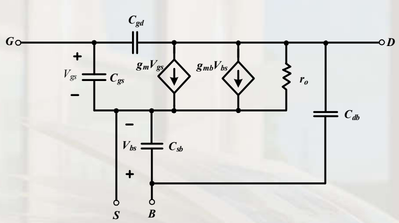

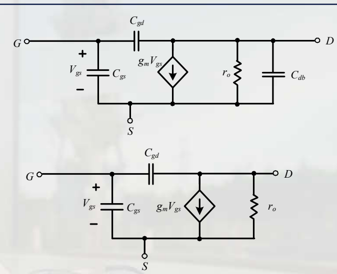

- Source is connected to the body (no **body effect**)
- Capacitance between drain and body C_{db} neglected

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Unity-Gain Frequency, f_T

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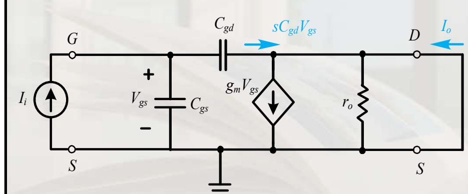
- f_T: frequency at which short-circuit current gain =1
  - FoM for transistor speed
  - Drain is grounded (short-circuit load)



$$I_o = g_mV_{gs} - sC_{gd}V_{gs} = (g_m - sC_{gd})V_{gs}$$

$$V_{gs} = \frac{I_i}{s(C_{gs}+C_{gd})}$$

Combine: $\frac{I_o}{I_i} = \frac{g_m - sC_{gd}}{s(C_{gs}+C_{gd})}$

$$\left|\frac{I_o}{I_i}\right|(s = j\omega_T) \cong \frac{g_m}{\omega_T(C_{gs}+C_{gd})} = 1$$

Unity gain freq.: $\omega_T = \frac{g_m}{(C_{gs}+C_{gd})}$

$$f_T = \frac{g_m}{2\pi(C_{gs}+C_{gd})}$$

As gate length reduces in advanced technology, C_{gs} reduces and f_T increases